IBM Maintenance Library

3705 Communications Controller
Theory—Maintenance
Volume I

SY27-0107-6

PREFACE

This publication is directed to the General Systems Customer Engineer assigned to maintain the IBM 3705 Communications Controller. He is assumed to be trained on either a System/360 or System/370 CPU and to have a teleprocessing background.

This publication should be used to locate and replace failing field replaceable units within the 3705. Pictures are combined with text to convey both comprehensive "how to fix" information and basic operational concepts. No attempt is made to provide detailed theory information. Each page contains one topic (although some topics may require more than one page). Tabs in the table of contents provide quick access to the individual sections.

There are two versions of the 3705, one with bridge storage and one with FET storage. In this manual references to the 3705 will be common to both versions. References to the 3705-I will apply to the bridge storage version and references to the 3705-II will apply to the FET storage version.

The CE should always start at the "Maintenance Philosophy" section when trying to locate a failure. This section contains a flowchart that points to the correct part of the manual for locating the failure.

Although this manual is packaged as one unit, it is divided into three volumes, which may be placed in separate binders for ease of use.

Volume one contains an abbreviation list, legend, the composite table of contents, maintenance philosophy, introduction to the 3705, a description of the control panel switches and lights and procedures for using them, diagnostic aids, ROS tests, IPL, and the theory-maintenance sections on the central control unit, storage, and type 1 channel adapter. A composite index of all three volumes is at the back of each volume.

Volume two contains an abbreviation list, legend, a volume table of contents, and the theory-maintenance sections on the type 2 channel adapter, the type 1 communication scanner the type 2 communication scanner, the line interface bases, and the line sets. A composite index of all three volumes is at the back of each volume.

Volume three contains an abbreviation list, legend, a volume table of contents and the theory-maintenance sections on the power supply, the type 3 communication scanner, the type 3 channel adapter and the type 4 channel adapter. It also contains information on test tools and equipment, preventive maintenance, and physical locations. A composite index of all three volumes is at the back of each volume.

The CE may reduce the size of this manual at his discretion. A 3705 may contain a type 1 or a type 2 communication scanner, but not both; therefore the CE can discard the theory-maintenance section that describes the scanner not included in the system. The CE can also discard the theory-maintenance section for the type 1 channel adapter, for the type 2 channel adapter, for the type 3 channel adapter, or for the type 4 channel adapter if that adapter is not included in the system. Sections should be removed from the system manual only; the CE should retain all sections in his own copy. (Remember that any pages discarded will still be listed in the index and in the table of contents.) A new system manual must be ordered if the system is expanded to include a different type of scanner or adapter. Individual sections cannot be ordered.

Prerequisiste Publication:

Introduction to the 3704 and 3705 Communications Controllers, GA27-3051

Related Publications:

IBM 3704 and 3705 Communications Controllers:
- Principles of Operation, GC30-3004
- Original Equipment Manufacturers' Information, GA27-3053

IBM 3705 Parts Catalog, S131-0032

System/360 Operating System Online Test Executive Program, GC28-6650

DOS OLTEP SRL, GC24-5086

OLTSEP Operators' Guide, D99-SEPDT

System/360 and System/370 I/O Interface Channel to Control Unit Original Equipment Manufacturers' Information, GA22-6974

IBM Maintenance Diagnostic Program IBM 3705 Communications Controller Channel Adapter On-Line Test and Wrap All-Lines, On-Line Test D99-3705C.

IBM Maintenance Diagnostic Program IBM 3705 Communications Controller Internal Functional Test Loader, Diagnostic Control Module, Initial Test, and Panel Line Test D99-3705D.

IBM Maintenance Diagnostic Program IBM 3705 Communications Controller Internal Functional Test Symptom Indexes D99-3705E.

Guide to Using the IBM 3705 Communications Controller Control Panel, GA27-3087

On-Line Terminal Test (OLTT)

IBM Maintenance Document On-Line Terminal Test User's Guide, D99-3700A

On-Line Line Test (OLLT)

- IBM Maintenance Document Program 3704/3705 Communications Scanner On-Line Line Test, D99-3700C (for NCP-3 or later)
- IBM Maintenance Document Program 3705 Communications Scanner On-Line Line Test, D99-3705B (for NCP-1 or 2)

Summary of Changes for SY27-0107-4

This revision contains new information about (1) 3705-II, (2) FET storage, (3) type 3 communication scanner, (4) type 4 channel adapter, (5) LIB type 12, and (6) Line sets 12A and 12B. This revision contains the following changes:

- Line sets 12A and 12B require that 'modem receive space' keep SCF 0 (Receive Break) set for five consecutive character times before the control program interprets this condition as a break signal. (The IBM 3767 Communication Terminal sends the 450 Hz break signal for six character times while the 3705 sends the 450 Hz break signal for three character times.)
- Diagnostic jumpering procedures to use the 'clock step' latch to freeze the clock have been updated.
- Unit and frequency codes have been added to the P.M. requirements.

In addition minor corrections and changes have been made. The page headings and the keying symbols have been changed for standardization.

Summary of Changes for SY27-0107-5

This revision contains new information about (1) Line Sets 1T and 1U, (2) the Remote Program Loader-II for the 3705-II and its impact on IPL, (3) multiple type 4 channel adapters, (4) N-channel ROS for the type 4 channel adapter, (5) 3705-II feature board locations, (6) 3705-II allowable hardware combinations and control panel configurations, (7) a procedure to clock step thru IPL phase 2 (load ROS), (8) a procedure to determine intermittent FET storage address errors, and (9) an IPL data flow.

The IPL phase 1 and 2 Timing chart has been expanded and minor corrections and changes have been made.

Summary of Changes for SY27-0107-6

This revision contains new information about (1) additional FET storage provided by 3705-II Models J-L, (2) 900 nanosecond cycle time, (3) Line Sets 1W and 1Z, and (4) the Cycle Utilization Counter Register. The new information affects sections describing:

- FET storage data flow and timings
- Physical Locations
- Card functions and locations
- Input and Output instructions
- Power supply information
- Line set and LIB information
- Channel adapters
- Communication scanners

In addition, minor corrections and changes have been made.

Seventh Edition (May 1979)

Changes are periodically made to the information herein; any such changes will be reported in subsequent revisions or technical newsletters. Before using this publication in connection with the servicing of IBM systems or equipment, refer to the latest edition that is applicable and current.

It is possible that this material may contain reference to, or information about, IBM products (machines and programs), programming or services which are not announced in your country. Such references or information must not be construed to mean that IBM intends to announce such IBM products, programming or services in your country.

Publications are not stocked at the address given below; requests for IBM publications should be made to your IBM representative or to the IBM branch office serving your locality.

This manual has been written by the IBM System Communications Division, Publications Development, Department E02, P.O. Box 12195, Research Triangle Park, North Carolina 27709. A reader's comment form is provided at the back of this publication. If the form has been removed, comments may be sent to the above address. IBM may use or distribute any of the information you supply in any way it believes appropriate without incurring any obligation whatever. You may, of course, continue to use the information you supply.

IBM has prepared this maintenance manual for the use of IBM customer engineers in the installation, maintenance, and repair of the specific machines indicated. IBM makes no representations that it is suitable for any other purpose.

ABBREVIATIONS

A	And circuit or ampere
AA	automatic answering
ABAR	attachment buffer address register
ABO	adapter bus out (register)
ac	alternating current
ACO	automatic call originate
ACF/NCP/ VS	Advanced Communications Function for Network Control Program/Virtual Storage
ACR	abandom call and retry
ACU	automatic calling unit
adr	address
AEQ	automatic equalizer
AHR	add halfword register (instruction)
ALD	automated logic diagram
ALU	arithmetic logic unit
AMP	amplifier
APAR	authorized program analysis report
AR	add register (instruction)
ARI	add register immediate (instruction)
B	branch (instruction)
BAL	branch and link (instruction)
BALR	branch and link register (instruction)
BAR	buffer address register
BB	branch on bit (instruction)
BC	bit clock
BCB	bit control block
BCC	bit clock control
BCL	branch on C latch (instruction)
BCT	branch on count (instruction)
BO	bus out
BP	break point
bps	bit per second
BSC	binary synchronous communication
BSM	bridge storage module
BZL	branch on Z latch (instruction)
CA	channel adapter
CACHKR	channel adapter check register
CACR	channel adapter control register
CADB	channel adapter data buffer
CAMR	channel adapter mode register
CASNSR	channel adapter sense register
CASTR	channel adapter status register
CB	circuit breaker
CBAR	CSB buffer address register
CCB	character control block
CCR	compare character register (instruction)
CCT	coupler cut through (modem)
CCU	central control unit
CD	carrier detect
CDS	configuration data set
CE	Channel End (status)
chan	channel
char	character
CHR	compare halfword register (instruction)
ck	check
clk	clock
cm	centimeter
CMDR	channel adapter command register
CMND	command
com	common
COS	Call Originate Status
CP	circuit protector
CPU	central processing unit
CR	compare register (instruction)
CRC	cyclic redundancy check
CRI	compare register immediate (instruction)
CRQ	Call Request
CS	cycle steal
CSAR	cycle steal address register
CSB	communication scanner
CSCD	clear to send, carrier detect
CSMC	cycle steal message counter
ctrl	control
CTS	Clear To Send
CUCR	Cycle Utilization Counter Register
CUE	Control Unit End (status)
CW	control word
CWAR	control word address register
CWCNTR	control word byte count register
DAA	data access arrangement
DA	data modem ready
dB	decibel
DBAR	diagnostic buffer address register
dc	direct current
DCE	data circuit-terminating equipment
DCM	diagnostic control module
DCR	data channel ready
DE	Device End (status)
DET	detector
diag	diagnostic
dist	distance
DLO	data line occupied
DOS	Disk Operating System
DPR	digit present
DR	display register or data ring (modem)
DCS	distant station connect (ACO only)
DSR	data set ready
DT	data tip (modem)
DTE	data terminal equipment
DTR	data terminal ready
EC	edge connector
EB	extended buffer
ECP	emulation control program
EIA	Electronic Industries Association
enbl	enable
EON	end of number (ACO only)
EPO	emergency power off
ESC	emulation subchannel
EXT	external
FCS	final control sequence
FET	field effect transistor modem card
FETOM	Field Engineering Theory of Operation Manual
FF	flip flop
FL	flip latch
FRU	field replaceable unit
GB	ground bus
gnd	ground
hex	hexadecimal
HIfwd	halfword
horz	horizontal
HS	heat sink
Hz	Hertz
I	instruction (cycle)
IAR	instruction address register
IC	insert character (instruction)
ICS	initial control sequence
ICT	insert character and count (instruction)
ICW	interface control word
IFT	internal functional test
IN	input (instruction)
INCWAR	inbound control word address register
Init	initial
int	internal
intf	interface
I/O	input/output
IPL	initial program load
IR	interrupt remember
ISACR	initial selection address and command register
L	load (instruction)
LA	load address (instruction)
LAR	lagging address register
LCD	line code definer
LCOR	load character with offset register (instruction)
LCR	load character register (instruction)
LED	light emitting diode
LGF	leading graphics flag
LH	load halfword (instruction)
LHOR	load halfword with offset register (instruction)
LHR	load halfword register (instruction)
LIB	line interface base
lim	limiter
LOR	load with offset register (instruction)
LOSC	last oscillator sample condition
LR	load register (instruction)
LRI	load register immediate (instruction)
LS or ls	local store
lt	latch
L1	level 1
L2	level 2
L3	level 3
L4	level 4
L5	level 5
mA	milliampere
Mem TB	memory terminal board
modem	modulator/demodulator
ms/divn	milliseconds per division
MST	monolithic system technology
mV	millivolt
NB	Digit Signal
N/C	normally closed
NCP	network control program
NCR	and character register (instruction)
NHR	and halfword register (instruction)
N/O	normally open
NR	and register (instruction)
NRI	and register immediate (instruction)
NRZI	non-return-to-zero inverted
ns	nanoseconds
NSC	native subchannel
OBR	outboard recorder
O/C	overcurrent
OCR	or character register (instruction)
OE	exclusive or
OH	off hook (modem)
OHR	or halfword register (instruction)
OLT	on line test
OLTEP	on line test executive program
OLTLIB	on line test library
OLTSEP	on line test standalone executive program
op	operation
op reg	operation register
OR	or register (instruction)
ORI	or register immediate (instruction)
OS	Operating System
OSC	oscillator
OUT	output (instruction)
OUTCWAR	outbound control word address register
OVRN	overrun
O/V	overvoltage
P	parity
PC	parity check
PCF	primary control field
PCI	program controlled interrupt
PDF	parallel data field
PEP	partitioned emulation programming
PG	parity generation
pgm	program
PH	polarity hold
PND	Present Next Digit
P/N	part number
POR	power on reset
pos	position

POSC	present oscillator sample condition
pot	potentiometer
P-P	post processor modem card
PPB	prime power box
PUT	programmable unijunction transistor
PWI	power indicator
R	resistance or resistor
rcv	receive
rd	read
rdy	ready
RE	register and external register (instructions)
ref	reference
reg	register
regen	regenerative
req	request
RI	register immediate (instruction) or ring indicator (modem)
RLSD	receive line signal detector
RMS	root mean square
ROS	read-only storage
RPL	remote program loader
RR	register to register (instructions)
RS	register to storage (instructions)
RSA	register and storage with addition (instructions)
RT	register branch or register and branch (instructions)
RTS	Request To Send
rly	relay
SAR	storage address register
SCF	secondary control field
SCR	silicon controlled rectifier or subtract character register (instruction)
SCRID	silicon controlled rectifier indicator driver
SDF	serial data field
SDLC	synchronous data link control
SDR	storage data register
sec	second
sel	selection
SEP	separator (ACO only)
seq	sequence
SG	signal ground
SH	switch hook (modem)
SHR	subtract halfword register (instruction)
SIG	signal
SIO	start I/O
SMS	standard modular system
SR	subtract register (instruction)
SRI	subtract register immediate (instruction)
SRL	Systems Reference Library
S/S	start/stop
ST	store (instruction)
STC	store character (instruction)
STCT	store character and count (instruction)
STH	store halfword (instruction)
stk	stacked
svc	service
sw	switch
SYN	synchronous idle
sync	synchronization or synchronous
TAR	temporary address register
TB	terminal board
TIC	Transfer In Channel
tr	trigger
TRM	test register under mask (instruction)
TSL	Technical Service Letter
T2	test 2
T3	test 3
T4	test 4
UC	Unit Check (status)
UE	Unit Exception (status)
V	volts
V/divn	volts per division
wd	word
wr	write
XCR	exclusive-or character register (instruction)
xfer	transfer
xfmr	transformer
XHR	exclusive-or halfword register (instruction)
xmt	transmit
XR	exclusive-or register (instruction)
XRI	exclusive-or register immediate (instruction)
2W	two-wire line connection (implies half-duplex)
4W	four-wire line connection (implies duplex, but actual duplex depends on the line set type and telephone company equipment.

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CONTENTS

LOCATION OF LOGIC PAGES BY VOLUME NUMBER

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3	DF–DZ	CCU
4	RA–RS	Type 1 scanner and channel adapter
A04	PA-PS	Type 4 channel adapter
5	QA–QN	Type 2 channel adapter
A05	SA-SQ	Type 3 channel adapter
6	TA–TB	Type 2 scanner
7	VA	Type 1 LIB–reference material
8	VB	Type 1 LIB–line sets 1A, 1B, 1C, 1D, 1E, 1F, 1G, 1GA, 1H, 1J, 1K, 1N, 1R, 1S, 1T, 1TA, 1U, 1W, 1Z
9	VC–VD	Type 2 LIB–line set 2A
10	VE–VF	Type 3 LIB–line sets 3A, 3B
11	VG–VH	Type 4 LIB–line sets 4A, 4B, 4C
12	VJ	Type 5 LIB–line sets 5A, 5B
13	VL	Type 6 LIB–line set 6A
14	VN	Type 7 LIB
15	VQ	Type 8 LIB–line sets 8A, 8B
16	VS	Type 9 LIB–line set 9A
17	GA–GC	Remote Program Loader Diskette Controller
18	VU	Type 10 LIB–line set 10A
19	VW	Type 11 LIB–line sets 11A, 11B
20	VX	Type 12 LIB–line sets 12A, 12B
21	MM	FET storage (3705-II)
22	TD-TE	Type 3 or 3HS scanner
23	TF	Type 3 or 3HS scanner
24	TA-TB	Type 2 scanner (3705-II)

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CE SAFETY PRACTICES

All Customer Engineers are expected to take every safety precaution possible and observe the following safety practices while maintaining IBM equipment:

1. You should not work alone under hazardous conditions or around equipment with dangerous voltage. Always advise your manager if you MUST work alone.
2. Remove all power AC and DC when removing or assembling major components, working in immediate area of power supplies, performing mechanical inspection of power supplies and installing changes in machine circuitry.
3. Wall box power switch when turned off should be locked or tagged in off position. "Do not Operate" tags, form 229-1266, affixed when applicable. Pull power supply cord whenever possible.
4. When it is absolutely necessary to work on equipment having exposed operating mechanical parts or exposed live electrical circuitry anywhere in the machine, the following precautions must be followed.
   a. Another person familiar with power off controls must be in immediate vicinity.
   b. Rings, wrist watches, chains, bracelets, metal cuff links, shall not be worn.
   c. Only insulated pliers and screwdrivers shall be used.
   d. Keep one hand in pocket.
   e. When using test instruments be certain controls are set correctly and proper capacity, insulated probes are used.
   f. Avoid contacting ground potential (metal floor strips, machine frames, etc. – use suitable rubber mats purchased locally if necessary).
5. Safety Glasses must be worn when:
   a. Using a hammer to drive pins, riveting, staking, etc.
   b. Power hand drilling, reaming, grinding, etc.
   c. Using spring hooks, attaching springs.
   d. Soldering, wire cutting, removing steel bands.
   e. Parts cleaning, using solvents, sprays, cleaners, chemicals, etc.
   f. All other conditions that may be hazardous to your eyes. REMEMBER, THEY ARE YOUR EYES.
6. Special safety instructions such as handling Cathode Ray Tubes and extreme high voltages, must be followed as outlined in CEM's and Safety Section of the Maintenance Manuals.
7. Do not use solvents, chemicals, greases or oils that have not been approved by IBM.
8. Avoid using tools or test equipment that have not been approved by IBM.
9. Replace worn or broken tools and test equipment.
10. Lift by standing or pushing up with stronger leg muscles—this takes strain off back muscles. Do not lift any equipment or parts weighing over 60 pounds.
11. All safety devices such as guards, shields, signs, ground wires, etc. shall be restored after maintenance.
12. Each Customer Engineer is responsible to be certain that no action on his part renders product unsafe or exposes hazards to customer personnel.
13. Place removed machine covers in a safe out-of-the-way place where no one can trip over them.
14. All machine covers must be in place before machine is returned to customer.
15. Always place CE tool kit away from walk areas where no one can trip over it (i.e., under desk or table).
16. Avoid touching mechanical moving parts (i.e., when lubricating, checking for play, etc.).
17. When using stroboscope—do not touch ANYTHING—it may be moving.
18. Avoid wearing loose clothing that may be caught in machinery. Shirt sleeves must be left buttoned or rolled above the elbow.
19. Ties must be tucked in shirt or have a tie clasp (preferably nonconductive) approximately 3 inches from end. Tie chains are not recommended.
20. Before starting equipment, make certain fellow CE's and customer personnel are not in a hazardous position.
21. Maintain good housekeeping in area of machine while performing and after completing maintenance.

KNOWING SAFETY RULES IS NOT ENOUGH
AN UNSAFE ACT WILL INEVITABLY LEAD TO AN ACCIDENT
USE GOOD JUDGMENT – ELIMINATE UNSAFE ACTS

229-1264-1

Artificial Respiration
GENERAL CONSIDERATIONS

1. **Start Immediately, Seconds Count**
   Do not move victim unless absolutely necessary to remove from danger. Do not wait or look for help or stop to loosen clothing, warm the victim or apply stimulants.
2. **Check Mouth for Obstructions**
   Remove foreign objects—Pull tongue forward.
3. **Loosen Clothing—Keep Warm**
   Take care of these items after victim is breathing by himself or when help is available.
4. **Remain in Position**
   After victim revives, be ready to resume respiration if necessary.
5. **Call a Doctor**
   Have someone summon medical aid.
6. **Don't Give Up**
   Continue without interruption until victim is breathing without help or is certainly dead.

Rescue Breathing for Adults
Victim on His Back Immediately

1. **Clear throat** of water, food, or foreign matter.
2. **Tilt head back** to open air passage.
3. **Lift jaw up** to keep tongue out of air passage.
4. **Pinch nostrils** to prevent air leakage when you blow.
5. **Blow** until you see chest rise.
6. **Remove your lips** and allow lungs to empty.
7. **Listen** for snoring and gurglings, signs of throat obstruction.
8. **Repeat mouth to mouth breathings** 10-20 times a minute.

Continue rescue breathing until he breathes for himself.

NO

Thumb and finger positions

Final mouth to mouth position

Reprint Courtesy Mine Safety Appliances Co.

LOCATION OF LOGIC PAGES BY VOLUME NUMBER

Volume	Logic Pages	Contents
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4	RA—RS	Type 1 scanner and channel adapter
A04	PA-PS	Type 4 channel adapter
5	QA—QR	Type 2 channel adapter
A05	SA—SR	Type 3 channel adapter
6	TA—TB	Type 2 scanner
7	VA	Type 1 LIB—reference material
8	VB	Type 1 LIB—line sets 1A,1B,1C,1D,1E,1F,1G, 1GA, 1H, 1J, 1K, 1N, 1S, 1T, 1TA, 1U, 1W, 1Z
9	VC—VD	Type 2 LIB—line set 2A
10	VE—VF	Type 3 LIB—line sets 3A, 3B
11	VG—VH	Type 4 LIB—line sets 4A, 4B, 4C
12	VJ	Type 5 LIB—line sets 5A, 5B
13	VL	Type 6 LIB—line set 6A
14	VN	Type 7 LIB
15	VQ	Type 8 LIB—line sets 8A, 8B
16	VS	Type 9 LIB—line set 9A
17	GA—GC	Remote Program Loader Diskette Controller
18	VU	Type 10 LIB—line set 10A
19	VW	Type 11 LIB—line sets 11A, 11B
20	VX	Type 12 LIB—line sets 12A, 12B
21	MM	FET storage (3705-II)
22	TD-TE	Type 3 or 3HS scanner
23	TF	Type 3 or 3HS scanner
24	TA-TB	Type 2 scanner (3705-II)

MAINTENANCE PHILOSOPHY

This manual is intended as a tool for the Customer Engineer to use while repairing the IBM 3705 Communications Controller. This section of the manual presents a planned approach to maintenance problems that will help make repair faster. This planned approach is based on error detection, recovery and recording, error isolation, repair, and repair verification.

Error Detection, Recovery, and Recording

Hardware error detection circuits work with the control program. Many hardware detected errors result in a level 1 program interrupt so that the appropriate error recovery procedure can be started, or an orderly shutdown of the system can occur.

Refer to the " Diagnostic Aids " section of one of these five manuals, depending upon which control program you are using, for a description of the control program's error recovery procedures and error recording functions:

IBM 3704 and 3705 Communications Controller Emulation Program—Program Logic Manual for 3705 with type 1 Channel Adapter, SY30-3001.

IBM 3704 and 3705 Communications Controller Emulation Program—Program Logic Manual, for 3705 with type 4 Channel Adapter, SY30-3031.

IBM 3704 and 3705 Communications Controller Network Control Program—Program Logic Manual, SY30-3003.

IBM 3704 and 3705 Communications Controller Network Control Program/VS—Program Logic Manual, SY30-3007.

IBM 3704 and 3705 Communications Controller, Network Control Program/VS, version 5—Program Logic Manual, SY30-3013.

ACF/NCP/VS Network Control Program Logic, LY30-3041.

If some other control program is being used, refer to the documentation for that program to see how it handles error detection, recovery, and recording.

Error Isolation

You are provided a series of test programs to use with the 3705.

The first of these is the ROS (read-only storage) test which is automatic with each IPL attempt. ROS testing is limited to those functions needed to transfer more extensive test programs across the channel from the CPU. ROS testing and error analysis are described in the *ROS TEST* section of this manual. For Remote 3705s, see the *Remote Program Loader Diagnostic Manual.* The ROS test requires dedicated use of the 3705.

The second test is the Initial Test which is also automatic with each IPL unless optioned out by the customer. The initial test is more extensive that ROS testing, but it does not completely test all of the 3705 hardware. The initial test and its associated error indications are described in the *Initial Test* section of *IBM Maintenance Program IBM 3705 Communications Controller Internal Functional Test Loader, Diagnostic Control Module Panel Line Test, and Initial Test, D99-3705D.* For remote 3705s, see the *Remote Program Loader Diagnostic Manual.* The initial test requires dedicated use of the 3705.

The most comprehensive of the tests provided are the Internal Functional Tests (IFTs). These tests run under control of the Diagnostic Control Module (DCM) and require dedicated use of the 3705 Controller. The IFTs are described in the *IBM Maintenance Diagnostic Program — IBM 3705 Communications Controller Internal Function Test Loader, Diagnostic Control Module, Panel Line Test, and Initial Test,* D99-3705D. Further explanations of the IFTs and their error indications are provided in the *IBM Maintenance Diagnostic Program IBM 3705 Communications Controller Internal Functional Test Symptom Indexes D99-3705E.* For Remote 3705s, see the *Remote Program Loader Diagnostic Manual.*

Terminal On-Line Tests, channel On-Line Tests, and panel procedures are also provided. The OLTs are described in the *IBM Maintenance Diagnostic Program 3705 Communications Controller On-Line Test and Wrap All Lines Test,* D99-3705C.

In addition to the test programs, control panel check-out procedures are provided to check out some of the 3705 hardware. These procedures are described in the *Control Panel* section of this manual.

Repair

Repair will generally consist of replacing a field replaceable unit (FRU), or making an adjustment in main storage or the power supply.

Repair Verification

Running appropriate sections of the diagnostic test programs will generally verify proper operation of the controller and be justification to return the system to the customer.

MAINTENANCE PROCESS

Some effort is required to determine why a failure occurred, whether it halts operations of the 3705, or permits recovery. The process of locating the failure is divided into three steps or phases: problem determination, problem definition, and problem isolation.

Problem Determination

In this step, either customer personnel or you determine which unit in the teleprocessing network is failing. Failures may be in the CPU, the 3705, a down-line terminal, a modem, the communications line or a remote 3705, if one is installed in the network.

Problem Definition

This step defines the failure to a functional unit. If the 3705 is still in use by the customer, the course of action is different than if the customer cannot use the controller. In either case, deciding which test procedure to use is primary.

- Control Panel
  The control panel can be used to check out certain hardware functions without loading a test program. The procedures that can be performed are explained in the "Control Panel" section of this manual.

- ROS Test
  This test is automatic with an IPL operation and tests a basic subset of the CCU hardware. The error analysis procedure for this test is explained in the "ROS" section of this manual. For Remote 3705s, see the *Remote Program Loader Diagnostic Manual.* The control panel must be used to locate errors detected by this test. The customer cannot use the machine when these tests are in use.

- Initial Test
  This test is automatic with an IPL operation unless optioned out by the customer. It tests a portion of the CCU hardware not tested by ROS. See the *Initial Test* section of *IBM Maintenance Diagnostic Program 3705 Communications Controller On-Line Test and Internal Functional Test,* D99-3705* for discriptions of normal run indications and CE options available. The errors indicated by this test are listed in a symptom index included in the initial test section of D99-3705*. The customer cannot use the machine when these tests are in use.

- Internal Functional Test (IFT)
  These tests cannot be run while the customer is using the 3705 because they run under control of a Diagnostic Control Module (DCM). The DCM is loaded into the 3705 storage from the CPU by the OLT loader running under OLTEP or OLTSEP.
  Remote 3705's DCM and IFTs are loaded from the diskette at the remote site by way of the control panel. IFTs indicate errors with coded displays using Display A and Display B. These indications are listed in order by functional unit in symptom indexes in the "DCM/IFT" section of *IBM Maintenance Diagnostic Program IBM 3705 Communications Controller Internal Functional Test Symptom Indexes D99-3705E.*

- On-Line Test
  These tests are executed in the host CPU under control of an On-Line Test Executive Program. On-Line Terminal Tests (OLTT) and On-Line Line Tests (OLLT) may be run when the customer is still using the 3705. The Loader and Channel Adapter OLT's require *total* use of the 3705. See the Related Publications section on page II (preface) for the proper On-Line IBM maintenance document program guide.

Problem Isolation

After the error has been further defined for a particular functional unit, problem isolation begins. The first step in problem isolation is to analyze the error indications. The course of action is based on the urgency of the customer situation and what is available in the error indications. If one of the test programs has been chosen, refer to that section of this manual for information on analyzing the problem.

CAUTION

When replacing any logic card (FRU) in the 3705, the controller must first be disabled and powered down.

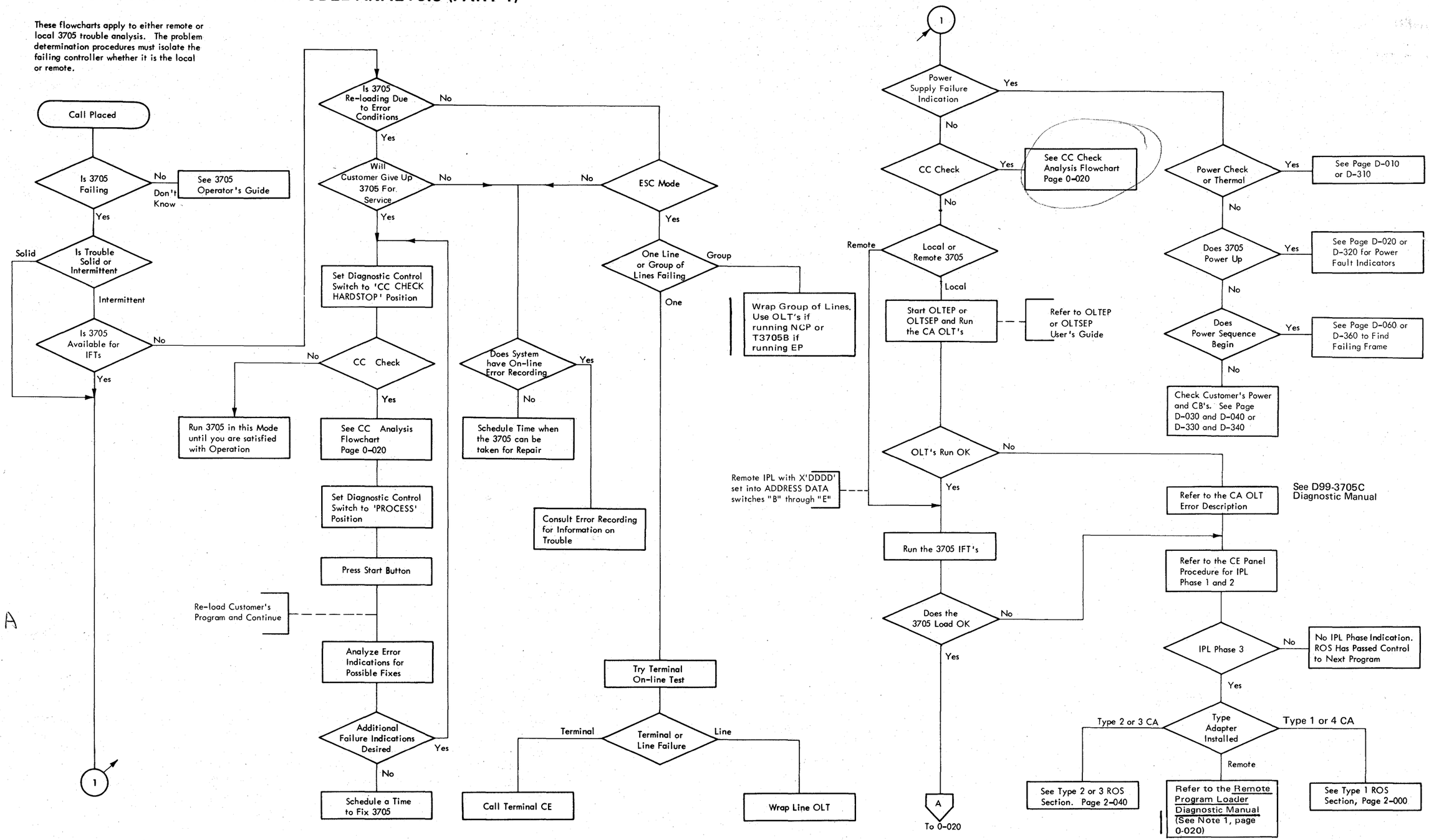
If cards are replaced on the Remote feature board with power on, the diskette may be damaged.

In addition, the host CPU must be in a Hard Stop condition (single cycle) when replacing the select-out bypass relay card in the channel adapter (type 1, 2, 3 or 4) at card location A4T4. Failure to observe this precaution causes channel checks at the CPU.

Prolonged touching of the pins on the CCU boards at 01A-B3 and 01A-B4 may result in CC checks.

DIAGNOSTIC APPROACH AND TROUBLE ANALYSIS (PART 1)

These flowcharts apply to either remote or local 3705 trouble analysis. The problem determination procedures must isolate the failing controller whether it is the local or remote.



D65A

DIAGNOSTIC APPROACH AND TROUBLE ANALYSIS (PART 2)

0400E

From 0-010

A

Bypass Initial Test Option — Yes

No

Initial Test Load Successful — No

Yes

CC Check — Yes → See CC Check Analysis Flowchart, See Page 0-020

No

Type Adapter Installed

Remote → Bypass it and Read LPG2 from Diskette

Type 2 or 3 CA → See Type 2 or 3 CA Loader Error Codes and Printouts in D99-3705D Diagnostic Manual

Type 1 or 4 CA → See Type 1 or 4 CA Loader Error Codes and Printouts in D99-3705D Diagnostic Manual

Initial Test Error — Yes

CC Check — Yes → See CC Check Analysis Flowchart Page 0-020

No → Local 3705—see the Diagnostic Manuals D99-3705D/E. Remote 3705—see the Remote Program Loader Diagnostic Manual, (See Note 1)

No

DCM Load Successful — No

Yes

DCM Error — Yes

CC Check — Yes → See CC Check Analysis Flowchart Page 0-020

No → Local 3705—see the Diagnostic Manuals D99-3705D/E. Remote 3705—see the Remote Program Loader Diagnostic Manual, (See Note 1)

No

IFT Loads — No

Yes

IFT Error — Yes

CC Check — Yes → See CC Check Analysis Flowchart Page 0-020

No → Local 3705—see the Diagnostic Manuals D99-3705D/E. Remote 3705—see the Remote Program Loader Diagnostic Manual, (See Note 1)

No

Have ALL IFT's Been Run — No → Load Next IFT

Yes

Run the Manual Intervention Routines

Local 3705—see the Diagnostic Manuals D99-3705D/E. Remote 3705—see the Remote Program Loader Diagnostic Manual, (See Note 1)

Rerun Customer's Program and See if Errors Continue

Note 1: Part Numbers For Remote Program Loader Diagnostic Manuals are:

1757889-Loaders, Initial Test, ROS
1757880-CCU Storage
1757882-Chan Adapters Type 1, 2, 3, 4
1757882-Type 1 Com. Scanner
1757883-Type 2 Com. Scanner
1757884-Type 3 Com. Scanner

Invalid Operation Codes

Operation Register															
Byte 0								Byte 1							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	X	X	X	0	X	X	X	0	0	X	0	0	0	0	0
0	X	X	X	0	X	X	X	0	1	0	1	0	0	0	0
0	X	X	X	0	X	X	X	0	1	1	X	0	0	0	0
1	0	1	1	1	0	0	1	0	1	0	0	0	0	0	0
1	0	1	1	1	0	1	X	0	1	0	0	0	0	0	0
1	0	1	1	1	1	X	X	0	1	0	0	0	0	0	0
1	0	1	1	1	X	X	X	0	1	0	0	0	0	0	1
1	0	1	1	1	X	X	X	0	1	0	0	0	0	1	X
1	0	1	1	1	X	X	X	0	1	1	0	0	0	X	X
1	0	1	1	1	X	X	X	0	X	X	1	X	X	X	X
1	0	1	1	1	X	X	X	0	X	X	0	1	0	X	X
1	0	1	1	1	X	X	X	0	X	X	0	X	1	X	X
1	0	1	1	1	X	X	X	0	1	X	0	X	1	X	X
1	0	1	1	1	X	X	X	0	1	X	0	1	X	X	X

3705-I

3705-II

X = Don't Care

CC CHECK ANALYSIS FLOWCHART

CC Check — Program Stop Hard Stop and Wait Light On

Perform Lamp Test

Prog L1 CC Check — Yes

No

Clock Check — Yes → Cycle Counter Error ABCD or T0-3 Counter Error CSB Clock Error See Page 6-981

No

SDR Error — Yes

See Description of Lights. Page 1-010

See Data Path Test Procedures, Page 1-170

See Control Panel Procedures, Page 1-120

No

B

To 0-030

In/Out Check — Yes → Display Op Reg. It Contains Input or Output Instruction Causing Error, see Page 1-020

No

Address Exception — Yes → Note: Contents SAR 1 Cycle (I1, I2, or I3). IAR for Level 1. Refer to: Instruction Decoding and Operations Charts to Further Define Error, see Page 6-150

No

Protect Check — Yes → To Define Failure, Note Contents of SAR, and Storage Key for that Area

No

Invalid Op — Yes → Display Op Reg. It contains Failing Instruction. Check for Invalid Op comparing with Invalid Op Code Chart. If Invalid, Display TAR then use that address minus 2 to do the Storage Control Panel Test. If Op Reg is valid, suspect Instruction Decode Failure on CDXXX

No → The In/Out check, address exception, and Invalid Op latches are reset if a re-IPL was forced (see 1-110). The CC check indicator is not reset.

Byte 0 Error — Yes → Storage Byte 0, SDR Byte X or 0, or Data Path failed (See Note 2)

No

Byte 1 Error — Yes → SDR Byte 1, Data Path, or Storage Failed (See Note 2)

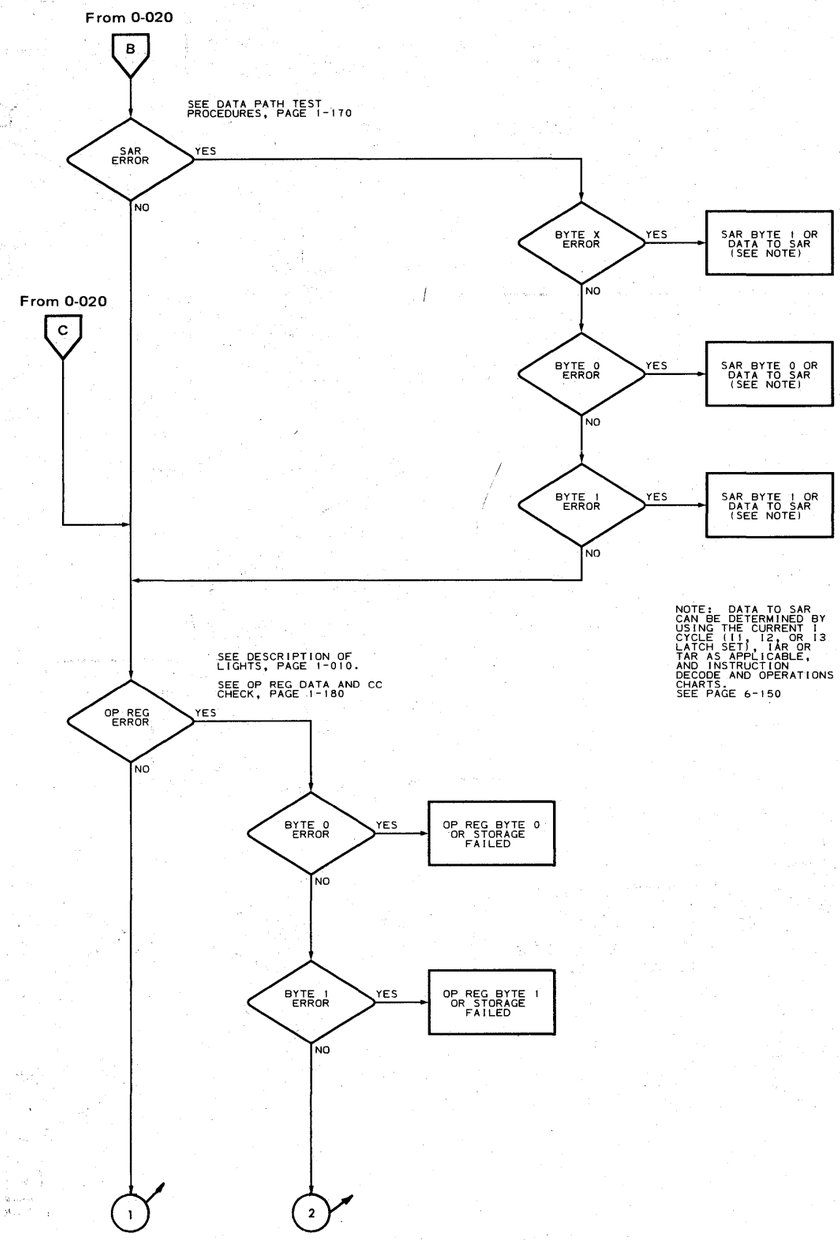
No

C

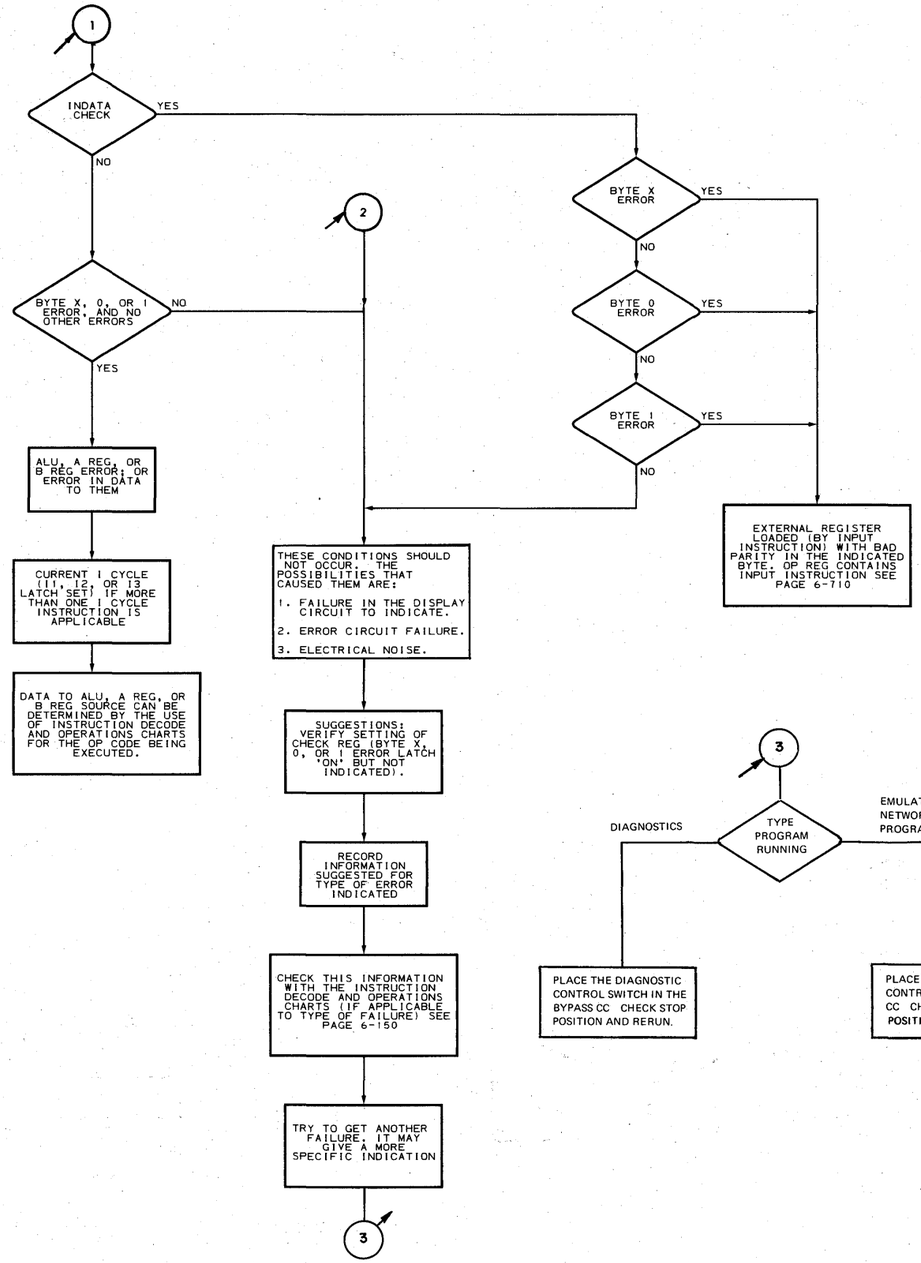
To 0-030

Note 2: Op Reg contains Op Code being executed. Data to SDR can be determined by the use of the Op Code, the current I cycle (I1, I2) or I3 Latch Set), and the instruction decode and operation charts. See Page 6-150

CC CHECK ANALYSIS FLOWCHART (PART 2)



D65A
F67A



INTRODUCTION TO THE 3705

The IBM 3705 Communications Controller is a transmission control unit with processing capabilities. Its functions are controlled by a program that resides in 3705 storage.

The 3705 is available in 64 models, based on the amount of storage and the maximum line-attachment capability. (The actual number of lines that the 3705 can support depends upon such factors as line speed and the throughput capability of the control program.)

All 64 models of the 3705 contain a central control unit, a control panel, at least 16K of storage for a 3705-I (32K for a 3705-II), a channel adapter, a communication scanner, and line interface bases and line sets. The communication scanner and the channel adapter are available in several versions.

Refer to the *Introduction to the IBM 3704 and 3705 Communications Controllers,* GA27-3051 for more introductory information.

CENTRAL CONTROL UNIT

The central control unit (CCU) contains the circuits and data flow paths necessary to execute the 3705 instruction set and to control 3705 storage and the attached adapters. The CCU operates under control of the 3705 control program.

CONTROL PANEL

The 3705 control panel contains the switches and lights necessary to control many 3705 functions manually. The control panel provides such functions as the ability to store and display information in storage and registers, the control and indication of power, the indication of status and error information, and operator and diagnostic controls.

STORAGE

Bridge Storage

3705-I contains a ferrite core storage unit. The amount of storage ranges from 16K bytes to 240K bytes in 32K increments. A storage protection mechanism in the CCU makes it possible to protect the contents of storage.

FET Storage

3705-II contains a FET (Field Effect Transistor) storage unit. The amount of storage ranges from 32K bytes to 256K bytes in 32K increments in the base frame of a 3705-II. For 3705-II Models J-L only, an additional 256K bytes of storage are available in increments of 64K bytes. This additional storage is located in the first expansion frame attached to the 3705.

This storage features automatic single-bit error correction, double-bit error detection, and a 1.0 or 0.9 microsecond cycle time depending on the model. A storage protection mechanism in the CCU makes it possible to protect the contents of storage.

TYPE 1 CHANNEL ADAPTER

The type 1 channel adapter (type 1 CA) provides attachment to an IBM System/360 or System/370 byte-multiplexer channel. The type 1 CA can handle only a relatively low volume of throughput and requires intervention from the 3705 control program for each data transfer. However, it is adequate for many small networks and is more economical than the type 2, type 3 CA, or type 4 CA.

TYPE 2 CHANNEL ADAPTER

The type 2 channel adapter (type 2 CA) provides attachment to an IBM System/360 or System/370 selector, byte-multiplexer, or block multiplexer channel. The type 2 CA transfers data by cycle steal, requires less program control than the type 1 CA, and can handle a larger volume of throughput.

TYPE 3 CHANNEL ADAPTER

The type 3 channel adapter (type 3 CA) is a type 2 CA modified by the addition of a two processor switch. The type 3 CA enables the 3705 to be attached to System/370 Model 158 and 168 tightly coupled multiprocessor systems as a symmetric shared I/O device and to single processors as an I/O device with alternate path capability.

TYPE 4 CHANNEL ADAPTER

The type 4 channel adapter (type 4 CA) is a modified type 1 CA that enables the control program to transfer across the channel interface multibyte bursts of up to 32 bytes in extended buffer mode with program intervention required only before and after each burst. A plugging option allows the bursts to be subdivided into groups of 4, 8, or 16 bytes with the type 4 CA disconnecting from the channel interface and reconnecting for each group to allow other channel activity to occur. The Type 4 CA can also transfer data by cycle steal under program control.

TYPE 1 COMMUNICATION SCANNER

The type 1 communication scanner provides the interface between the line interface bases and the central control unit. The scanner monitors the communications lines for service requests.

The type 1 scanner interrupts the 3705 for each bit that arrives or leaves over a communication line. The program assembles and disassembles characters for the scanner. The type 1 scanner can handle lines at speeds up to 7200 bps and is more economical than the type 2 or 3 scanner. The 3705 can handle only one type 1 scanner. Type 1 and 2 scanners or type 1 and type 3 cannot be mixed on a 3705.

TYPE 2 COMMUNICATION SCANNER

The type 2 communication scanner provides the interface between the line interface bases and the central control unit. The scanner monitors the communication line for service requests.

The type 2 communication scanner hardware assembles and disassembles characters. It interrupts the control program only when an entire character is ready for transfer to or from a line. The type 2 scanner can handle lines at speeds up to 50,000 bps. The 3705 can have up to four type 2 scanners. Type 1 1 and type 2 scanners cannot be mixed on a 3705.

TYPE 3 COMMUNICATION SCANNER

The type 3 communication scanner provides the interface between the line interface base and the central control unit. The scanner monitors the communication line for service requests.

The type 3 communication scanner hardware assembles and disassembles characters. The scanner cycle-steals data to and from buffers for each line. The scanner maintains an associated storage address and byte count, accumulates the CRC, and scans the data for line control characters. The scanner transfers data until certain control characters are detected and/or the byte count is reduced to zero, either of which requests control program interruption.

The type 3 communication scanner handles eight-bit code for SDLC or BSC (EBCDIC or USASCII) line operation. The 3705-I allows the type 3 scanner to be mixed with a type 2 scanner provided the type 3 scanner is installed in the first expansion frame. The 3705-II allows any mix of type 2 and type 3 scanners.

LINE INTERFACE BASES

Line interface bases (LIBs) attach the lines to the 3705. Nine LIB types are available to handle requirements for different types of line terminations. Depending upon the line termination, as many as 16 lines can be attached through one LIB.

LINE SETS

Lines are attached to LIBs through line sets. Depending upon the type of line termination, either one or two lines can be attached to one line set.

REMOTE PROGRAM LOADER

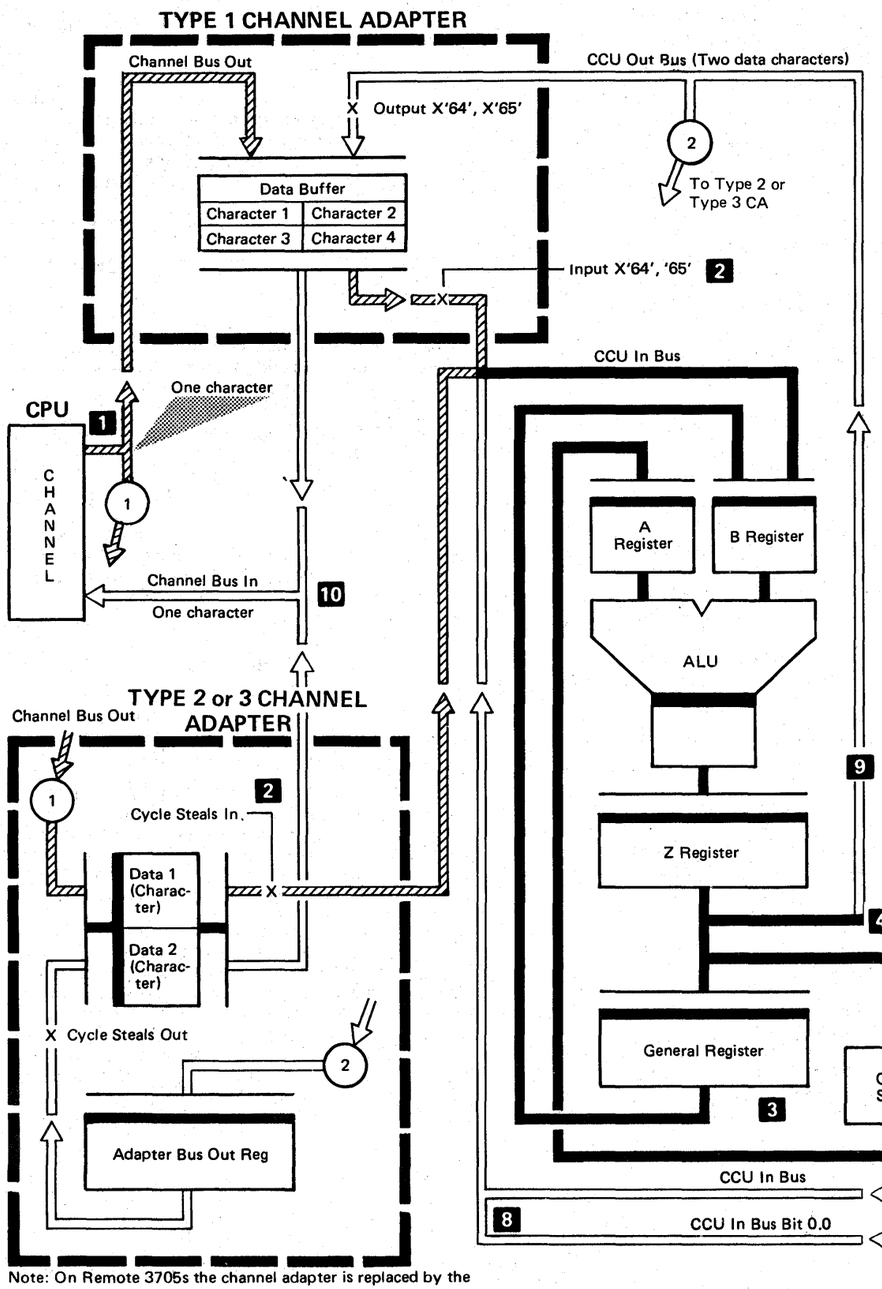
A 3705, used only as a remote communications controller, requires a remote program loader instead of a channel adapter. The remote program loader consists of an ROS bootstrap program, a diskette, a diskette drive, and a diskette controller. It is used to load a control program from a local 3704 or 3705 to the remote 3705 via an SDLC communication facility. Internal functional tests for the remote 3705 reside on the diskette.

In addition to the RPL feature, the base frame of a 3705-II can contain a channel adapter. With both features installed, internal function tests (IFTs) can be run using either the channel or the RPL feature.

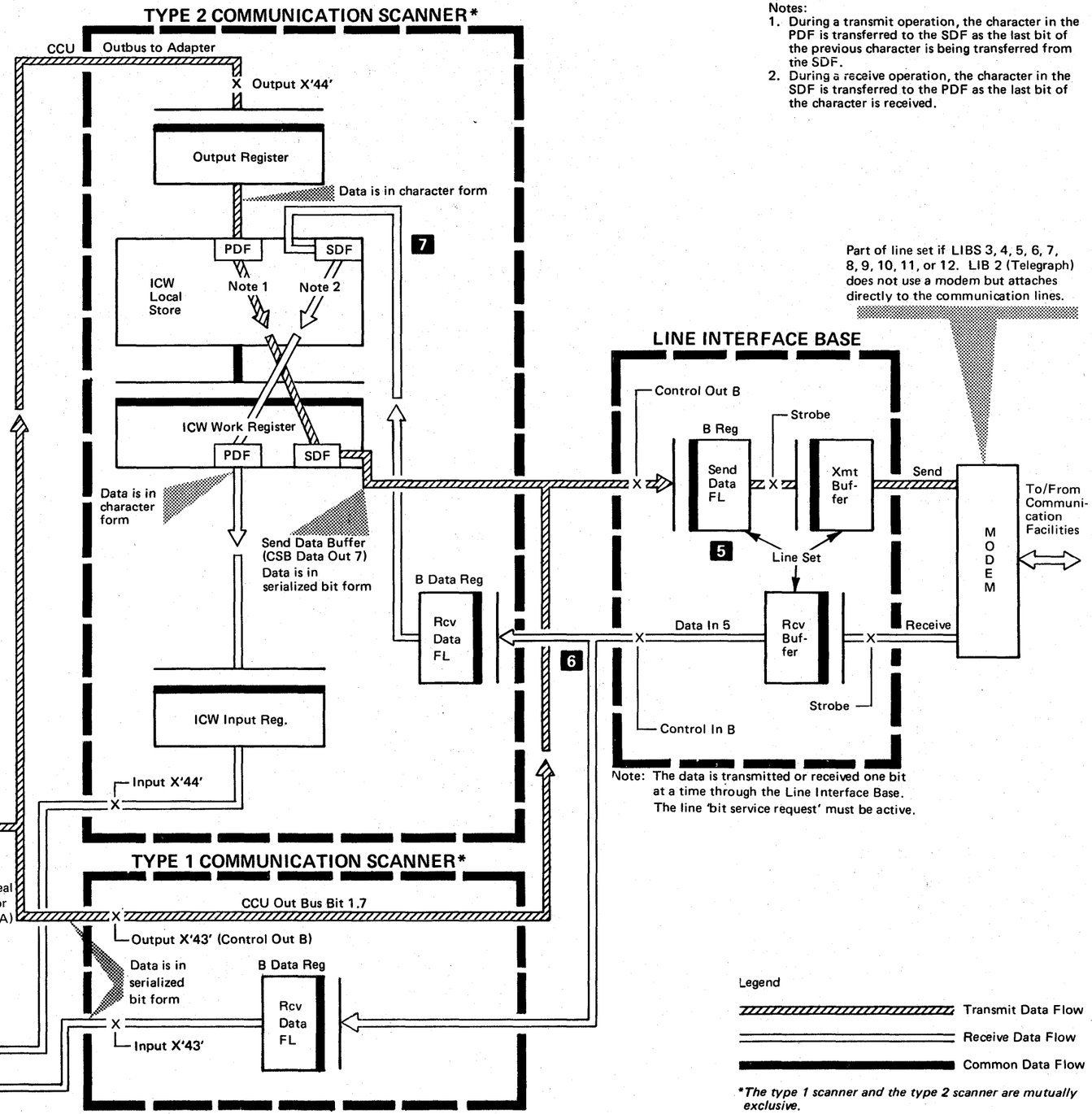
For a 3705 containing an RPL feature only (no channels), all IFTs are contained on the diskette.

3705-I DATA FLOW

Refer to page 0-070 for description



Note: On Remote 3705s the channel adapter is replaced by the Remote Program Loader. See 6-965 for the remote IPL sequence.



Notes:
1. During a transmit operation, the character in the PDF is transferred to the SDF as the last bit of the previous character is being transferred from the SDF.
2. During a receive operation, the character in the SDF is transferred to the PDF as the last bit of the character is received.

Note: The data is transmitted or received one bit at a time through the Line Interface Base. The line 'bit service request' must be active.

Legend
- Transmit Data Flow
- Receive Data Flow
- Common Data Flow

**The type 1 scanner and the type 2 scanner are mutually exclusive.*

3705-I DATA FLOW, (PART 2)

THESE DESCRIPTIONS REFER TO PAGE 0-060

HIGH LEVEL DATA FLOW FROM THE CPU TO THE COMMUNICATION FACILITIES (TRANSMIT)

1 The channel adapter issues a request for service to the channel to transfer data into its data buffer.

2
- Type 1 CA—An Input X'64' gates data characters 1 and 2 to the CCU In Bus. An Input X'65' gates data characters 3 and 4 to the CCU In Bus.
- Type 2 or 3 CA—A Cycle steal "in" operation gates the data 1 and data 2 characters to the CCU In Bus. See 9-430 for odd byte transfers.

3
- Type 1 CA—The two data characters are stored in the general register specified by the input instruction.
- Type 2 or 3 CA—The cycle steal operation gates the two data characters through CCU logic to storage.

In either case, the control program must place the data to be sent to the scanner in a general register in the proper format. The format depends on the type of scanner as follows:

- Type 1 scanner—The control program serializes the data character and places the bit to be transmitted in bit 1.7 ('send data') of the general register prior to each Output X'43' instruction. An Output X'43' instruction is required for each bit of the character.
- Type 2 scanner—The control program places the data character in byte 1 of the general register.

4
- Type 1 scanner—When the scanner addresses the line and 'bit service request' is active, an Output X'43' gates the data bit from bit 1.7 of the general register through CCU logic to the scanner.
- Type 2 scanner—An Output X'44' gates the data character from byte 1 of the general register through CCU logic to the 'output register'. The Output X'44' places the data character in bit positions 8-15 (parallel data field bits 0-7) of the ICW (interface control word) previously selected by the control program. Scanner hardware transfers the data character from the 'parallel data field' to the 'serial data field' where the character is serialized.

5 When the scanner addresses the line and the line's 'bit service request' is active, the serialized bit is buffered in the 'send data' latch of the line set's B register. The strobe, controlled by the transmit oscillator or the modem transmit clock, gates the bit to the transmit buffer where it is sent to the communication facility.

HIGH LEVEL DATA FLOW FROM THE COMMUNICATION FACILITIES TO THE CPU (RECEIVE)

6 The line set strobes the received bit into its receive buffer.
- Type 1 scanner—When the scanner addresses this line interface and 'bit service request' is active, the scanner gates the received data bit (data in 5) to the 'receive data' latch when neither Input X'42' or Input X'43' is decoded.
- Type 2 scanner—When the scanner addresses this line interface and 'bit service request' is active, the scanner gates the received data bit (data in 5) to the 'received data' latch.

7 The type 2 scanner assembles the received bits into a character in the ICW 'serial data field' for that line interface. The scanner then transfers the character to the ICW 'parallel data field'. When the CCU accepts the scanner character service interrupt, the scanner gates the character to the ICW 'input register'.

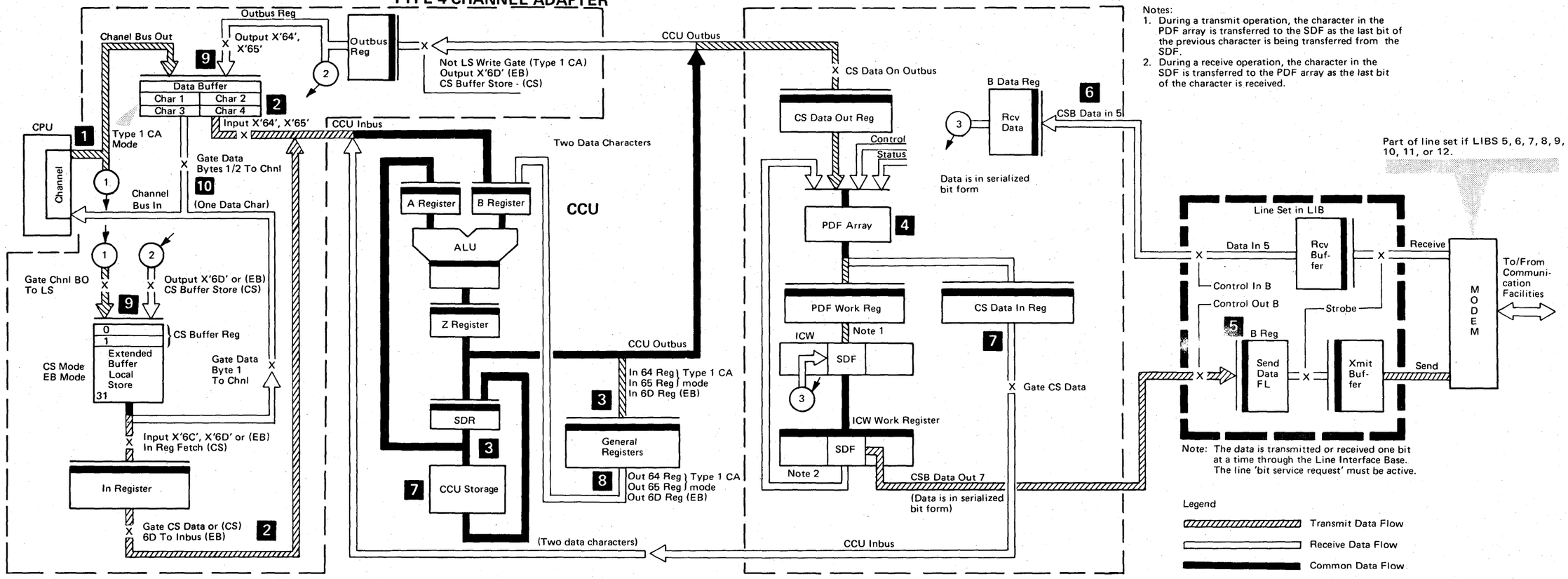
8
- Type 1 scanner—An Input X'43' gates the 'received data' bit to the general register specified by the input instruction. An Input X'43' is required for each bit received. The control program must assemble the character from the data bits received.
- Type 2 scanner—An Input X'44' gates the character from the ICW 'input' register to the general register specified by the input instruction.

In either case, the control program must prepare the data now in main storage for use by the channel adapter according to the type of channel adapter.
- Type 1 CA—The control program places the next two data characters to be transferred to the channel adapter in a general register.
- Type 2 or 3 CA—The control program places the received data characters into appropriate areas of main storage for subsequent cycle steal operations and sets up the CA to transfer the data to the channel.

9
- Type 1 CA—An Output X'64' gates data character 1 and 2 out of the general register, through CCU logic, onto the CCU Out Bus to the CA 'data buffers'. An Output X'65' gates data characters 3 and 4.
- Type 2 or 3 CA—A cycle steal "out" operation gates two data characters from main storage through CCU logic to the CCU Out Bus into the 'adapter bus out' register.

10 The channel adapter issues a service request to transfer data characters to the Channel Bus In. The data characters are transferred one character at a time.

3705-II DATA FLOW



Notes:
1. During a transmit operation, the character in the PDF array is transferred to the SDF as the last bit of the previous character is being transferred from the SDF.
2. During a receive operation, the character in the SDF is transferred to the PDF array as the last bit of the character is received.

HIGH LEVEL DATA FLOW FROM THE CPU TO THE COMMUNICATION FACILITIES (TRANSMIT)

1 After the type 4 CA responds to a Write type command, the CA issues a request for service to the channel to transfer data to the CA data buffer.

2
- Type 1 CA mode – An Input X'64' gates data characters 1 and 2 to the CCU In Bus. An Input X'65' gates data characters 3 and 4 to the CCU In Bus.
- EB mode – The data characters are loaded into the 32 character extended-buffer local store. The CA4 sets data characters 1 and 2 into the In register with an Input X'6C' - the remaining 30 with Input X'6D'. Input X'6D's gate two data characters to the CCU Inbus.
- CS mode – Two data characters are loaded in the two character CS buffer register in the EB local store. Cycle steal timings gate the two data characters to the In register then to the CCU In Bus.

3
- Type 1 CA mode – The two data characters are stored in the general register specified by the Input instruction.
- EB mode – Same as for type 1 CA mode.
- CS mode – The cycle steal operation gates the two data characters through CCU logic to storage.

The control program must place the data characters in the storage "data buffers" for the type 3 scanner.

4 A cycle steal operation transfers up to eight data characters from storage to the CS data out register and then to the PDF array. The scanner transfers one character from the PDF array to the SDF in the ICW where the character is serialized and sent one bit at a time to the line set. The other characters are transferred one at a time to the SDF as the SDF needs them. Cycle steal operations transfer two more data characters to the PDF array after two characters are sent to the SDF.

5 When the scanner addresses the line and the line's 'bit service request' is active, the serialized bit is buffered in the 'send data' latch of the line set's B register. The strobe, controlled by the transmit oscillator or the modem transmit clock, gates the bit to the transmit buffer where it is sent to the communication facility.

HIGH LEVEL DATA FLOW FROM THE COMMUNICATION FACILITIES TO THE CPU (RECEIVE)

6 The line set strobes the received bit into its receive buffer. When the scanner addresses this line interface and 'bit service request' is active, the scanner gates the received data bit (data in 5) to the 'received data' latch.

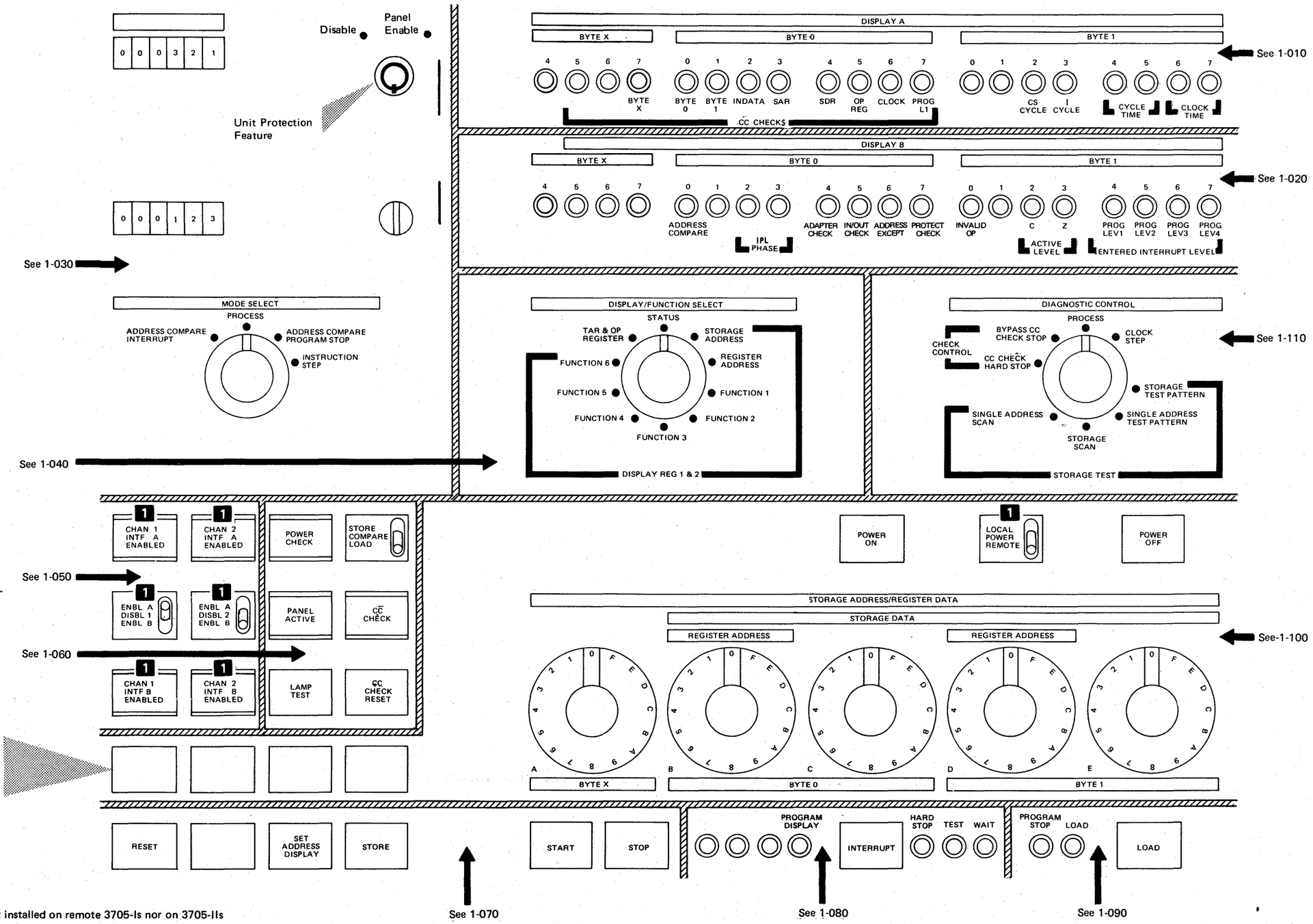
7 The type 3 scanner assembles the received bits into a character in the ICW 'serial data field' for that line interface. The scanner then transfers the character to the PDF array where up to eight data characters can be buffer. When two PDF buffers are loaded, a cycle steal operation transfers the two characters to the CS data in register and then through CCU logic to storage.

8 The control program must prepare the data now in main storage for use by the type 4 CA depending on the CA mode.
- Type 1 CA mode – the control program places the next two data characters to be transferred to the channel adapter in a general register.
- EB mode – Same as for type 1 CA mode.
- CS mode – The control program places the received data characters into appropriate areas of main storage for subsequent cycle-steal operations and sets up the CA to transfer the data to the channel.

9
- Type 1 CA mode – An Output X'64' gates data characters 1 and 2 from the general register, through CCU logic, onto the CCU Out Bus through the outbus register to the CA 'data buffers'. An Output X'65' gates data characters 3 and 4.
- EB mode – An Output X'6D' gates data characters 1 and 2 from the general register, through CCU logic, onto the CCU Out Bus to set the outbus register. The CA then loads the data into the EB local store where 32 data characters can be buffered.
- CS mode – A cycle-steal operation gates two data characters through CCU logic onto the CCU Out Bus, through the outbus register to the CS buffer register in the EB local store.

10 After the type 4 CA responds to a Read type command, the CA issues a service request to the channel to transfer data characters to the channel Bus In. The data characters are transferred one character at a time.

CONTROL PANEL LAYOUT



See E-040 for the layout of the enable-disable switches for all allowable combinations of channel adapters.

See E-040 for the layout of the IPL source switch for use with two type 4 CAs.

1 These switches are not installed on remote 3705-Is nor on 3705-IIs used only as Remotes.

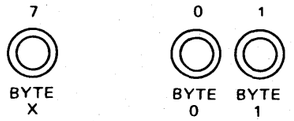
DISPLAY A

DISPLAY A CHECK LIGHTS

The DISPLAY/FUNCTION SELECT switch must be in STATUS to display check conditions in display A.

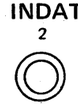
- Any of the following turn off the display A check lights if additional checks are not detected:
  a. Pressing the CC CHECK RESET push button.
  b. Pressing the RESET push button.
  c. Executing an Output X'77' instruction with bit 0.1 on in the general register designated by the R field of the instruction (when in bypass CC check stop mode).
  d. Executing an Output X'77' instruction from the control panel by storing a "1" in bit 0.1 of external register X'77'. (See 1-160.) (The 3705 must be in program stop mode.)

BYTE X, 0, and 1



- Turned on by the CCU (Central Control Unit) check register when a parity check occurs in the data path. If one or more of the BYTE lights are on, but no other CC CHECK light is on, the parity check is in the ALU (arithmetic logic unit), the A register, the B register, or the Z register.
  Note: If the IPL is not successfully completed, the local store registers can cause a parity check because they are not initialized.

INDATA



- Turned on when the CCU detects a parity error on the 'indata' bus.

The BYTE X, BYTE 0, and/or BYTE 1 CHECK light and the CC CHECK light also come on.

SAR

- Turned on when a SAR (storage address register) parity check occurs.

The BYTE X, BYTE 0, and/or BYTE 1 CHECK light and the CC CHECK light also come on.

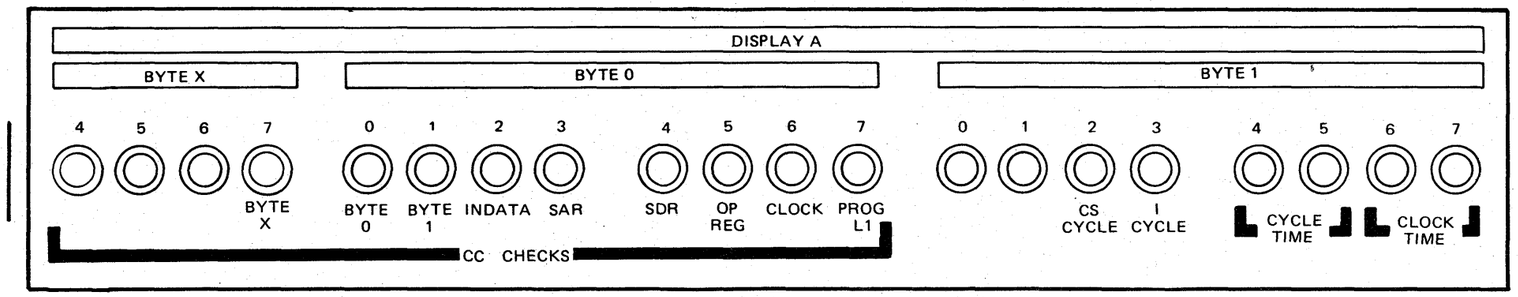
Note: A program error can cause a SAR byte X adapter check when a CA2, CA3, CA4 or a type 3 scanner is cycle-stealing . This failure can occur if the program sets up a cycle-steal address for that adapter to address a location larger than the storage size installed.

SDR

- Turned on when an SDR (storage data register) parity check occurs.

FET Storage Note: If storage is not initialized, an SDR check will likely occur. Storage may be initialized by (1) the initial test diagnostic, or (2) storage IFTs, or (3) manually performing a control panel "Storage Test Pattern" operation.

The BYTE 0 and/or BYTE 1 CHECK light and the CC CHECK light also come on.



OP REG

- Turned on when an OP (operation) register parity check occurs.

The BYTE 0 and/or BYTE 1 CHECK light and the CC CHECK light also come on.

CLOCK

- Turned on when a CCU or CS (communication scanner) support feature clock check occurs.

PROG L1

- Turned on when in program level 1, and one of the following occurs, causing a CC check.
  a. In/out check
  b. Address except check
  c. Protect check
  d. Invalid op check

If any one of these occurs in program level 1, it causes a CC check.

DISPLAY A STATUS LIGHTS

The DISPLAY/FUNCTION SELECT switch must be in STATUS to display status conditions in display A.

CS CYCLE

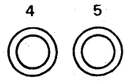
- Turned on at T0 of A time during a cycle steal cycle.
- Turned off after T3 of D time if no other cycle steal cycle is to follow immediately.

I CYCLE

- Turned on at T0 of A time during instruction execution cycles.
- Turned off after T3 of D time during instruction execution cycles if no other instruction cycle is to follow immediately.

If this light is off for any noticeable length of time, the HARD STOP, PROGRAM STOP, or WAIT light should be on for the same length of time.

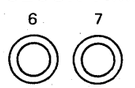
CYCLE TIME



- Displays a binary designation of the six basic cycle times. (See the chart below.)

During normal operation, the 3705 Models A-D cycle times are 200 nanoseconds in duration (250 ns for Models E-H and 225 ns for Models J-L) and are under the control of the machine oscillator. To observe the stepping of these lights, set the DIAGNOSTIC CONTROL switch to CLOCK STEP and repeatedly press the START pushbutton.

CLOCK TIME



- Displays a binary designation of the four basic clock times. (See the chart below.)

During normal operation the 3705-I clock times are 50 nanoseconds in duration (62.5 ns for 3705-II) and are under the control of the machine oscillator. To observe the stepping of these lights, set the DIAGNOSTIC CONTROL switch to CLOCK STEP and repeatedly press the START pushbutton.

3705-I only

Cycle Time	A				E*				B			
Clock Time	T0	T1	T2	T3	T0	T1	T2	T3	T0	T1	T2	T3
Bit 1.4 light	0				0				0			
Bit 1.5 light	0				0				1			
Bit 1.6 light	0	0	1	1	0	0	1	1	0	0	1	1
Bit 1.7 light	0	1	0	1	0	1	0	1	0	1	0	1

3705-I only

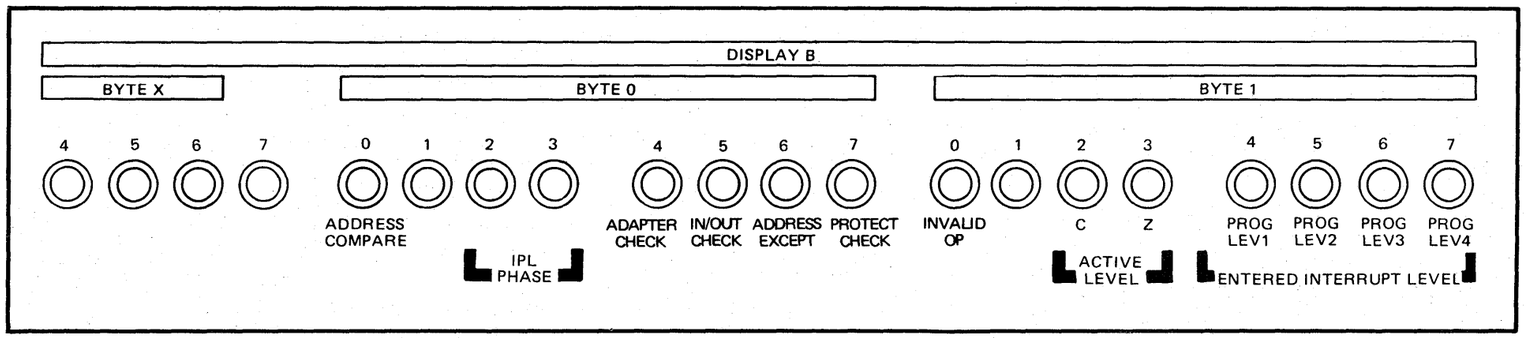
Cycle Time	F*				C				D			
Clock Time	T0	T1	T2	T3	T0	T1	T2	T3	T0	T1	T2	T3
Bit 1.4 light	0				1				1			
Bit 1.5 light	1				0				1			
Bit 1.6 light	0	0	1	1	0	0	1	1	0	0	1	1
Bit 1.7 light	0	1	0	1	0	1	0	1	0	1	0	1

Lights indicate the clock time that was just completed.

*Cycle times E and F are "dummy" times that are added to make a clock cycle equal to a 1.2 usec storage cycle (3705-I only). On the control panel, cycle times E and F appear as repetitions of cycles A and B respectively. A 1.2 usec storage cycle is necessary because of bridge storage characteristics.

DISPLAY B

Note: For control panel storage-address and storage-scan functions, DISPLAY B BYTE X should be ignored because storage operates only on halfwords.



DISPLAY B STATUS LIGHTS

The DISPLAY/FUNCTION SELECT switch must be in STATUS to display status conditions in display B.

ADDRESS COMPARE

0

ADDRESS COMPARE

- Turned on during instruction cycles when the address compare conditions described under LOAD/STORE ADDRESS COMPARE switch on page 1-060 are met.
- Turned off during the next cycle unless the PROGRAM STOP light is on.

IPL PHASE

2 3

IPL PHASE

- Displays a binary designation of the three IPL (Initial Program Load) phases.

  Both lights turn off at the end of IPL initialization when the program executes Output X'77' with bit 0.0 on. Reinitialization of the IPL also turns both lights off.

  Unless the DIAGNOSTIC CONTROL switch is in CLOCK STEP, IPL phases 1 and 2 should be hardly noticeable. If these lights stay on, it indicates a hardware failure.

A persistent IPL phase 3 indication is likely to be caused by either a hardware failure in read-only storage, a program failure, a CCU failure, or the CPU not loading the 3705.

The 'IPL phase' latches are on CU010.

IPL Phase	Display B Light 0.2	0.3
1	0	1
2	1	0
3	1	1

C and Z LEVEL

2 3

C Z

ACTIVE LEVEL

- Indicates the C and Z condition latches for the active program level.

ENTERED INTERRUPT LEVEL

4 5 6 7

PROG LEV1 PROG LEV2 PROG LEV3 PROG LEV4

ENTERED INTERRUPT LEVEL

- Indicates which of the five program levels are active or have interrupt requests entered. (No light indicates that level 5 is active if instructions are being executed.)
- Turned on when an interrupt occurs for that program level.
- Turned off when one of the following occurs:
  a. Exit instruction is executed at that level.
  b. 'Interrupt entered' latch for that level is reset by a machine reset.

If more than one of these lights are on, the highest priority program level indicated is the active level. Program level 5 is active when none of these lights are on and instructions are being executed.

DISPLAY B CHECK LIGHTS

The DISPLAY/FUNCTION SELECT switch must be in STATUS to display check conditions in display B.

ADAPTER CHECK

4

ADAPTER CHECK

- Turned on when any adapter (CA or CS) requests a program level 1 interrupt. See page 8-130 (type 1 CA), 9-200 (type 2 or 3 CA),H-380 (type 4 CA), A-220 (type 1 scanner), B-130 (type 2 scanner) or F-200 (type 3 scanner). An adapter check causes a level 1 interrupt. An adapter check while in program level 1 causes a CC check.
- Turned off when the interrupt request is reset.

IN/OUT CHECK

5

IN/OUT CHECK

- Turned on when the CCU detects one of the following.
  a. Invalid input or output instruction. (See page 6-151.)
  b. Parity check on the 'indata' bus during execution of an input instruction.
  c. Execution of an input or output instruction while in program level 5.

An in/out check causes a level 1 interrupt. An in/out check in program level 1 causes a CC check.

- Turned off by one of the following:
  a. Machine reset occurs.
  b. Executing Output X'77' with bit 1.5 on in the register designated by the R field of the instruction (when in bypass CC check stop mode).
  c. Executing Output X'77' from the control panel by displaying register X'77' and then storing a '1' in bit position 1.5. (See 1-160.) (The 3705 must be in program stop mode.)

ADDRESS EXCEPTION

6

ADDRESS EXCEPT

- Turned on when an address greater than the maximum installed storage address is addressed by instruction execution. An address exception causes a level 1 interrupt. An address exception in program level 1 causes a CC check.
- Turned off by either:
  a. A machine reset.
  b. Executing Output X'77' with bit 1.5 on in the register designated by the R field (when in bypass CC check stop mode).
  c. Executing an Output X'77' from the control panel by displaying register X'77' and then storing a '1' in bit position 1.5. (See 1-160.) (The 3705 must be in program stop mode.)

PROTECT CHECK

7

PROTECT CHECK

- Turned on when an attempt is made to change protected data. A protect check causes a level 1 interrupt. A protect check in program level 1 causes a CC check.
- Turned off by either:
  a. A machine reset.
  b. Executing an Output X'77' with bit 1.5 on in the register designated by the R field (when in bypass CC check stop mode).
  c. Executing Output X'77' from the control panel by displaying register X'77' and then storing a '1' in bit position 1.5. (See 1-160.) (The 3705 must be in program stop mode.)

INVALID OP

0

INVALID OP

- Turned on when the CCU detects an invalid OP code. An invalid op check causes a level 1 interrupt. An invalid op check in program level 1 causes a CC check.
- Turned off by any of the following:
  a. A machine reset.
  b. Executing Output X'77' with bit 1.5 on in the register designated by the R field (when in bypass CC check stop mode).
  c. Executing an Output X'77' from the control panel by displaying register X'77' and then storing a '1' in bit position 1.5. (See 1-160.) (The 3705 must be in program stop mode.)

CONTROL PANEL SWITCHES AND LIGHTS

CUSTOMER AND CE USAGE METERS

The 3705 has a customer usage meter (top meter) and a CE usage meter. The meters show the run time in hours and tenth hours. The CE Key switch position determines which meter is conditioned to run. The minimum usage meter run time is 400 msec. The following list tells when one of the meters should be running.

The 400 msec minimum time is reinitiated whan one of the following occur:

a. An instruction is executed at program level 1, 2, 4, or 5.

b. An instruction is executed at program level 3 after approximately 8ms have elapsed since the interval timer interrupt request was set.

c. An instruction is executed at program level 3 and an interrupt request other than the interval timer level 3 interrupt request is set.

d. A cycle steal cycle occurs.

Neither meter runs during:

a. Idle cycles.

b. IPL phases 1-3.

NOTE: The meter will run if the Emulation Program is loaded, the access method is not operating, and the DISPLAY/FUNCTION SELECT switch is set to function 1 or 6. Return the switch to the STATUS position to prevent unnecessary meter time.

MODE SELECT SWITCH

- Controls the 3705 mode of operation.

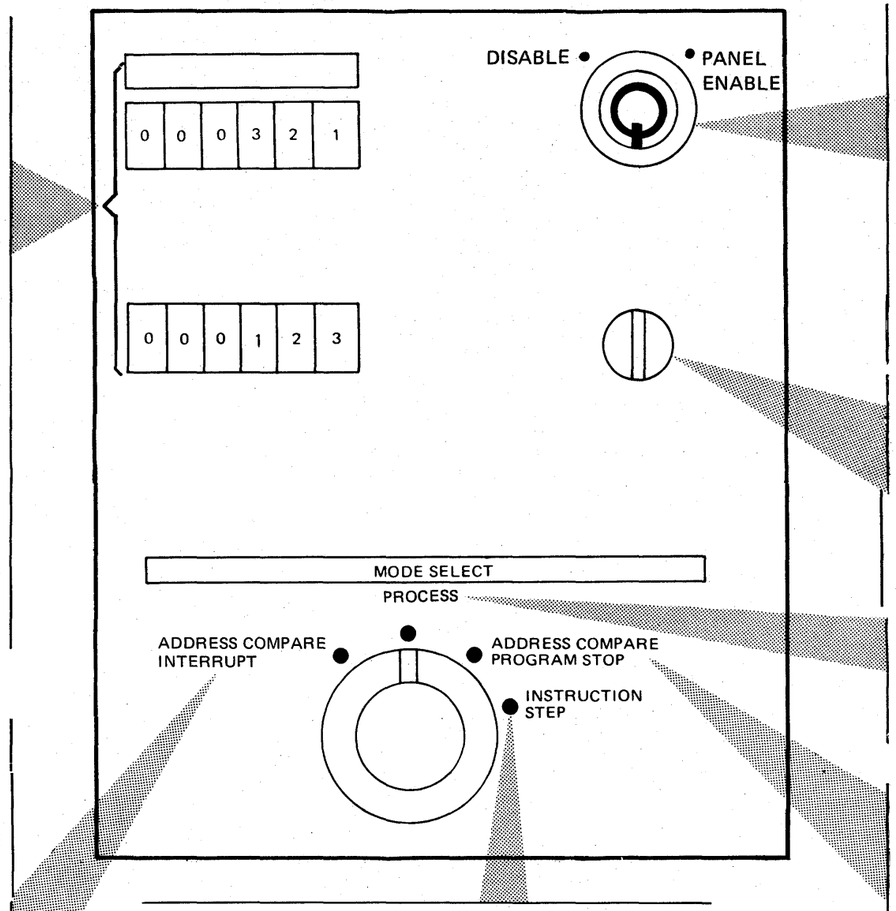
When the PANEL ACTIVE light is off, the 3705 runs as if the MODE SELECT switch and the DIAGNOSTIC CONTROL switch were in PROCESS, no matter what position the switches are in.

NOTE: If the panel is active and DIAGNOSTIC CONTROL switch is in any one of the STORAGE TEST positions or in the CLOCK STEP position, it overrides the MODE SELECT switch.

ADDRESS COMPARE INTERRUPT

- Causes the address compare L1 interrupt request to set at the end of the instruction if the address compare conditions described in *LOAD/STORE ADDRESS COMPARE SWITCH* on page 1-060 are met.

The 3705 operates normally except for the interrupt request when an address compare occurs.



INSTRUCTION STEP

- Causes the 3705 to execute one instruction each time the START push button is pressed and released.

The 'program stop' latch sets after the execution of the instruction. All interrupts except program L1 and PCI interrupts to higher program levels are inhibited until an 'exit' instruction is executed. After an 'exit' instruction is executed, the machine cycle priority controls determine which program level is active until the next 'exit' instruction, PCI to a higher level, or program level 1 interrupt.

Unless it is already set, the interval timer L3 interrupt request cannot be set when the MODE SELECT switch is in this position.

PANEL ENABLE/DISABLE SWITCH

- Available as the Unit Protection Feature.
- This allows the operator to disable/enable the operator panel switches (except power on/off) with a key controlled switch.

The disable position will prevent inadvertent or unauthorized use of the control panel.
When in the disable position the setting of the Storage Address/Register Data switches can be entered as input by the program.
When in the disable position and EP (emulation program) mode, the display lights can still be used.

CE KEY SWITCH

- Determines whether the CE or the customer usage meter is conditioned to run.

If the slot is vertical, the customer usage meter is conditioned to run.
If it is horizontal, the CE usage meter is conditioned to run.

PROCESS

- Allows the 3705 to run normally.

If the MODE SELECT switch is in any other position, the TEST light comes on.

ADDRESS COMPARE PROGRAM STOP

- Causes a program stop at the end of the instruction if the address compare conditions described in *LOAD/STORE ADDRESS COMPARE SWITCH* on page 1-060 are met.

With the switch in this position, an address compare detection does not set the address compare L1 interrupt request.

CAUTION

When the 'program stop' latch is set, cycle steal operations can cause adapter problems.

DISPLAY/FUNCTION SELECT SWITCH

- Used to display or store in storage or register; to display machine status or TAR and the Op register; and to make on line parameter changes.

In any position, except STATUS or TAR & OP REGISTER, displays A and B show the contents of display registers 1 and 2.

TAR & OP REGISTER

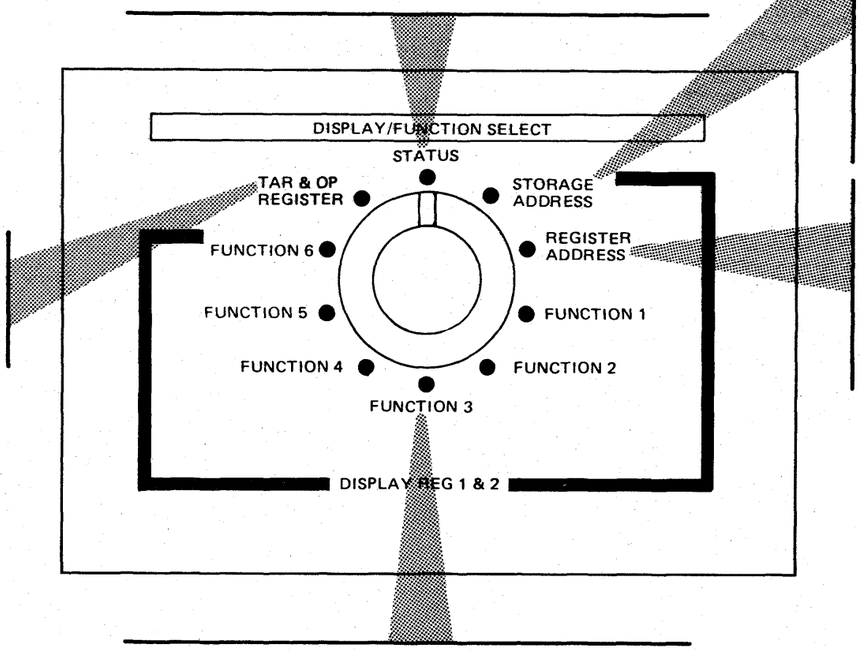
- Causes display A to show the contents of TAR (Temporary Address Register).
- Causes display B, bytes 0 and 1 to show the contents of the Op register. (Ignore byte X.)

Note: After a REGISTER ADDRESS, STORAGE ADDRESS, or STORAGE TEST function, the TAR & OP REGISTER position will no longer display the last previous TAR and OP code. Therefore, display and record these values before you do any other displaying if you will later need this information.

STATUS

- Causes displays A and B to show check and status information.

See page 1-010 and 1-020 for information about the check and status lights.



FUNCTIONS 1-6

The active program determines the function of the FUNCTION 1-6 positions.

STORAGE ADDRESS

- Used to select a storage address for displaying storage and for storing data in a storage location.

Pressing and releasing the SET ADDRESS/DISPLAY push button with the DISPLAY/FUNCTION SELECT switch in this position causes a display storage CS1 maintenance cycle. (See page 1-130, *Set Address and Display Storage Procedure.)*

Pressing and releasing the STORE push button with the DISPLAY/FUNCTION SELECT switch in this position causes a store storage CS1 maintenance cycle and a store storage CS2 maintenance cycle if the 3705 is in a stopped state. (See page 1-140, *Storing Data in Storage Locations.)*

REGISTER ADDRESS

- Used to select a register address for displaying a register and for storing data in a register.

Pressing and releasing the SET ADDRESS/DISPLAY push button causes a display register CS1 maintenance cycle. (See page 1-130, *Set Address and Display Register Procedure.)*

Pressing and releasing the STORE push button causes a store register CS1 maintenance cycle if the 3705 is in a stopped state.

CHANNEL 1 INTERFACE ENABLE/DISABLE SWITCH

CAUTION

When operating with a type 1 or type 4 CA in an NCP (PEP included) environment, do not attempt to disable a channel interface unless the 3705 network has been quiesced or a system reset has occurred. If this procedure is not followed, the NCP may, while disabled, attempt to send asynchronous status which inhibits the CA1 or 4 from becoming enabled again.

- Used to enable and disable channel interfaces 1A and 1B. Refer to 8-140 (Type 1 CA) and 9-080 (Type 2 CA) for a description of interfaces 1A and 1B. See G-040 for the type 3 CA switch positions and descriptions

If the DIAGNOSTIC CONTROL switch is in one of the four STORAGE TEST positions and the START push button is pressed, any interface that is enabled is disabled abruptly. The CHANNEL INTERFACE ENABLED light stays on until the CPU drops 'clock out', even though the interface is disabled. No channel can become enabled.

NOTE: Be sure the channel is disabled before performing storage test operations.

ENBL A

- Used to enable interface 1A.
- Interface 1B is disabled.

If interface 1B is installed and enabled and the switch is turned to this position, interface 1B is disabled when 'clock out' drops on interface 1B and command chaining stops. Channel 1A is enabled when these conditions are met.

DISBL 1

- Used to disable both interfaces 1A and 1B.

If one of the interfaces is enabled when you set the switch to DISBL 1, the interface is disabled when 'clock out' drops on that interface, and command chaining stops. Pressing the RESET push button with the switch in DISBL 1 also disables the interface.

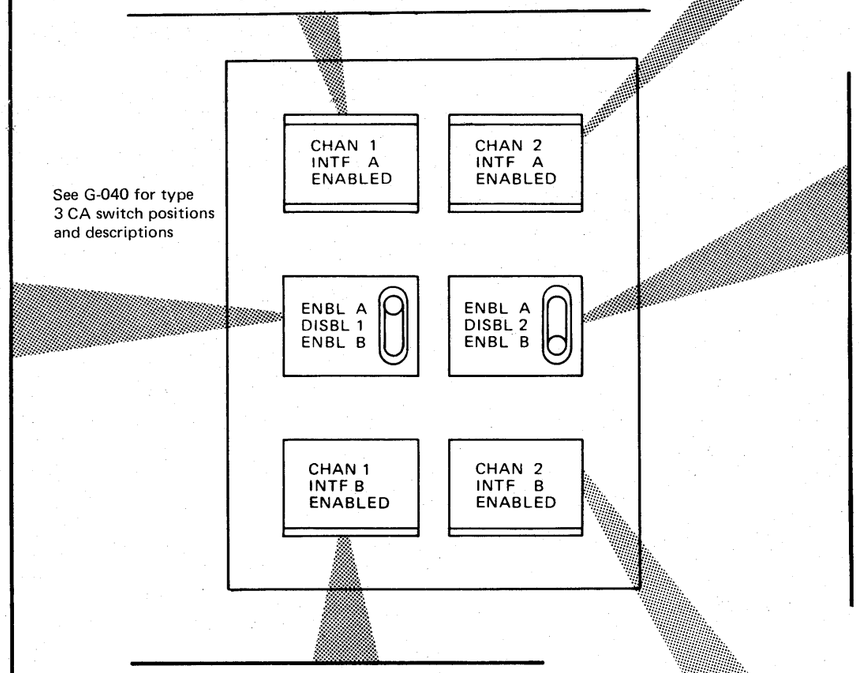
ENBL B

- Present only if the 3705 has the Two-Channel Switch feature for channel interface 1.
- Causes the same results for interface 1B that are described under *ENBL A.*

CHANNEL 1 INTERFACE A ENABLED LIGHT

- Turned on when interface 1A is enabled.
- Turned off when interface 1A is disabled.

NOTE: The light stays on when the 3705 is in hard stop, even though the adapter is disabled.



CHANNEL 1 INTERFACE B ENABLED LIGHT

- Turned on when interface 1B is enabled.
- Turned off when interface 1B is disabled.

NOTE: The light stays on when the 3705 is in hard stop, even though the adapter is disabled.

CHANNEL 2 INTERFACE A ENABLED LIGHT

- Turned on when interface 2A is enabled.
- Turned off when interface 2A is disabled.

NOTE: The light stays on when the 3705 is in hard stop, even though the adapter is disabled.

CHANNEL 2 INTERFACE ENABLE/DISABLE SWITCH

CAUTION

When operating with a type 1 or type 4 CA in an NCP (PEP included) environment, do not attempt to disable a channel interface unless the 3705 network has been quiesced or a system reset has occurred. If this procedure is not followed, the NCP may, while disabled, attempt to send asynchronous status which inhibits the CA1 or 4 from becoming enabled again.

This switch and the CHANNEL 2 INTERFACE A and B ENABLED lights are on the control panel only if a second channel adapter is installed in an expansion frame. The switch provides the same functions for the second channel adapter that the CHANNEL 1 INTERFACE ENABLE/DISABLE switch provides for channel interface 1.

CHANNEL 2 INTERFACE B ENABLED LIGHT

- Turned on when interface 2B is enabled.
- Turned off when interface 2B is disabled.

NOTE: The light stays on when the 3705 is in hard stop, even though the adapter is disabled.

POWER CHECK LIGHT

- Turned on when a power check occurs. (See D-010 for conditions that cause a power check.)
- Turned off by pressing the POWER-OFF push button on the control panel, if a thermal condition does not exist.
- Also turned on and off during a normal power-on sequence.
- Not turned on by LAMP TEST push button.

If the light is on because of a check condition, you cannot turn power on until you reset the check condition. If the power check resulted from an undervoltage sense, an overvoltage sense, or an overcurrent sense, reset the check by pressing the POWER OFF push button. If the check resulted from an open thermal switch, reset the check by pressing the THERMAL RESET push button located inside the covers of the 3705 (See D-010).

PANEL ACTIVE LIGHT

CAUTION

When the PANEL ACTIVE light is on, all the control panel switches and push buttons are active.

- Turned on when the MODE SELECT and DIAGNOSTIC CONTROL switches have been in the PROCESS position at least once since the last power-on sequence.

If the light is off and 3705 power is on, the 3705 operates as if the switches were in the PROCESS position. However, the push buttons, except for the power controls, have no effect.

LAMP TEST PUSH BUTTON

- Turns on all control panel lights, except POWER CHECK and the spares.

Pressing the LAMP TEST push button does not affect normal operation. The lights are much brighter than usual.

LOAD/STORE ADDRESS COMPARE SWITCH

STORE COMPARE

- Used to determine if data from a general register is stored in a specific byte of storage. (See *Store Address Compare* on 1-150.)

With the switch in this position, the addresses in the ADDRESS/DATA switches and in SAR are compared during each I2 and I3 cycle of a ST, STC, STH or STCT instruction. If the addresses are equal, an address compare occurs, and the ADDRESS COMPARE light in display B comes on if the DISPLAY/FUNCTION SELECT switch is in STATUS.

During I2 cycle for STH and ST instructions, bit 1.7 of the addresses is ignored in the comparison. (Both bytes are stored in the storage halfword.)

During I2 cycle for STC and STCT instructions and I3 cycle for ST instructions, bit 1.7 is included in the comparison. (Only one byte is stored in the addressed storage halfword location.)

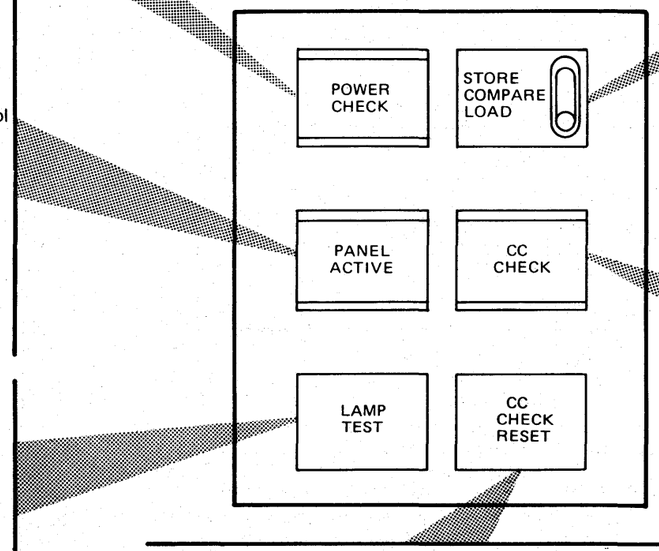
LOAD COMPARE

- Used to determine if an instruction loads data from a specific storage location into a general register. (See *Load Address Compare* page 1-150.)

The storage address in ADDRESS/DATA switches A-E is compared with SAR during each I1, I2 or I3 cycle of a load instruction. In this case a load instruction is any instruction except ST, STC, STH, or STCT. If the addresses are equal, an address compare occurs and the ADDRESS COMPARE light in display B comes on if the DISPLAY/FUNCTION SELECT switch is in STATUS.

During all I1 cycles, during I2 cycles for LH instructions, and during I3 cycles for the L instruction, bit 1.7 of the addresses is ignored in the address comparison. (Storage is addressed on a halfword basis.)

During I2 cycles for IC, ICT, and L instructions, bit 1.7 is included in the address comparison. (Storage is addressed on a byte basis.)



CC CHECK RESET PUSH BUTTON

- Resets the CCU check register and turns off the CC CHECK light, if the CC checks are no longer present.

This push button works only if the PANEL ACTIVE light is on.

CC CHECK LIGHT

- Turned on when a CC check is detected.
- Turned off by any of the following:
  a. Pressing the CC CHECK RESET push button if there are no more CC checks.
  b. Executing an Output X'77' with bit 0.1 on in the register designated by the R field of the instruction.
  c. Executing an Output X'77' from the control panel by displaying register X'77' and then storing a '1' in bit position 0.1. (See 1-160.)
  d. Pressing the RESET push button if there are no more CC checks.

Use Input X'7D' or turn the DISPLAY/FUNCTION SELECT switch to STATUS to display the specific CC check in display A.

CAUTION

MST cards are very sensitive and touching the pin side of certain cards can cause a CC check.

Note: The CC CHECK light is referred to as the CCU check indicator in logic.

RESET PUSH BUTTON

Pressing the RESET push button:

1. Sets the 'hard stop' and 'program stop' latches.
2. Sets odd parity in the local store register X'00'. (The data is not affected.)
3. Sets valid parity in the Op register and in SDR.
4. Sends a reset signal across the adapter interface to the 3705 adapters.
5. Disables the channel adapters (Type 2 or 3 CA). Logically disconnects the channel adapter from the interface by not allowing select out to be trapped (Type 1 or 4 CA).
6. Signals to the adapters that a *not initialized* state exists until the state ends as a result of IPL.
7. Resets the CCU error register.
8. Masks program levels 2-5 and adapter level 1.

NOTE: Output X'7F' must be executed to reset the mask bits.

9. Resets the 'program level entered' latches.
10. Resets all CCU interrupt requests.
11. Sets the 'test mode' latch.
12. Aborts IPL phase 2, if it is active.

SET ADDRESS/DISPLAY PUSH BUTTON

- Used to:
  a. Display the contents of a storage location, a CCU register, or an adapter external register in display B.
  b. Set the address of a storage location, CCU register, or adapter register for a store operation.

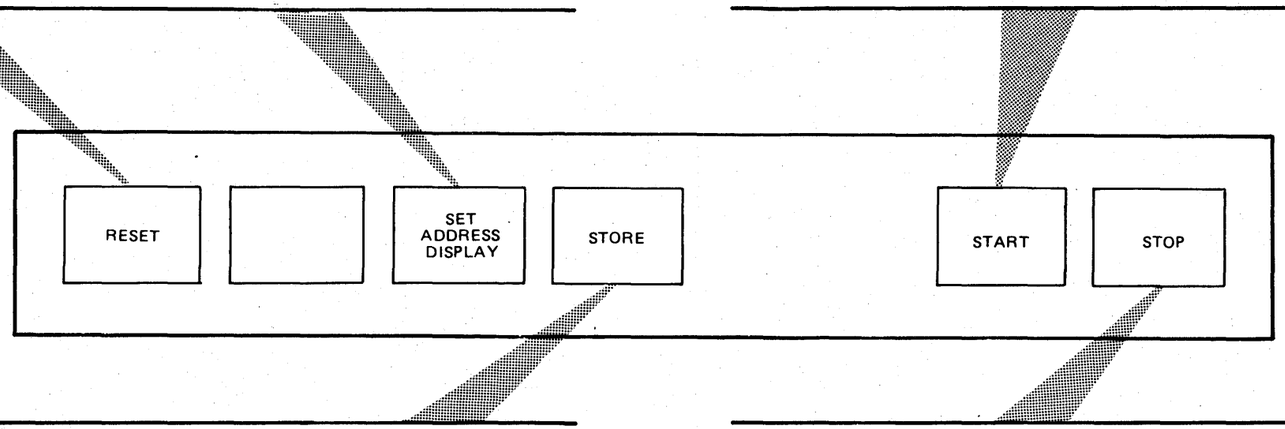
This push button functions only when the PANEL ACTIVE light is on and the DISPLAY/FUNCTION SELECT switch is in REGISTER ADDRESS or STORAGE ADDRESS. It does not function during IPL phase 1 or 2 or when the DIAGNOSTIC CONTROL switch is in one of the four STORAGE TEST positions and you have pressed the START push button (unless the 'hard stop' latch was set previously).

A dynamic display can be done provided a program display is not present.

START PUSH BUTTON

- Used to:
  a. Restart the program. Reset the 'hard stop' and 'program stop' latches if the DIAGNOSTIC CONTROL switch is in PROCESS, BYPASS CC CHECK STOP, or CC CHECK HARD STOP.
  b. Reset the 'hard stop' latch and start one of the four storage test functions.
  c. Start the clock step function to step the CCU clock when the DIAGNOSTIC CONTROL switch is in CLOCK STEP.

The START push button works only if the PANEL ACTIVE light is on. Pressing the START push button always causes a 1.2 usec CS1 start push button maintenance cycle.



STORE PUSH BUTTON

CAUTION

Be careful when you perform a store operation. the data stored may alter normal program and cycle steal operation. An adapter check can occur when channel cycle steals and store operations occur at the same time.

- Pressed and released to store data from the ADDRESS/DATA switches in a storage location or in a register.

The STORE push button works only when the PANEL ACTIVE and PROGRAM STOP lights are on and the DISPLAY/FUNCTION SELECT switch is in REGISTER ADDRESS or STORAGE ADDRESS. It does not work during IPL Phase 1 and 2 or when the DIAGNOSTIC CONTROL switch is in one of the four STORAGE TEST positions and you have pressed the START push button. The 'program stop' latch should be set before setting the address for the store operation.

STOP PUSH BUTTON

- Pressed to set the 'program stop' latch and stop program execution at the next instruction boundary.

This push button works only when the PANEL ACTIVE light is on. It does not stop adapter or maintenance cycle steal operations.

CAUTION

When the 'program stop' latch is set, cycle steal operations can cause adapter problems.

PROGRAM DISPLAY LIGHT

- Turned on when display register 1 or 2 contains program output. (CCU executed Output X'71' or X'72'.)
- Turned off when the CCU takes a maintenance cycle, or when you press and release the START push button if the 'hard stop' or 'program stop' latch is on.

If the light is on, turn the DISPLAY/FUNCTION SELECT switch to a position other than TAR & OP REGISTER or STATUS. This causes displays A and B to display the data that is in display registers 1 and 2.

HARD STOP LIGHT

- Turned on when the 'hard stop' latch sets.

The 'hard stop' latch sets when any of the following happen.

a. The CCU executes Output X'70' when in program level 1, 2, 3, or 4.

b. The control panel is active, the DIAGNOSTIC CONTROL switch is in STORAGE SCAN or STORAGE TEST PATTERN, and a CCU check occurs.

c. The control panel is active, the DIAGNOSTIC CONTROL switch is in CC CHECK HARD STOP, and a CC check occurs.

d. The control panel is active, and you press the RESET push button.

e. The 3705 is in IPL phase 2 or 3, and a CC check occurs (unless the 'bypass check stop' latch is set).

f. The control panel is active, and you turn the DIAGNOSTIC CONTROL switch to CLOCK STEP.

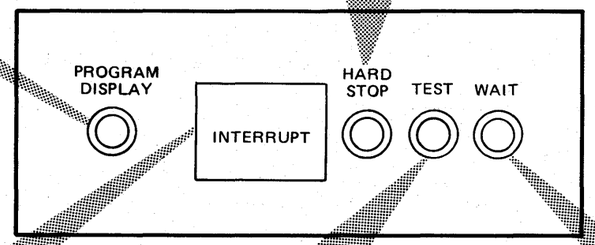
- Turned off when the 'hard stop' latch is reset.

The 'hard stop' latch is reset when any of the following happen.

a. A power-on reset occurs.

b. IPL phase 1 reset occurs.

c. The DIAGNOSTIC CONTROL switch is not in any of the four STORAGE TEST positions; none of the conditions that set the 'hard stop' latch are present; and you press the START push button. If the DIAGNOSTIC CONTROL switch is in CLOCK STEP and you press the START push button, the latch is reset during the start cycle, but not immediately.



INTERRUPT PUSH BUTTON

- Causes a program level 3 interrupt request.

Before you press the INTERRUPT push button, set the DISPLAY/FUNCTION SELECT switch and the ADDRESS/DATA switches according to the convention established by the program handling the request.

To reset the interrupt request, Output X'77' must be executed with bit 0.2 on in the register designated by the R field of the instruction. (The CE can execute this output by using the control panel. See 1-160.)

This push button works only when the PANEL ACTIVE light is on.

TEST LIGHT

- Turned on when any of the following occur.

a. The MODE SELECT switch is not in PROCESS.

b. The DIAGNOSTIC CONTROL switch is not in PROCESS.

c. The 'test mode' latch is set. (Note: The 'test mode' latch can be set by the control program via Output X'79' or by pressing the RESET push button.)

- Turned off when all of the following occur.

1. The MODE SELECT switch is in PROCESS,
2. The DIAGNOSTIC CONTROL switch is in PROCESS,
3. The 'test mode' latch is reset by the control program.

WAIT LIGHT

- Turned on when the CCU is in the wait state (running, but not taking instruction cycles or cycle steal cycles). Also comes on when the PROGRAM STOP or HARDSTOP light is on.
- Turned off when an interrupt occurs or the CCU takes a cycle steal cycle.

The usage meter does not run when the WAIT light is on. See 6-060 for an explanation of the wait state.

PROGRAM STOP LIGHT

- Turned on when the 'program stop' latch sets.

The 'program stop' latch sets when one of the following happens.

a. The control panel is active; the MODE SELECT switch is in ADDRESS COMPARE PROGRAM STOP; the LOAD/STORE ADDRESS COMPARE switch is in LOAD or STORE; and the contents of SAR match the address in ADDRESS/DATA switches A-E. (See 1-060.)

b. The panel is active; the MODE SELECT switch is in INSTRUCTION STEP; and the CCU reaches an instruction boundary.

c. The 'hard stop' latch sets.

d. The control panel is active, and you press the STOP push button.

e. The control panel is active, the DIAGNOSTIC CONTROL switch is in one of the STORAGE TEST positions, and you press the START push button.

- Turned off when the 'program stop' latch resets.

The 'program stop' latch is reset when one of the following happens.

a. A power-on reset occurs.

b. IPL phase 1 reset occurs.

c. The control panel is active, DIAGNOSTIC CONTROL switch is not any of the four STORAGE TEST positions, none of the conditions that set the 'program stop' latch are present, and you press the START push button. If the DIAGNOSTIC CONTROL switch is in CLOCK STEP, and you press the START push button, the latch is reset during the start cycle.

CAUTION

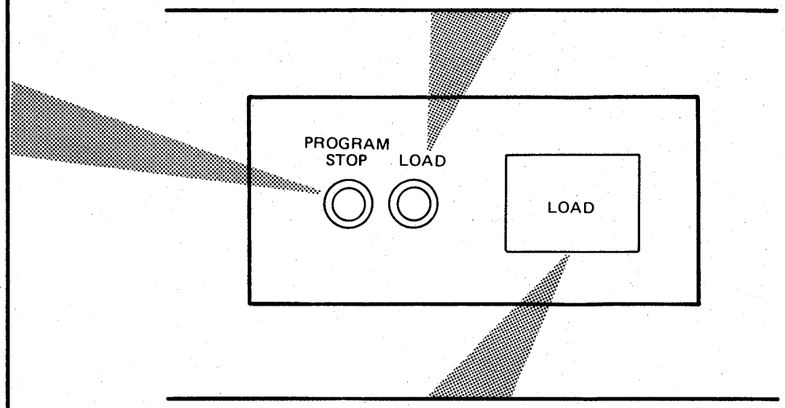
When the 'program stop' latch is set, cycle steal operations can cause adapter problems.

LOAD LIGHT

- Turned on when IPL starts.
- Turned off by either:

a. Executing Output X'79' with bit 1.1 on in the register designated by the R field of the instruction.

b. Executing Output X'79' from the control panel by displaying register X'79' and then storing a '1' in bit position 1.1. (See page 1-160.)



LOAD PUSH BUTTON

- Causes a machine reset and starts an IPL if the 'panel active' latch is set. (The PANEL ACTIVE light should be on.) See pages 6-960 to 6-964 for information on IPL.

POWER ON PUSH BUTTON

- Starts a power-on sequence if the LOCAL/REMOTE POWER switch is in LOCAL (Not affected by the Unit Protection Feature).

The POWER CHECK light comes on when you press the POWER ON push button and goes off when the power-on sequence is complete. The light stays on if a failure prevents completion of the power-on sequence.

An IPL starts at the end of a power-on sequence. The MODE SELECT and DIAGNOSTIC CONTROL switches must be in PROCESS so that the channel interface can be enabled during IPL.

REMOTE/LOCAL POWER SWITCH

- Determines whether the CPU or the 3705 controls dc power. (Not affected by the Unit Protection Feature).

LOCAL

- Dc power can be turned on and off only at the 3705 control panel. An emergency power off at any attached CPU turns off 3705 power.

REMOTE

- The CPU controls 3705 dc power.

Dc power comes on at the 3705 when power is turned on at any attached CPU. Dc power goes off at the 3705 when power is off at every attached CPU, when an emergency power off occurs at any attached CPU, or when you press the POWER OFF push button.

POWER OFF PUSH BUTTON

- Starts a power-off sequence. Resets any power check (except those caused by overheating) and turns off the POWER CHECK light (Not affected by the Unit Protection Feature).

This push button shuts down power with the REMOTE/LOCAL POWER switch in either position.

NOTE: Turn the CHANNEL INTERFACE ENABLE/DISABLE switch(es) to DISBL and wait for the INTERFACE ENABLED lights to go off before you press the POWER OFF push button. This prevents interference with the attached CPU.

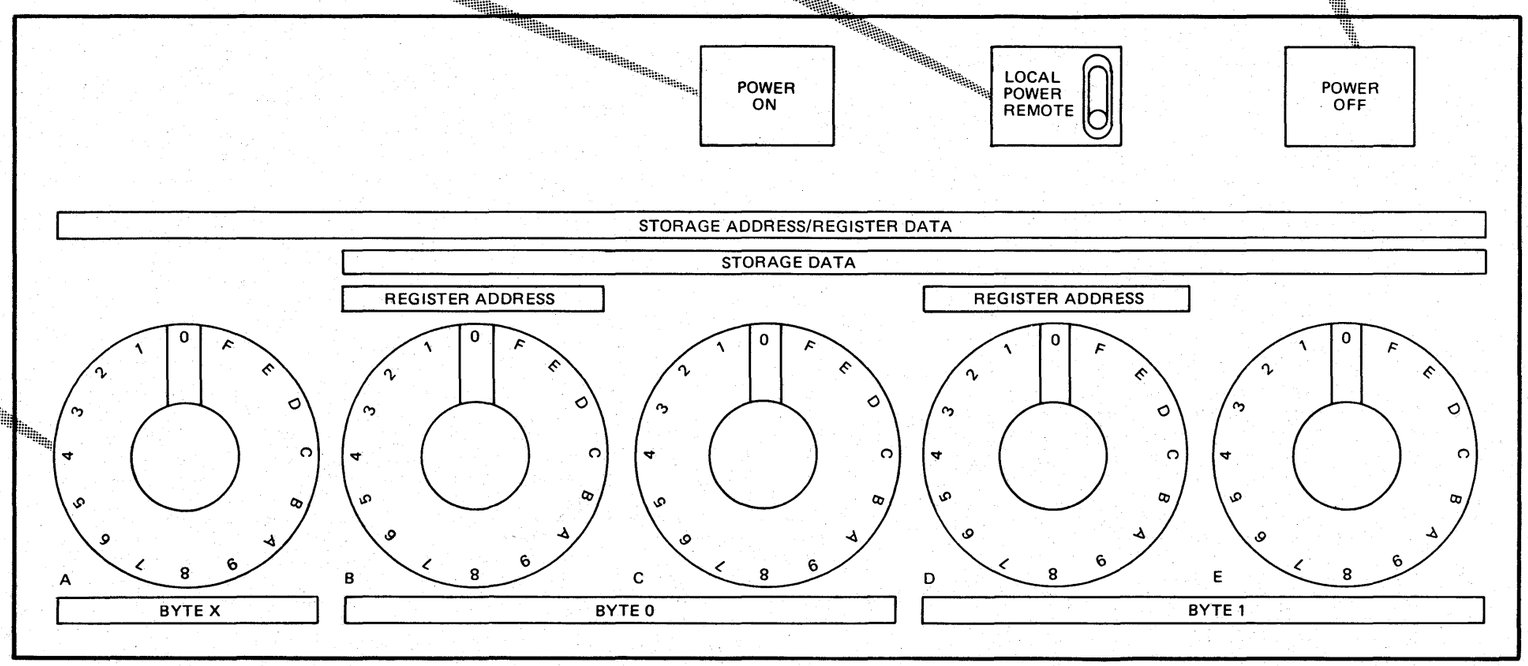
STORAGE ADDRESS/REGISTER DATA (ADDRESS/DATA) SWITCHES

- Sets addresses or enters data to test the 3705.

For storage addressing, you should use only positions 0-7 on switch A. For data entry, turning the switch to positions 8-F will also cause data to be entered 8=0, 9=1, A=2, B=3, C=4, D=5, E=6, F=7.

When Input X'71' is executed,the data in the switches is placed in the general register designated by the R field in the instruction.

NOTE: If Input X'71' is executed while you are turning the ADDRESS/DATA switches, the data loaded into the general register is unpredictable.



DIAGNOSTIC CONTROL SWITCH

- Used to perform diagnostic tests on the 3705.

If the PANEL ACTIVE light is off, the 3705 runs as if the switch were in PROCESS. The TEST light comes on if the switch is in any position other than PROCESS.

CAUTION

Before starting a clock step, storage scan, single address scan, storage test pattern, or single address test pattern procedure, perform a program shutdown procedure and disable the channel adapters. If you do not take this precaution, the channel adapters will be suddenly forced to the disabled state, and a system error may occur.

NOTE: Certain storage failures are not detected by performing storage scan, single address scan, single address test pattern, and storage test pattern procedures. Storage IFTs must be run to indicate these failures.

PROCESS

- Allows the 3705 to run normally.

BYPASS CC CHECK STOP

- Allows normal operation except the 'hard stop' latch does not set, and the CCU does not start an IPL sequence when a CC check occurs. Normal operation can be affected if the check alters the program in any way. See chart below.

The 'hard stop' latch does not set, but the appropriate CC check latch sets, and the CC CHECK light comes on.

CC CHECK HARD STOP

- Allows normal operation except that a CC check causes the 3705 to hard stop at the end of that cycle and prevents the latch 'mach ck set IPL'. (See Output X'79' page 6-930.) See chart below.

The 'hard stop' latch sets, the appropriate CCU check latch sets, and the CC CHECK light comes on; but the CCU does not start an IPL sequence.

CCU Action When a Check Condition Occurs

Diagnostic Control Switch Position	Hardstop		Process		Bypass Check Stop	
Error Occurred in Program Level	1	2, 3, 4, 5	1	2, 3, 4, 5	1	2, 3, 4, 5
Hardware Check						
ALU**	hardstops	hardstops	Note A	Note A	bypasses	bypasses
INDATA						
SAR						
SDR						
OP REG						
CLOCK						
Program Check						
ADAPTER	hardstops	bids level 1	Note A	bids level 1	bypasses	bids level 1
IN/OUT					bypasses	
ADDRESS EXCEPT					Note B	
PROTECT					Note B	
INVALID OP					bypasses	

NOTE A: A check sets the 'mach ck set IPL' latch and causes the 3705 to re-IPL. If another program check occurs before the 3705 exits level 1, the 3705 will hardstop.

NOTE B: This type error is not bypassed and program execution does not continue. However, the hardstop latch is not set and the hardstop light is not lit.

**The check condition is an ALU Check if the byte 0, byte 1, and/or byte X lights are on and the INDATA, SAR, SDR, OP REG, and CLOCK lights are off.

CLOCK STEP

(See also page 1-160)

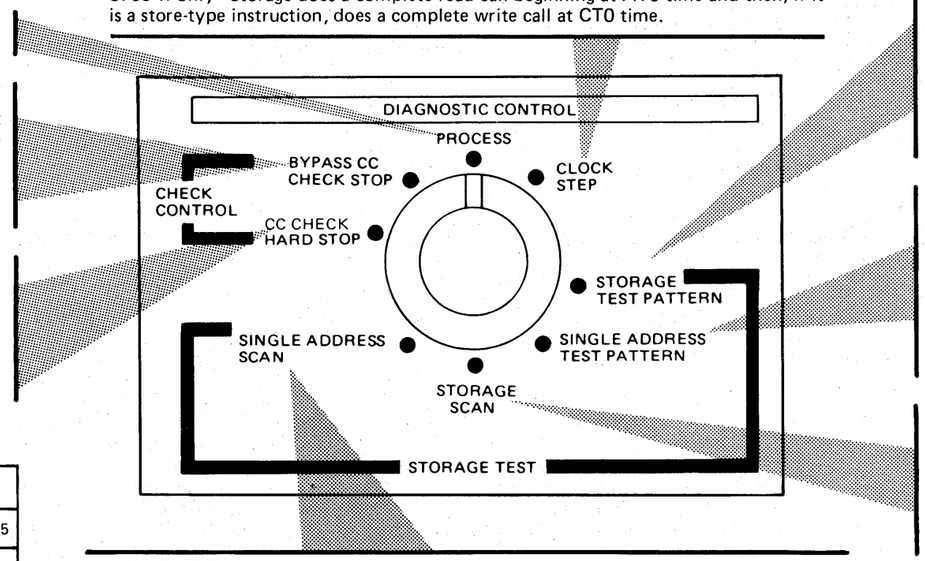
- Causes the CCU clock to be controlled by the START push button instead of the 3705 oscillator. (Refer to *Clock Step Procedure* on page 1-160.)

The 3705 stays in process mode until the START push button is pressed and an instruction boundary is reached. Pressing it the first time stops the 3705 in T0 of A time.

Each time you press and release the START push button, the CCU clock advances one T time. (This can be observed in the CLOCK TIME lights in display A. See chart A.) Press and release the START push button repeatedly to step the CCU clock through one "dummy" cycle (23 times for 3705-I; 15 times for 3705-II). Then step the CCU clock through one CS Start cycle (24 times for 3705-I; 16 times for 3705-II) to set up the following I cycle (observe the CS CYCLE light). Step the CCU clock through the instruction cycle(s). A CS Start cycle occurs before each of the following instruction's I cycle.

In CLOCK STEP the 3705 operates normally except:

1. Instead of the machine oscillator, the START push button steps the CCU clock.
2. The Z bus is gated to display register 1 at each AT3 time during maintenance cycles.
3. The Z bus is gated to display register 2 at every T3 time during maintenance cycles.
4. 3705-I only—Storage does a complete read call beginning at AT1 time and then waits to start a complete write call at FT1 time.
   3705-II only—Storage does a complete read call beginning at AT0 time and then, if it is a store-type instruction, does a complete write call at CT0 time.



SINGLE ADDRESS SCAN

- When the DIAGNOSTIC CONTROL switch is in this position, pressing and releasing the START push button causes a continuous scan of the storage location addressed by ADDRESS/DATA switches. (See *Single Address Scan* page 1-150.)

The 3705 stays in the process state until the START push button is pressed and released. This sets the 'program stop' latch and starts the operation. This operation continues regardless of error indications.

Chart A

3705-I only

Cycle Time	A				E*				B			
Clock Time	T0	T1	T2	T3	T0	T1	T2	T3	T0	T1	T2	T3
Bit 1.4 light	0				0				0			
Bit 1.5 light	0				0				1			
Bit 1.6 light	0	0	1	1	0	0	1	1	0	0	1	1
Bit 1.7 light	0	1	0	1	0	1	0	1	0	1	0	1

3705-I only

Cycle Time	F*				C				D			
Clock Time	T0	T1	T2	T3	T0	T1	T2	T3	T0	T1	T2	T3
Bit 1.4 light	0				1				1			
Bit 1.5 light	1				0				1			
Bit 1.6 light	0	0	1	1	0	0	1	1	0	0	1	1
Bit 1.7 light	0	1	0	1	0	1	0	1	0	1	0	1

Lights indicate the clock time that was just completed.

*Cycle times E and F are "dummy" times that are added to make a clock cycle equal to a 1.2 usec storage cycle (3705-I only). On the control panel, cycle times E and F appear as repetitions of cycles A and B respectively.

STORAGE TEST PATTERN

- Causes the continuous storing of test data from the ADDRESS/DATA switches in sequential storage locations. (See *Storing a Test Pattern in Storage* page 1-140.) After storing the pattern at a location, the CCU reads that location to check for good parity. The pattern is then stored at the next address. The operation stops when the switch is turned to another position or when the CCU detects an error.

The 3705 stays in the process state until the START push button is pressed and released. This sets the 'program stop' latch and starts the operation.

SINGLE ADDRESS TEST PATTERN

- When the DIAGNOSTIC CONTROL switch is in this position, pressing and releasing the START push button causes a continuous store and read operation for the storage location addressed by TAR. (See *Single Address Test Pattern Procedure* page 1-150.)

The 3705 stays in the process state until the START push button is pressed and released. This sets the 'program stop' latch and starts the operation. The operation stops when the switch is turned to another position. The operation continues regardless of error indications.

STORAGE SCAN

- When the Diagnostic Control switch is set in this position, pressing and releasing the START push button causes a storage scan operation.

The 3705 stays in the process state until the START push button is pressed and released. This sets the 'program stop' latch and starts the operation. The operation stops when the switch is turned to another position or when the CCU detects an error.

CONTROL PANEL PROCEDURES

POWER-ON PROCEDURE

1. Set the LOCAL/REMOTE POWER switch to LOCAL.
2. Press the POWER ON push button. The POWER CHECK light should turn on.
3. The POWER CHECK light turns off when the power on sequence ends. See D-050 for power sequence problems.

NOTE: The power-on procedure causes an IPL.

POWER-OFF PROCEDURE

1. Set the CHANNEL INTERFACE ENABLE/DISABLE switch (es) to DISBL.
2. Wait until all the CHANNEL INTERFACE ENABLED lights turn off.
3. Press the POWER OFF push button.

ACTIVATING THE CONTROL PANEL

1. Set the MODE SELECT and the DIAGNOSTIC CONTROL switches to PROCESS.
2. The 'panel active' latch is set and the PANEL ACTIVE light turns on.

ENABLING A CHANNEL INTERFACE

1. Set the CHANNEL INTERFACE ENABLE/DISABLE switch to ENBL A or ENBL B.
2. When the interface is enabled, the CHANNEL INTERFACE ENABLED light for that interface turns on.

NOTE: You may need to stop the CPU momentarily, to satisfy certain enable conditions if the CPU is very busy. Interface enable must also be conditioned by the 3705 program.

DISABLING A CHANNEL INTERFACE

1. Set the CHANNEL INTERFACE ENABLE/DISABLE switch to DISBL.
2. When the channel interface is disabled and the 'clock out' line from the CPU is inactive, the CHANNEL INTERFACE ENABLED light for that interface turns off.

NOTE: You may need to stop the CPU momentarily to satisfy certain disable conditions if the CPU is very busy.

IPL PROCEDURE

See "Enabling Type 4 CA NSC Address", page H-000, for the procedure for selecting the CA4 that is to accept the IPL if dual type 4 CAs are installed.

1. Activate the panel.
2. Press the LOAD push button.
3. The LOAD light turns on when IPL starts.

RESETTING THE 3705

CAUTION

Disable the channels interfaces before pressing the RESET push button.

1. Press the RESET push button.
2. This resets all the 3705 hardware. (See *RESET Push Button* page 1-070.)
3. Press the LOAD push button to start an IPL sequence.

RESETTING A CC CHECK

1. Press the CC CHECK RESET push button.
2. If no more checks are detected, the CC CHECK light turns off.

REQUESTING A PROGRAM LEVEL 3 INTERRUPT

1. Set the DISPLAY/FUNCTION SELECT switch and the ADDRESS/DATA switches according to the convention established by the program handling the request.
2. Press and release the INTERRUPT push button.

DISPLAYING 3705 STATUS

1. Set the DISPLAY/FUNCTION SELECT switch to STATUS.
2. The lights in display A and display B show check and status information as indicated by their labeling.

DISPLAYING TAR AND THE OP REGISTER

1. Set the DISPLAY/FUNCTION SELECT switch to TAR & OP REGISTER.
2. Display A shows the address in TAR. Display B bytes 0 and 1 show the contents of the Op register. Byte X of display B contains all 0s.

NOTE: After a register address, storage address or storage test function, the TAR & OP REGISTER position of the DISPLAY/FUNCTION SELECT switch will no longer display the last previous TAR and OP code.

SET ADDRESS AND DISPLAY REGISTER PROCEDURE

(See page 6-052 for flowchart.)

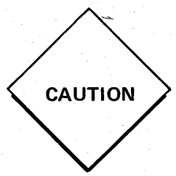
You can display most addressable registers using this procedure with the program running without affecting normal program operation. However, when you address certain registers, control functions occur and affect program operation. Refer to pages 8-060 (type 1 CA), 9-100 (type 2 and 3 CA) and H-040 (type 4 CA) for information on these registers. Inputs X'41', X'42', and X'43' are invalid when executed from the panel unless the scanner is stopped (type 1 scanner only).

1. Set ADDRESS/DATA switches B and D to the address of an input register. (See 6-151 for the register addresses.)
2. Set the DISPLAY/FUNCTION SELECT switch to REGISTER ADDRESS.
3. Press and release the SET ADDRESS/DISPLAY push button.
   - A display register CS1 maintenance cycle is taken on the next instruction boundary.
   - Display A bits 0.0 - 0.3 and bits 1.0 - 1.3 display the contents of ADDRESS/DATA switches B and D. All other bits in display A are 0.
   - The input register address in the ADDRESS/DATA switches is also put in the Op register.
   - Display B shows the register contents. If the register address is unassigned, all zero's, or a CA register address that cannot be displayed, display B shows all 0s. (See 8-060 (type 1 CA), 9-100 (type 2 and 3 CA) and H-040 (type 4 CA) for a description of undisplayable CA registers.) The In/Out Check L1 interrupt request is not set.
   - If the PROGRAM STOP light is on, the register address is also placed in TAR. It can then be used as the register address in a subsequent store register operation.

NOTE: If the PROGRAM DISPLAY light is on, this operation will not work with the program running.

STORING DATA IN A REGISTER

(See page 6-054 for flowchart.)



Be careful when using the STORE push button. The data stored may affect normal program and cycle steal operation and destroy program data.

1. If the PROGRAM STOP light is not on, press the STOP push button.
2. Perform a set address and display register operation to set in the Op register the address of the output register in which you desire to store data. Leave the DISPLAY/FUNCTION SELECT switch at REGISTER ADDRESS.
3. Set the data in ADDRESS/DATA switches A-E.
4. Press and release the STORE push button.
   - The PROGRAM DISPLAY light turns off, if it was on.
   - Display A shows the contents of TAR. (TAR and the Op register contain the address entered in the set address and display register operation.)
   - The data in ADDRESS/DATA switches A-E is stored in the output register addressed by the Op register, and is displayed in display B.
   - If the register address in the Op register is unassigned, the store operation has no effect. The In/Out Check L1 interrupt request is not set.

SET ADDRESS AND DISPLAY STORAGE PROCEDURE

(See page 6-056 for flowchart.)

NOTE: Displaying storage locations using this procedure does not affect normal program or cycle steal operation.

1. Set ADDRESS/DATA switches A-E to the storage address.
2. Set the DISPLAY/FUNCTION SELECT switch to STORAGE ADDRESS.
3. Press and release the SET ADDRESS/DISPLAY push button.
   - A display storage CS1 maintenance cycle is taken on the next instruction boundary.
   - The contents of ADDRESS/DATA switches A-E are placed in SAR and in display A.
   - Display B bytes 0 and 1 shows the contents of the addressed storage halfword location. Because control panel storage-address and storage-scan functions operate only on halfwords, display B byte X should be ignored. If the storage address is invalid for the machine configuration, display B shows all 0's. The Address Exception L1 interrupt request does not set.
   - If the PROGRAM STOP light is on, the storage address is also placed in TAR. It can then be used as the initial address in a store storage operation.

NOTE: If the PROGRAM DISPLAY light is on, this operation will not work with the program running.

STORING DATA IN STORAGE LOCATIONS

(See page 6-057 for flowchart.)

NOTE: Certain storage failures are not detected by this procedure. Storage IFTS must be executed to indicate these failures.

1. If the PROGRAM STOP light is not on, press the STOP push button.
2. Perform a set address and display storage operation to set the storage address in TAR. (See page 1-130.) Leave the DISPLAY/FUNCTION SELECT switch at STORAGE ADDRESS.
3. Set the data in ADDRESS/DATA switches B-E.
4. Press and release the STORE push button.
   - The PROGRAM DISPLAY light turns off, if it was on.
   - The contents of ADDRESS/DATA switches B-E are stored at the location addressed by TAR.
   - TAR is incremented to address the next halfword storage location. Display A shows this new address.
   - Display B bytes 0 and 1 displays the data from the addressed storage location. Because control panel storage-address and storage-scan functions operate only on halfwords, display B byte X should be completely ignored. If the storage address is too large for the machine configuration, display B shows all 0's. The Address Exception L1 interrupt request is not set.
5. Press the STORE push button each time you want to store data from ADDRESS/DATA switches B-E in the next sequential storage location.

STORING A TEST PATTERN IN STORAGE

(See page 6-060 for flowchart.)

CAUTION

Disable the channel interfaces before you start this procedure.

If a test pattern that is an invalid Op is stored, pressing the START push button will cause an invalid Op CC check.

NOTE: Certain storage failures are not detected by this procedure. Storage IFTS must be executed to indicate these failures.

1. Set the test pattern data in ADDRESS/DATA switches B-E.
2. Set the DIAGNOSTIC CONTROL switch to STORAGE TEST PATTERN.
3. Set the DISPLAY/FUNCTION SELECT switch to any position except TAR and OP Register or STATUS.
4. Press the START push button.
   - The PROGRAM STOP light turns on.
   - The data in ADDRESS/DATA switches B-E is stored in the storage location addressed by TAR.
   - Display A displays the address in TAR. TAR is then incremented to address the next storage halfword location.
   - Display B bytes 0 and 1 displays the data from the storage location. Because control panel storage-address and storage-scan functions operate only on halfwords, display B byte X should be completely ignored.
   - The stored data is checked for parity. A parity check causes the appropriate CC CHECK light to turn on. The 3705 stops. To continue the operation: (1) press the CC CHECK RESET push button, and (2) press the START push button. The operation continues until the CCU detects an error.
5. To end the operation, set the DIAGNOSTIC CONTROL switch to another position.

NOTE: Because an asynchronous stop occurs when the switch is turned, an indata check may occur. Ignore the check, and press the CC CHECK RESET push button.

STORAGE SCAN

(See page 6-063 for flowchart.)

CAUTION

Disable the channel interfaces before you start this procedure.

NOTE: Certain storage failures are not detected by this procedure. Storage IFTs must be executed to indicate these failures.

1. Set the DIAGNOSTIC CONTROL switch to STORAGE SCAN.
2. Press the START push button.
   - The PROGRAM STOP light turns on.
   - The storage location addressed by TAR is scanned first.
   - Each CS1 cycle increments the address in TAR by two and puts the new address in display A (unless the DISPLAY/FUNCTION SELECT switch is in STATUS.)
   - Display B bytes 0 and 1 shows the last thing set in the Op register if the DISPLAY/FUNCTION SELECT switch is in TAR & OP REGISTER. (The Op register is not changed during this operation.) If the switch is not in the TAR and OP Register or STATUS position, display B shows the contents of the storage location addressed by SAR. Because control panel storage-address and storage-scan functions operate only on halfwords, display B byte X should be completely ignored.
   - If the address in TAR is invalid for the machine configuration, the operation proceeds, but display B shows all 0s. This continues until the addressing starts again at the first address.
   - A parity check causes the appropriate check light to turn on. The 3705 stops. The address in display A is two greater than the address that caused the parity check. To continue the operation: (1) press the CC CHECK RESET push button, and (2) press the START push botton. The operation continues until the CCU detects an error.
3. To end the operation, set the DIAGNOSTIC CONTROL switch to another position.

NOTE: Because an asynchronous stop occurs when the switch is turned, an indata check may occur. Ignore the check and press the CC CHECK RESET push button.

SINGLE ADDRESS TEST PATTERN PROCEDURE

(See page 6-064 for flowchart.)

CAUTION Disable the channel interfaces before you start this procedure.

NOTE: Certain storage failures are not detected by this procedure. Storage IFTs must be run to indicate these failures.

1. Set the address of the storage location in TAR, using the procedure in *Set Address and Display Storage Procedure* or in *Single Address Scan.*
2. Set the test pattern in ADDRESS/DATA switches B-E.
3. Set the DIAGNOSTIC CONTROL switch to SINGLE ADDRESS TEST PATTERN.
4. Set the DISPLAY/FUNCTION SELECT switch to any position except TAR and OP Register or STATUS.
5. Press the START push button.
   - The PROGRAM STOP light turns on.
   - The data in ADDRESS/DATA switches B-E is stored in the storage location addressed by TAR.
   - Display A shows the address in TAR. TAR is not incremented.
   - Display B bytes 0 and 1 shows the data stored in the storage location. The data is checked for parity. If the storage address is too large for the machine configuration, display B shows all 0's. Because control panel storage-address and storage-scan functions operate only on halfwords, display B byte X should be ignored.
   - A parity check does not cause the machine to stop, but the appropriate CC CHECK light does turn on.
6. To end the operation, set the DIAGNOSTIC CONTROL switch to another position.

   NOTE: Because an asynchronous stop occurs when the switch is turned, an indata check may occur. Ignore the check and press the CC CHECK RESET push button.

SINGLE ADDRESS SCAN (See page 6-067 for flowchart.)

1. Set ADDRESS/DATA switches A-E to the address of the storage location that you want to scan.
2. Set the DIAGNOSTIC CONTROL switch to SINGLE ADDRESS SCAN.
3. Set the DISPLAY/FUNCTION SELECT switch to any position except TAR and OP Register or STATUS.
4. Press the START push button.
   - During each CS1 cycle, display A displays the address in the ADDRESS/DATA switches.
   - Display B bytes 0 and 1 shows the data in the addressed location. Because control panel storage-address and storage-scan functions operate only on halfwords, display B byte X should be ignored.
   - The storage address is not incremented.
   - The scanning does not stop if a parity check occurs, but the appropriate CC CHECK light does turn on.
5. The ADDRESS/DATA switches can be rotated to continuously display the contents of the storage locations.
6. To end the operation, set the DIAGNOSTIC CONTROL switch to another position.

   NOTE: Because an asynchronous stop occurs when the switch is turned, an indata check may occur. Ignore the check and press the CC CHECK RESET push button.

STORE ADDRESS COMPARE

1. Set the LOAD/STORE ADDRESS COMPARE switch to STORE.
2. Set ADDRESS/DATA switches A-E to the storage address.

   NOTE: To determine if a 'store character' (STC) or 'store character and count' (STCT) instruction stores data from a general register in a storage byte, set the ADDRESS/DATA switches to the address of that byte.
   To determine if a 'store' (ST) or 'store halfword' (STH) stores byte 0 and byte 1 of a general register in a storage halfword, set the ADDRESS/DATA switches to the address of either byte.

   - During I2 and I3 cycles, the storage address in the ADDRESS/DATA switches is compared with the contents of SAR. If the addresses are equal, and the instruction being executed is a ST, STC, STH, or STCT instruction, the ADDRESS COMPARE light in display B turns on, if the DISPLAY/FUNCTION SELECT switch is in STATUS. Bit 1.7 is included in the address comparison only if the instruction is a *byte* instruction.
3. To cause a program stop to occur when the address compare occurs, set the MODE SELECT switch to ADDRESS COMPARE PROGRAM STOP. Pressing and releasing the START push button resets the 'program stop' latch and restarts the program.
4. To cause the address compare L1 interrupt request to set when the address compare occurs, set the MODE SELECT switch to ADDRESS COMPARE INTERRUPT.

LOAD ADDRESS COMPARE

1. Set the LOAD/STORE ADDRESS COMPARE switch to LOAD.
2. Set ADDRESS/DATA switches A-E to the storage address.

   NOTE: To determine if an instruction at a specific address is ever executed, the address set in the ADDRESS/DATA switches can be either the address of byte 0 or byte 1 of the instruction.
   To determine if a storage byte is ever loaded into a general register, set the ADDRESS/DATA switches to the address of that byte.
   To determine if a storage halfword is ever loaded into byte 0 and 1 of a general register, set the ADDRESS/DATA switches to the address of either byte 0 or byte 1 of the storage location.

   - During I1, I2, and I3 cycles, the storage address in the ADDRESS/DATA switches is compared with the contents of SAR. If the addresses are equal, and the instruction is any instruction other than ST, STC, STH, or STCT, the ADDRESS COMPARE light in display B turns on if the DISPLAY/FUNCTION SELECT switch is in STATUS. Bit 1.7 is included in the address comparison only if the instruction is a *byte* instruction.
   - If the MODE SELECT switch is at ADDRESS COMPARE PROGRAM STOP when the addresses are equal, pressing and releasing the START push button resets the 'program stop' latch and restarts the program.
3. To cause a program stop to occur when the address compare occurs, set the MODE SELECT switch to ADDRESS COMPARE PROGRAM STOP.
4. To cause the address compare L1 interrupt request to set when the address compare occurs, set the MODE SELECT switch to ADDRESS COMPARE INTERRUPT.

LAMP TEST

NOTE: Pressing the LAMP TEST push button does not affect normal 3705 operation.

1. Press the LAMP TEST push button.
2. All the control panel lights, except the POWER CHECK light and the spares, turn on.

CLOCK STEP PROCEDURE

Disable the channel interfaces before you start this procedure.

1. Set the DIAGNOSTIC CONTROL switch to CLOCK STEP.
2. Press the START push button.
   - The 3705 stops in T0 of A time.
   - The START push button, instead of the 3705 oscillator, provides pulses to drive the CCU clock.
   - If the DISPLAY/FUNCTION SELECT switch is in STATUS, displays A and B show check and status information. If the switch is in TAR & OP REGISTER, display A shows the contents of TAR and display B shows the contents of the Op register. If the switch is in any other position, the contents of the Z bus are gated to display register 1 at each AT3 time and to display register 2 at every T2 time during maintenance cycles.

NOTE: 3705-I only — Clock cycles E and F are not indicated on the control panel; they appear as repetitions of cycles A and B, respectively.

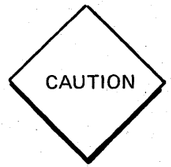
Rules for observing clock-step operations.

- The first instruction executed in clock-step mode is preceded by an idle cycle (CS indicator off, I indicator off).
- A CS1 start-push button cycle (CS indicator on, I indicator off) is taken before the start of each instruction.
- The I cycle being executed can be determined by observing the Display A status indicators 1.3-1.7. By counting the number of transistions thru IA T0 since the last cycle steal cycle, the I-cycle number is known (be sure to watch the I indicator — ignore the interspersed idle cycles).
- Additional idle cycles may be interspersed depending on the machine model and instruction.

In CLOCK STEP the 3705 operates normally except:

1. Instead of the machine oscillator, the START push button steps the CCU clock.
2. The Z bus is gated to display register 1 at each AT3 time during maintenance cycles.
3. The Z bus is gated to display register 2 at every T3 time during maintenance cycles.
4. 3705-I only—Storage does a complete read call beginning at AT1 time and then waits to start a complete write call at FT1 time.
   3705-II only—Storage dows a complete read call beginning at AT0 time and then, if it is a store-type instruction, does a complete write call at CT0 time.

INSTRUCTION STEP PROCEDURE



During instruction step mode,cycle steal operations could cause adapter problems.

1. Set the MODE SELECT switch to INSTRUCTION STEP.
   - The PROGRAM STOP light turns on.
2. Press and release the START push button to continue with the next instruction.
   - The 3705 executes one instruction, and the PROGRAM STOP light turns off.
3. Each time you press and release the START push button, the 3705 executes one instruction.

NOTE: The CCU handles cycle steal requests normally during this procedure. All interrupts, except program level 1 interrupts and interrupts to higher program levels, are inhibited until the program executes an 'exit' instruction.

EXECUTING AN INPUT OR OUTPUT INSTRUCTION FROM THE CONTROL PANEL

Input instructions can be executed from the control panel by displaying the corresponding external register. See *Set Address and Display Register Procedure* on page 1-130.

Output instructions can be executed from the control panel by displaying the corresponding external register and then storing the desired bits in the register. (The 3705 must be in program stop mode.) See *Storing Data in a Register* on page 1-130.

Example: The CC CHECK lights in displays A and B can be turned off by executing an Output X'77' instruction with bit 0.1 on the general register designated by the R field of the instruction. The lights can also be turned off by storing a "1" in bit 0.1 of external register X'77'.

The bits stored in an external register from the control panel have the same hardware function as when they are set on by a program. Therefore, many hardware functions can be checked by simulating input and output instructions from the control panel.

SETTING UP AND EXECUTING AN INSTRUCTION

Disable the channel interfaces before starting this procedure.

NOTE: This procedure is an example of one method to set up and execute an instruction.

1. Press the STOP push button.
2. Use the *Set Address and Display Storage Procedure* (page 1-130) to set the storage address that you want to store the instruction in.
3. Use the steps in *Storing Data in a Storage Location* (page 1-140) to store the desired instruction in the storage location.
4. In the next storage location, store a 'branch' instruction to cause a branch back to the preceding storage location.
5. Use the *Set Address and Display Register Procedure* (page 1-130) to set the IAR (register 0) for the program level that you are in. (The current program level can be determined from the status lights in display B.)
6. Follow the steps in *Storage Data in a Register* (page 1-130) to store the address of the storage location from step 3 in the IAR.
7. If you want to step through the instructions:
   a. Turn the MODE SELECT switch to INSTRUCTION STEP.
   b. Press and release the START push button. The CCU executes one instruction. The 3705 stops, and the PROGRAM STOP light turns on.
   c. Press and release the START push button to execute the next instruction. Each time you press the START push button, the CCU executes one instruction.

NOTE: If the CCU is in level 1 (as it is immediately after ROS is loaded), program execution in levels 2, 3, 4, or 5 requires the following previous steps: (1) reset level 1 requests—Output X'77', (2) unmask appropriate interrupt level—Output X'7F', (3) generate an appropriate interrupt request, and (4) EXIT.

CONTROL PANEL TEST OF CCU DATA PATH

PART 1. BASIC CONTROL AND DATA FLOW

This section tests the part of the data path in the CCU necessary to load ROS and those controls that may be necessary to analyze a failure detected by the ROS test.

LAMP TEST

1. Press LAMP TEST.—All panel lights, except POWER CHECK and the spares, should light.
2. Swap any failing lights with lights in working positions to verify that the lights are bad.
3. Replace the lights found to be defective.
4. If the lights tested are good, swap the driver cards located at 01A-B4U2 and 01A-B4U3. Refer to D-210 and ALDs AP009 to AP015 for details.

PANEL ACTIVE (REQUIRED FOR FURTHER PANEL TESTING)

The following conditions should activate the PANEL ACTIVE light:

a. DIAGNOSTIC CONTROL switch in PROCESS

b. Not power-on reset

c. MODE SELECT switch in PROCESS

Refer to ALD CU001 - BM6.

CAUTION

Disable all channel interfaces before proceeding.

CLOCK STEP

1. Set the DIAGNOSTIC CONTROL switch to CLOCK STEP.
2. Press RESET.—Verify that the HARDSTOP, PROGRAM STOP, TEST, and WAIT lights are on.
3. Set the DISPLAY/FUNCTION SELECT switch to STATUS.
4. Press START.—Check CYCLE TIME and CLOCK TIME in display A. CYCLE TIME should equal '00'; CLOCK TIME should equal '00'.
5. Press START repeatedly and observe the stepping of CLOCK TIME and CYCLE TIME. CYCLE TIME should increment each time CLOCK TIME steps from '11' to '00'.

NOTE: 3705-I only — Cycle time E occurs after cycle time A (00) and appears as a repeat of cycle A. Cycle F occurs after cycle B (01) and appears as a repeat of cycle B. E and F times are necessary because of bridge storage characteristics. Cycles C, D, and A follow in normal order.

INITIAL DATA PATH TEST (ALU-B SIDE, Z BUS, DISPLAY A)

1. Set the DISPLAY/FUNCTION SELECT switch to STORAGE ADDRESS.
2. Set the DIAGNOSTIC CONTROL switch to SINGLE ADDRESS SCAN.
3. Press START.
4. The address set in ADDRESS/DATA switches should be equal to Display A. Vary the ADDRESS/DATA switches to test various data bit combinations (for example, 0101, 5555, AAAA, etc.)
5. Compare display A with the switch values to check for data bit failures.
6. If data bit failures occur, refer to *CCU DATA BITS/CARD LOCATIONS* (page 1-190) for card swapping.

NOTE: This procedure can also be used as convenient way to display multiple storage locations. Data is displayed in display B.

7. Return the DIAGNOSTIC CONTROL switch to PROCESS.

STORAGE DATA PATH TEST (ALU-A SIDE, DISPLAY B)

1. Press STOP.
2. Display storage at any valid address using the set address and display storage procedure (page 1-130).
3. Press STORE.—The data in the ADDRESS/DATA switches is stored at the address displayed in step 2.
4. Press STORE again.—Display A should increment by 2 each time STORE is pressed. Display B should be the contents of the address indicated in display A.

NOTE: The data being stored is not displayed because TAR is incremented; the next storage location is displayed.

5. Verify that the correct data was stored by using the display storage procedure.
6. Set the DIAGNOSTIC CONTROL switch to SINGLE ADDRESS TEST PATTERN.
7. Press START.—The contents of display B should equal the value in the ADDRESS/DATA switches. Vary data pattern in the switches as desired.

STORAGE TEST PATTERN

1. Set the DIAGNOSTIC CONTROL switch to STORAGE TEST PATTERN.
2. Set the ADDRESS/DATA switches to 'FFFF'.
3. Set the DISPLAY/FUNCTION SELECT switch to STORAGE ADDRESS.
4. Press START.
5. Display A shows the incrementing address; display B shows the data.
6. If the machine stops because of a CC check, record the following:
   a. Failing storage address (equals the address in display A minus 2)
   b. Failing bits (Compare the ADDRESS/DATA switches and display B.)
   c. Set the DISPLAY/FUNCTION SELECT switch to STATUS.—Display A shows the error status.

NOTE: If a CC check has occurred, but the ADDRESS/DATA switches and display B are equal, the parity bit has probably failed. (The BYTE lights indicated the byte with the bad parity bit.)

7. Press CHECK RESET, then press START.
8. Repeat steps 1 through 6 using different data patterns in the ADDRESS/DATA switches (for example, 0000, 0101, 5555, AAAA, etc.)
9. Analyze failures to determine a failing pattern (data or addressing).

ROS TEST CONTROL

Verifies that IPL phase 1 and 2 execute correctly.

1. With the channel interface disabled, press LOAD on the local 3705. On the Remote 3705, press LOAD.

2. The IPL phase lights should equal '11' with the program looping, waiting for the 'interface enabled' signal. Do not enable the interface unless channel data transfer is desired. If trouble is suspected, refer to the ROS listing and to the ROS test section of this manual.

   a. If the IPL PHASE lights are '01', check the hardware reset function.

   b. If the IPL PHASE lights are '10', ROS test transfer to storage is incomplete.

      (1) Press RESET to force IPL phase 3 ('11').

      (2) Run the storage pattern test with data equal to 'FFFF' to establish a background pattern.

      (3) Press LOAD.

      (4) If the same failure occurs: Turn the DISPLAY/FUNCTION SELECT switch to TAR & OP REGISTER. Display A shows the next storage address. Press RESET and display storage starting at X'0000' to determine how much of ROS was loaded (data instead of FFFF).

3. Refer to *ROS TEST,* page 2-000 if a failure occurs in IPL phase '11'. (Local 3705.)

4. Refer to *Remote Loader Diagnostic Manual*, page 0-028, for ROS Testing for a Remote 3705.

ADDRESS COMPARE STOP, INSTRUCTION STEP, AND HARD STOP

1. Set the DISPLAY/FUNCTION SELECT switch to TAR and OP REGISTER.

2. Set the LOAD/STORE ADDRESS COMPARE switch to LOAD.

3. Set the MODE SELECT switch to ADDRESS COMPARE PROGRAM STOP.

4. Set the ADDRESS/DATA switches to '00012'.

5. Press LOAD. (The address compare pulse is available at 01A-B3P2-S09. See ALD page CU004.)

6. The 3705 should stop with:

   a. PROGRAM STOP light on.

   b. TEST light on.

   c. LOAD light on.

   d. DISPLAY A set to X'00014' (The instruction at address X'0012' was executed).

   e. ADDRESS COMPARE and PROG L1 lights are on, if the DISPLAY/FUNCTION SELECT switch is set to STATUS.

7. Set the MODE SELECT switch to INSTRUCTION STEP.

8. Press START. Verify that DISPLAY A equals X'00016' (IAR incremented).

9. Display register X'70'.

10. Store register X'70' (Ignore the data.)—The HARDSTOP light should be on.

PART 2. MISCELLANEOUS CONTROLS

This section tests the panel functions that are not required for ROS testing and analysis but are used for DCM Diagnostic Control Module control and indications. Note the input and output instructions can be executed from the control panel by displaying and storing into the external register. Refer to *Executing an Input or Output Instruction From the Control Panel* on page 1-160.

LOAD LIGHT

1. Press LOAD.—Verify that the LOAD light is on.

2. Press RESET.

3. Display register X'79'.

4. Store X'0040' in register X'79'.—Verify that the LOAD light is off.

SET AND RESET TEST MODE

1. Set the MODE SELECT switch to PROCESS.

2. Set the DIAGNOSTIC CONTROL switch to PROCESS.

3. Display register X'79'.

4. Store X'0010' in register X'79'.—TEST light goes off if it was on.

5. Store X'0020' in register X'79' —TEST light turns on.

SCOPE SYNC PULSE

1. Display register X'79'.

2. Store X'0002' in register X'79'.—Fires scope sync # 1 at 01A-B3M2-P10, ALD page CU015.

3. Store X'0001' in register X'79'.—Fires scope sync #2 at 01A-B3M2-P13, ALD page CU015.

WAIT LIGHT

1. Press RESET.—Verify that the WAIT light is on.

2. Set the DIAGNOSTIC CONTROL switch to SINGLE ADDRESS SCAN.

3. Press START.—Verify that the WAIT light is off.

4. Set the DIAGNOSTIC CONTROL switch to PROCESS.

OP REGISTER DATA AND CC CHECK

1. Press RESET.

2. Set the MODE SELECT switch to INSTRUCTION STEP.

3. Press LOAD (forces program level 1).

4. Store X'FFFF' in address X'0012' (Branch on Bit using register 7; this will be the first instruction executed).

5. Store X'0000' in address X'0014' (Invalid OP decode).

6. Store X'00000' in register X'07'.

7. Set DISPLAY/FUNCTION SELECT switch to TAR and OP REGISTER.

8. Press START.

   a. DISPLAY B equals X'FFFF' (instruction stored in Step 4).

   b. Repeat steps 4, 6, and 7 varying the data in Step 4 if a hot/cold bit is suspected in the OP REG.

9. Press START again.

10. The lights should indicate:

    a. CC check

    b. Invalid OP

    c. L1 program check

    d. Hardstop

11. Store X'4004' in register X'77'.

    a. CC CHECK lights should be reset.

    b. Invalid OP and L1 program check should be reset.

12. Reset the 3705.

DISPLAY/FUNCTION SELECT SWITCH AND PROGRAM DISPLAY

1. Reset the 3705.
2. Set the MODE SELECT switch to INSTRUCTION STEP.
3. Press LOAD (forces program level 1).
4. Store the following instructions at the given address:

   Address X'0012' - X'742C' (Puts contents of the DISPLAY/FUNCTION SELECT switch in CCU register 4.)
   Address X'0014' - X'7414' (Output register 4 to display register 1).
   Address X'0016' - X'7424' (Output register 4 to display register 2).
   Address X'0018' - X'A809' (Branch back to first instruction).

5. Set the DISPLAY/FUNCTION SELECT switch to TAR and OP REGISTER.
6. Press START to step through the program.
   a. Verify that the program loops.
   b. The PROGRAM DISPLAY light should turn on and off while the program is stepped.
7. Set the MODE SELECT switch to PROCESS.
8. Press START.
   a. The program should run continuously. (The PROGRAM STOP light should stay off.)
   b. The PROGRAM DISPLAY light should stay on.
9. Rotate the DISPLAY/FUNCTION SELECT switch to the following positions and check the values in both displays A and B bytes 0 and 1.
   a. STORAGE ADDRESS - X'1000'
   b. REGISTER ADDRESS - X'0800'
   c. FUNCTION SELECT 1 - X'0040'
   d. FUNCTION SELECT 2 - X'0020'
   e. FUNCTION SELECT 3 - X'0010'
   f. FUNCTION SELECT 4 - X'0008'
   g. FUNCTION SELECT 5 - X'0004'
   h. FUNCTION SELECT 6 - X'0002'
10. Press STOP to stop the program.

INTERRUPT REQUEST AND RESET

1. Press RESET.
2. Display register X'7F'. — Verify that bit 0.6 is off.
3. Press INTERRUPT.
4. Display register X'7F'. — Verify that bit 0.6 is on (Panel irpt req L3).
5. Store X'2000' in register X'77'. — Reset panel irpt req L3.
6. Display register X'7F'. — Verify that bit 0.6 is off.

PART 3. CCU DATA BITS—CARD LOCATIONS

This section shows cards containing the data bit groups and miscellaneous controls. This information should be useful when running either panel tests or memory IFTs. Logic references are given for further detail.

GENERAL DATA FLOW: Includes B register, LAR, local store, CCU display, ALU, SAR, TAR, A register, and ALU check bits.

Bits	X.4,X.5	X.P,X.6, X.7	0.P-0.1	0.2-0.4	0.5-0.7	1.P-1.1	1.2-1.4	1.5-1.7
Card	B4S2	A-B4J2	A-B4K2	A-B4L2	A-B4M2	A-B4N2	A-B4P2	A-B4Q2
ALD Page	DExxx	DF	DG	DH	DJ	DK	DL001-	DM001-

OP REGISTER AND SDR REGISTER

Bits	0.0-0.4	0.5-0.7,0.P	1.0-1.4	1.5-1.7,1.P
Card	A-B4G2	A-B4G2	A-B4H2	A-B4H2
ALD Page	DN001-004	DP001-004	DQ001-004	DR001-004

SAR AND SDR DRIVERS AND RECEIVERS (3705-I)

Frame	1	2	3	4
ALD Page	DS001-005	DT001-005	DU001-005	DV001-005
SAR Drivers	A-B4C2	A-B4C3	A-B4C4	A-B4C5
SDR Dr/Rec Byte 0	A-B4B2	A-B4B3	A-B4B4	A-B4B5
SDR Dr/Rec Byte 1	A-B4A2	A-B4A3	A-B4A4	A-B4A5

SAR AND SDR DRIVERS AND RECEIVERS (3705-II)

Frame	1	2
ALD Page	DS001-005	DT001
SAR Drivers	A-B4B2	A-B4B3
SDR Dr/Rec Byte 0	A-B4A3	Same as frame 1 through first storage assembly
SDR Dr/Rec Byte 1	A-B4A2	

MISCELLANEOUS LOGIC REFERENCES AND CARD LOCATIONS

Functions	ALD Pages	Cards
ALU Controls	CA001-004	01A-B3J2
Panel Controls	CU001-015	01A-B3N2, B3L2, B3P2
Clock and Controls	CC001-008	01A-B3Q2, B3R2
Data Flow Reg Controls	CS001-007	01A-B3F2, B4E2
Condition Codes	CZ001-005	01A-B3G2
Local Store Controls	CL001-005	01A-B3K2
Instruction Decode	CD001-004	01A-B3H2
Storage Controls	CM001-003	01A-B3T4
Priority Controls	CP001-007	01A-B3M2

DIAGNOSTIC AIDS: SCOPE POINTS AND JUMPERING CAPABILITIES

SCOPE POINTS

The following scope points can be used to diagnose problems:

A. '+ diag scope sync point 1' at 01A-B3M2-P10 on ALD page CU015. The DCM controls this sync point by means of an Output X'79' when bit 1.6 is a 1. Scope sync point 1 is used to sync on the beginning of each routine or on the hardware setup block when the DCM is in a scoping loop.

B. '+ diag scope sync point 2' at 01A-B3M2-P13 on ALD page CU015. The DCM controls this sync point by means of an Output X'79' when bit 1.7 is a 1. Scope sync point 2 is used to sync on the test function of a test routine.

Diag scope points 1 and 2 may be used together to count repetitions of the test function. Sync point 1 is used to trigger the scope and the delayed sweep feature is used to count the number of pulses (each pulse represents one repetition) on sync point 2.

See 'Setting Up a Scoping Loop' (below) for information on scoping for a failure while running the IFTs.

C. '+ address compare test pin' at 01A-B3P2-S09 on ALD page CU004. The STORAGE ADDRESS/REGISTER DATA switches on the control panel are used to establish a sync reference on this test pin at any location in any IFT routine or in the DCM. A sync pulse is generated when the address for fetch or store (controlled by the LOAD/STORE ADDRESS COMPARE switch) is the same as the address in the STORAGE ADDRESS/REGISTER DATA switches.

D. '-A time' at 01A-B3R2-P04 on ALD page CC001.

SETTING UP A SCOPING LOOP (IFT Failures)

After a failure has been detected, the DCM and IFTs provide two looping options.

- The Loop on First Error option selects the smallest possible loop within the IFT. The loop includes the hardware setup, pretest, set scope sync point 2, test, analysis, and error display. The loop for this option normally takes less time to execute than the Restart on First Error option. The loop continues whether or not the error occurs again.
- The Restart Routine on First Error option selects a loop that starts at the beginning of a routine, continues the routine to the point where the error was first detected, and then restarts the routine again. The loop for this option takes longer; however, it may be required for sequence-sensitive failures. The loop continues whether or not the error occurs again.

After selecting the looping option, use the continue function to continue from the error stop. The time required to stop on the error code again gives an indication of the length of the loop. Repeat this process several times and use the longest length of time.

To obtain continuous running loops, the 'bypass error stop' CE sense switch must also be set.

If an error other than the one selected for looping occurs, the DCM stops to display the new error code. To bypass stops for other errors, set the 'bypass new error stop' CE sense switch.

When the scoping loop is running correctly, the scoping indicator (Display B, bit 0.4) blinks at the rate of 3.2 seconds (1.6 seconds on and 1.6 seconds off). Display B (byte 0, bits 5, 6, and 7) is incremented by one for each error detected. This error counter (together with the loop time) indicates the failure is solid or intermittent. Other information is also displayed. Display A shows the adapter, IFT and routine number. Display B (byte 0, bits 0-3 and byte 1) shows the error code being looped on.

DIAGNOSTIC JUMPERING CAPABILITIES

The following jumpering capabilities can be used to diagnose problems.

Invoke IPL When an Address Compare Occurs

1. Plug the CE MST-1 latch card P/N 5851882 onto a socket position that has no second level wraps on any pin. Probe pins A, F, or M located on latch card according to instructions.

CAUTION The latch card must be plugged onto the board with the component side of the card toward the right or circuit damage will result.

2. Connect 01A-B3P2-S09 to pin A. Refer to ALD page CU004.
3. Connect 01A-B3L2-J09 to pin M. Refer to ALD page CU010.
4. Set the LOAD/STORE ADDRESS COMPARE switch and the ADDRESS/DATA switches as desired.

Invoke IPL When the 'Hard Stop' Latch Sets

1. Same as step 1 of *Invoke IPL When an Address Compare Occurs.*
2. Connect 01A-B3L2-M03 to pin F. Refer to ALD page CU006.
3. Connect 01A-B3L2-J09 to pin M. Refer to ALD page CU010.
4. Press the START push button.

Invoke IPL When the 'Machine Check' Latch Sets

1. Same as step 1 of *Invoke IPL When an Address Compare Occurs.*
2. Connect 01A-B3N2-J06 to pin F. Refer to ALD page CK006.
3. Connect 01A-B3L2-J09 to pin M. Refer to ALD page CU010.
4. Press the START push button.

Cause the 'Clock Step' Latch to Freeze the Clock When an Address Compare Occurs

1. Same as step 1 of *Invoke IPL When an Address Compare Occurs.*
2. Connect 01A-B3P2-S09 to pin A. Refer to ALD page CU004.
3. Connect 01A-B3P2-J09 to pin M. Refer to ALD page CU007.
4. Set the LOAD/STORE ADDRESS COMPARE switch and the ADDRESS/DATA switches as desired.
5. Press the START push button.
6. Set the DIAGNOSTIC CONTROL switch to CLOCK STEP after the address compare stop.

Cause the 'Clock Step' Latch to Freeze the Clock When the 'Hard Stop' Latch Sets

1. Same as step 1 of *Invoke IPL When an Address Compare Occurs.*
2. Connect 01A-B3L2-M03 to pin F. Refer to ALD page CU006.
3. Connect 01A-B3P2-J09 to pin M. Refer to ALD page CU007.
4. Press the START push button.
5. Set the DIAGNOSTIC CONTROL switch to CLOCK STEP after the hard stop.

Prevent Loading of ROS During IPL

Connect 01A-B3L2-U02 to 01A-B3L2-G08. Refer to ALD page CU010.

Cause the 'Clock Step' Latch to Freeze the Clock When the 'Machine Check' Latch Sets

1. Same as step 1 of *Invoke IPL When an Address Compare Occurs.*
2. Connect 01A-B3N2-J06 to pin F. Refer to ALD page CK006.
3. Connect 01A-B3P2-J09 to pin M. Refer to ALD page CU007.
4. Press the START push button.
5. Set the DIAGNOSTIC CONTROL switch to CLOCK STEP after the machine check.

Simulate a Continuous Panel Display Register Operation

1. The 3705 must be stopped.
2. Set the DISPLAY/FUNCTION SELECT switch to REGISTER ADDRESS.
3. Set ADDRESS/DATA switches B and D to the desired register address.
4. Press the SET ADDRESS DISPLAY push button.
5. Jumper 01A-B3P2-J03 to ground. Refer to ALD page CU003.

NOTE: This operation does not occur every time. Therefore, when scoping, use a cycle steal time as a sync point. (CS1A-B3Q2B10 on CC002)

Simulate a Continuous Panel Store Register Operation

1. The 3705 must be stopped.
2. Set the DISPLAY/FUNCTION SELECT switch to REGISTER ADDRESS.
3. Set ADDRESS/DATA switches B and D to the desired register address.
4. Press the SET ADDRESS DISPLAY push button.
5. Jumper 01A-B3P2-J06 to ground. Refer to ALD page CU003.
6. Set the ADDRESS/DATA switches B thru E to the desired data.

NOTE: This operation does not occur every cycle time. Therefore, when scoping, use a cycle steal time as a sync point.

Deactivate Interval Time Bids

Jumper 01A-B3M2-G09 to ground. Refer to ALD page CU014.

NOTE: If a bid has already been set, that bid will be honored before the interval timer is deactivated.

Clock Step Thru IPL Phase 2 (Load ROS)

1. Press the RESET push button.
2. Set the DIAGNOSTIC CONTROL switch to CLOCK STEP.
3. Press the START push button.
4. Jumper 01A-B3P2J09 (+ Active clock step) to 01A-B3L2D09 (+IPL 2 Latch). Refer to ALD pages CU007 and CU010.
5. Press the LOAD push button. Observe IPL phase 2 when the LOAD push button is released.
6. You can now clock step thru the loading of ROS by using the START push button.

DIAGNOSTIC AIDS - CE INDICATOR LATCH CARD

MST-1 CE Indicator Latch Card

C. E. Indicator Latch Card P/N 5851882 is available from Mechanicsburg for servicing IBM products using the MST-1 technology.

The Latch Card is a 2-High, 2-Wide card which plugs onto the pin side of an MST-1 board. The card can be plugged onto any two vertically adjacent socket positions except edge connector positions. The Latch Card is intended for use on socket locations with no discrete wiring; however, with care, it can be used on socket positions that have no second level wraps on any pin. If the Latch Card is left on an MST-1 board for an extended period of time, normal machine vibration may cause it to work loose from the pins and lose contact.

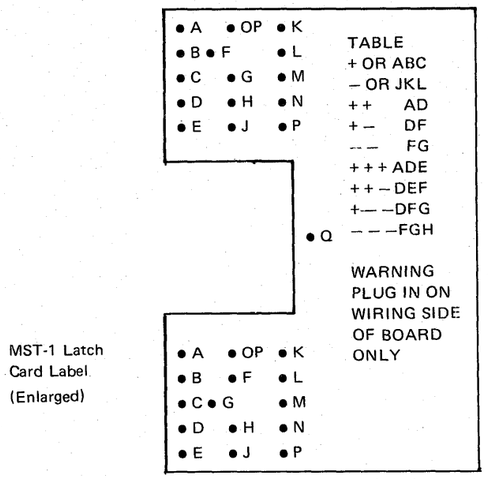
CAUTION

The Indicator Latch Card must be plugged onto the MST-1 board with the component side of the card toward the right. If the card is plugged on upside down, or is plugged into the card side of the board, circuit damage will result.

The Latch Card contains two complete latch circuits. Each latch circuit has its own set of input pins, output pins, and latch status indicator lamp.

A reset line which is common to both latch circuits can be activated by the manual reset switch or by a plus signal applied to program pin Q.

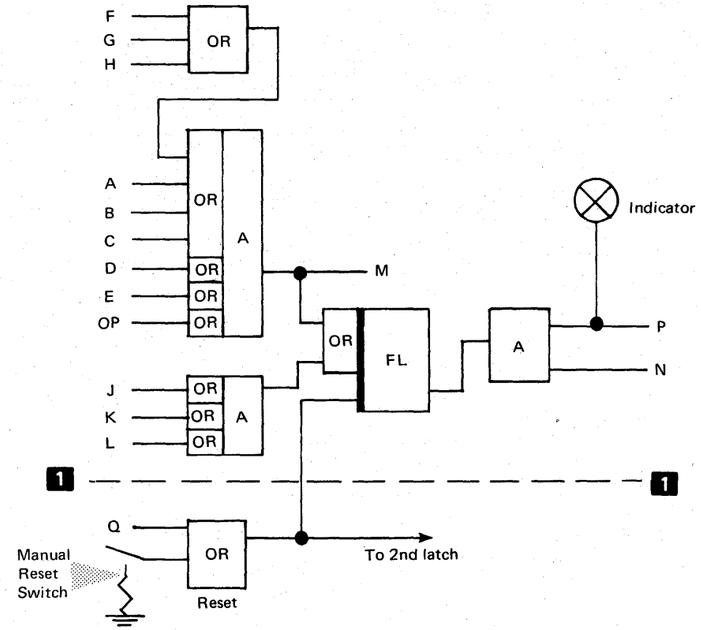
The correlation between active signal levels and input pins to be used is shown below for the various combinations which can be monitored.



Pin OP is an optional, plus level input pin. It can be used in place of, or in addition to, input pins D and E.

Output pin M is a summation of input pins A through H prior to the latch. Pin M will be at a plus level whenever the combination of signals being monitored is active. Thus, the signal occurring at output pin M can be used as an input to the latch circuitry contained on the other half of the latch card.

Output pins P and N provide outputs from the latch. Output pin P will be at a plus level when the latch is set (indicator lamp on) and at a negative level when the latch is reset (indicator lamp off). Pin N provides the inverse level of pin P.



Note: The CE Indicator Card contains two sets of circuitry as shown above line 1 — 1

Listed below are some of the ways the latch card can be used:

1. Baby Sitter

   To determine if several signal lines are all at their active levels at the same time, plug the card onto the pin side of the MST-1 board and jumper the signal lines to the proper input pins for the ANDing condition being monitored. If all signal lines are at their active level at the same time, the latch will be set and turn on the indicator lamp.

2. One-Time Pulse Detection

   If a signal line should not change during a particular sequence of events, jumper the signal line to an appropriate OR input pin. For example, if the line is plus and should never go minus, jumper it to a -"OR" input pin. If the line goes to a minus level, the latch will be set and turn on the indicator lamp.

3. Scope Sync Point

   The signal lines required to generate the desired sync should be jumpered to appropriate input pins. Jumper a plus level reset signal to pin Q. The latch will be set by the sync condition and reset under control of the reset line. The signal at latch output pin P or N can now be used as a stable scope sync.

Use C. E. Jumper P/N 4110178, cut to required length. The ends of this wire are simply plugged onto the pins to be connected. The plastic insulation coating serves as a receptacle for the pin.

MST-1 Indicator Latch Card P/N 5851882
Indicator Lamp P/N 5353889
Jumper P/N 4110178 Specify length when ordering.
MST-1 Latch Card label P/N 5500728.

Note: The latch card does *not* include a label. Always order a label for each latch card.

DIAGNOSTIC AIDS: TEST BLOCKS

These illustrations provide a ready reference to the interface leads available at the interface connector positions on the I/O gate. Some Communication Scanner IFT Manual Intervention Routines refer to wrapping a pair of lines or tying certain lines up or down. The test blocks provide a convenient method of doing this in most cases.

To force an interface lead to the active state, jumper it to 'Data Terminal Ready'. The state of DTR can be determined from the symptom index. If the inactive state of an interface lead is to be tested, allow the lead to float. EIA, CCITT V.35 (except for transmit and receive data), and digital interface lines float to the inactive level.

To wrap data between two compatible line interfaces, jumper all interface leads to their normal operational state. Use the check lists below for typical jumpering.

FOR INTERFACES THAT CONNECT TO STAND-ALONE MODEMS OR LOCAL ATTACHMENTS, JUMPER:

a. 'Request to Send' and 'Clear to Send' of the transmit interface to 'Receive Line Signal Detect' (Carrier Detect) of the receive interface using Y jumper P/N 1770810.

b. 'Request to Send' and 'Clear to Send' of the receive interface to 'Receive Line Signal Detect' (Carrier Detect) of the transmit interface using Y jumper P/N 1770810.

c. 'Data Terminal Ready' to 'Data Set Ready' on both interfaces. (See special notes for the 1G line set on page 1-310).

d. Send data of one line to receive data of the opposite line.

e. Receive data of one line to send data of the opposite line.

FOR INTERFACES WITH IBM LIMITED DISTANCE OR LEASED LINE ADAPTERS OR WITH LEASED LINE MODEMS, JUMPER:

a. Send data to receive data of the opposite line.

b. Receive data to send data of the opposite line.

FOR TELEGRAPH CURRENT LOOP INTERFACES (See Line Set 2A test block), JUMPER:

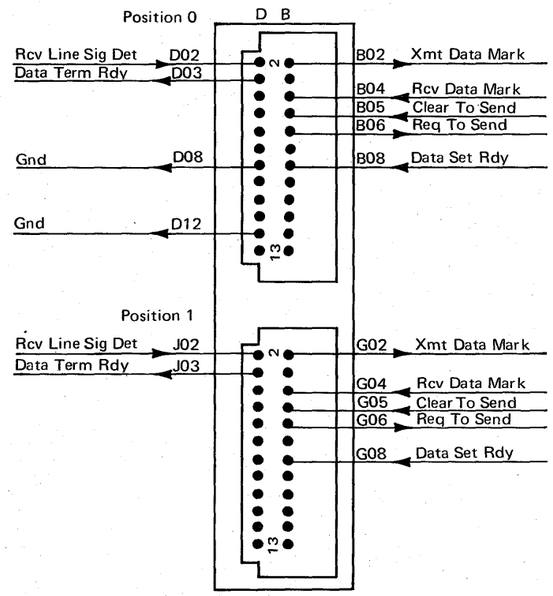
a. Ring + of position 0 through a 100 ohm, 1 watt resistor to H2G11 (+6 Vdc) on the LIB Type 2 board.

b. TIP of position 1 to any D08 pin (ground) on the LIB Type 2 board.

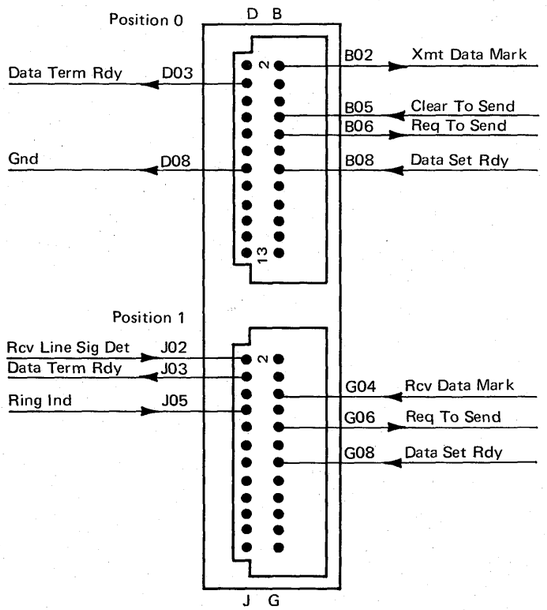
c. TIP of position 0 to Ring + of position 1.

Note: Test Blocks are shown facing the jumper pin side. See page E-010 for jumper and test block part numbers.

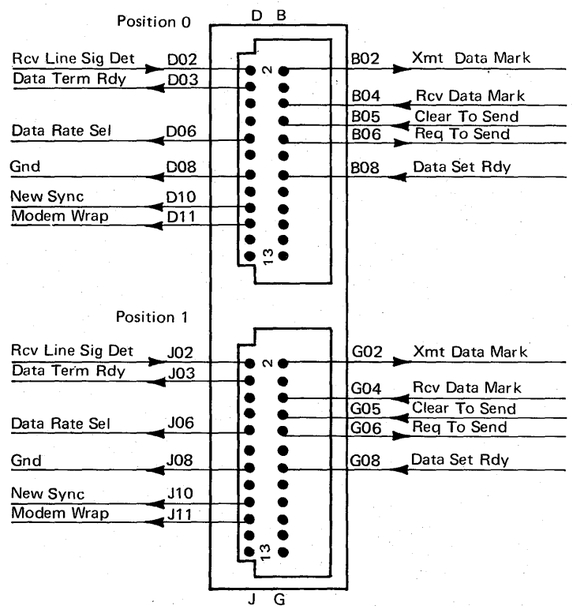
Line Set 1A (Logic VA003)
(Note 1)



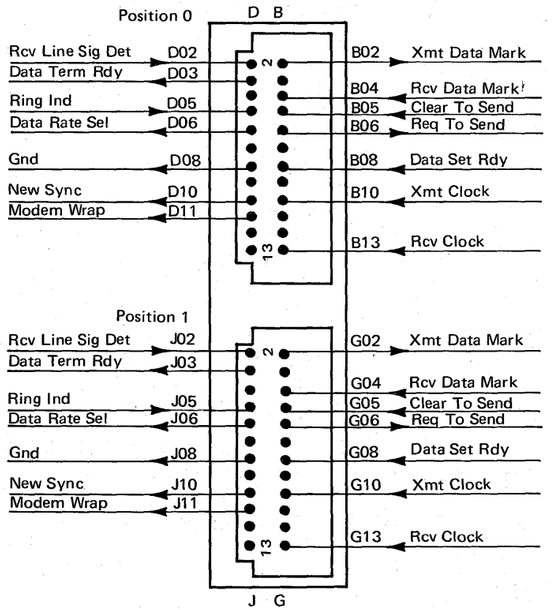
Line Set 1B (Logic VA011)
(Note 1)



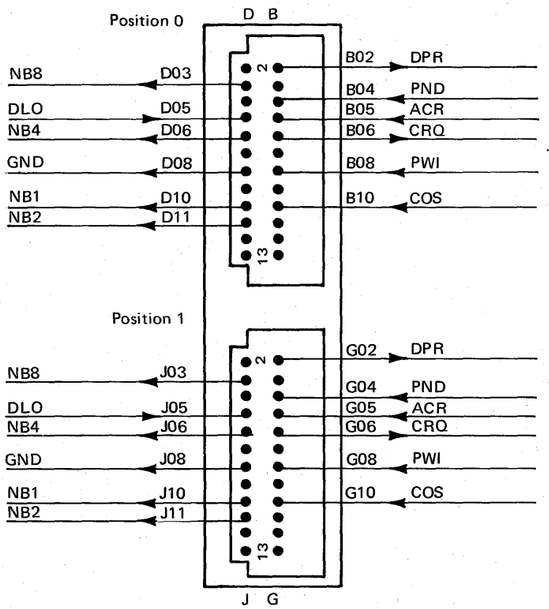
Line Set 1C (Logic VA009)
(Note 1)



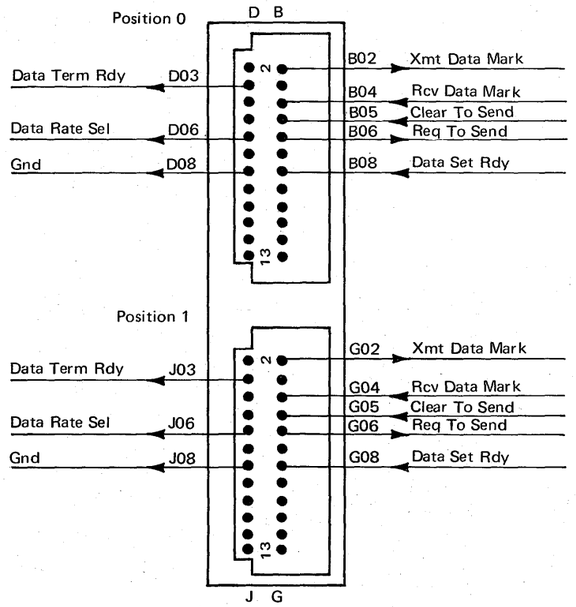
Line Set 1D (Logic VA004)
(Note 1)



Line Set 1E (Logic VA005)
(Note 2)



Line Set 1F (Logic VA010)
(Note 1)

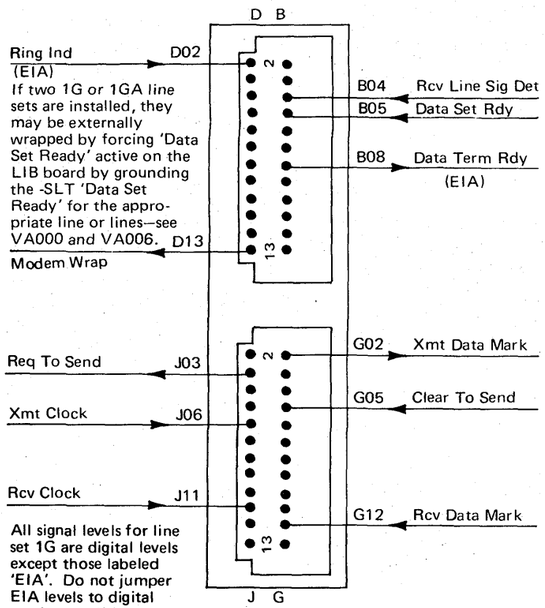


Notes:
1. Line sets 1A, 1B, 1C, 1F, and 1H are no longer available for the IBM 3705. The functions these line sets provided are now performed by line set 1D. However, appropriate cables must be attached to the 1D line set. Refer to "Line Set 1D" on C-002.
2. Line set 1E can not be wrapped using this block-jumper reference only.

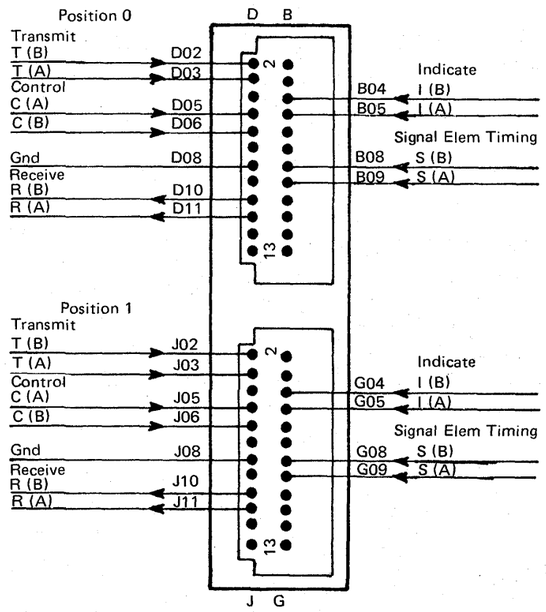
CP

DIAGNOSTIC AIDS: TEST BLOCKS (PART 2)

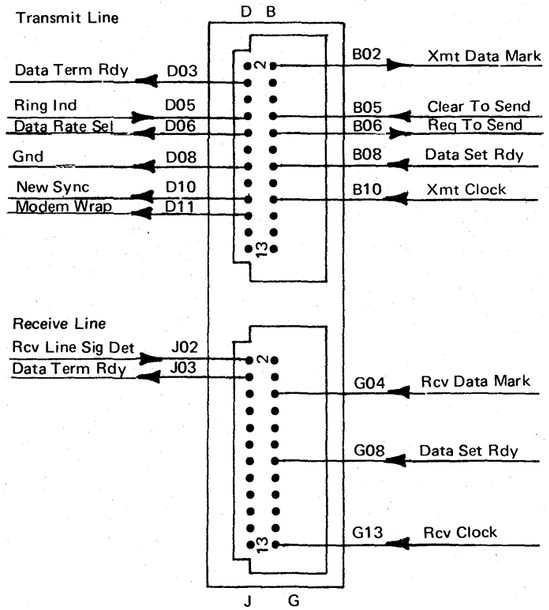
Line Set 1G or 1GA (Logic VA006)



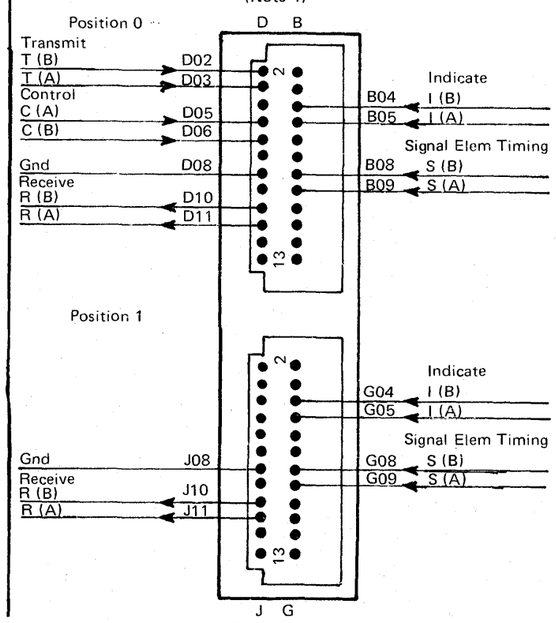
Line Set 1N — Half-Duplex (Logic VA017)
(Note 1)



Line Set 1H (Logic VA012)
(Note 5)



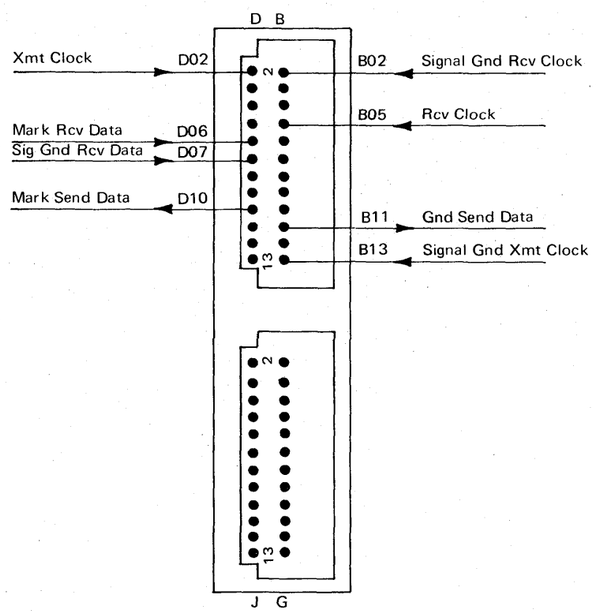
Line Set 1N or 1R — Duplex (Logic VA017)
(Note 4)



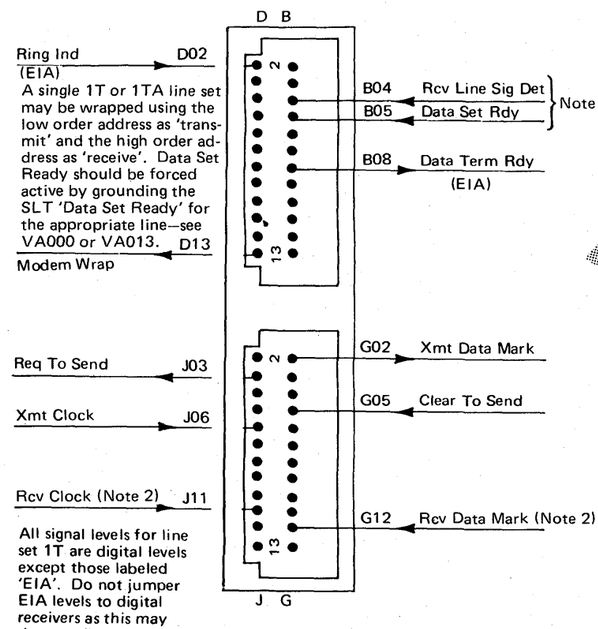
Notes:

1. To wrap a pair of lines, connect T of the transmit line to R of the receive line and C of the transmit line to I of the receive line (connect A to A and B to B). Do not wrap S leads. Internal clock must be specified.
2. Signals used only by high-address receive line.
3. Signals used by both low-address transmit line and high-address receive line. Signals not noted are used only by the low-address transmit line.

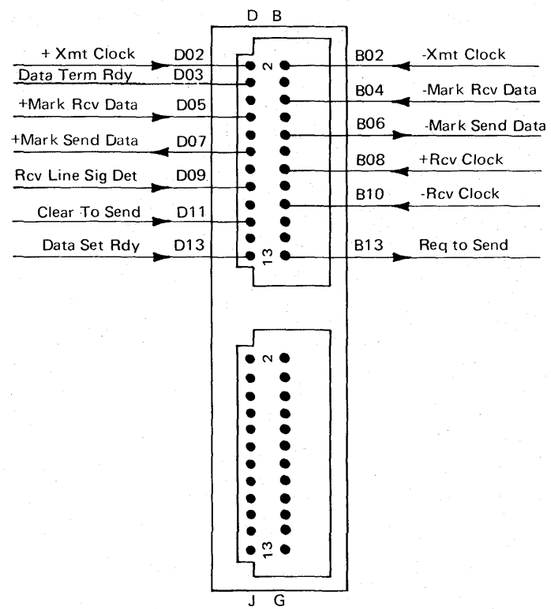
Line Set 1J (Logic VA007)



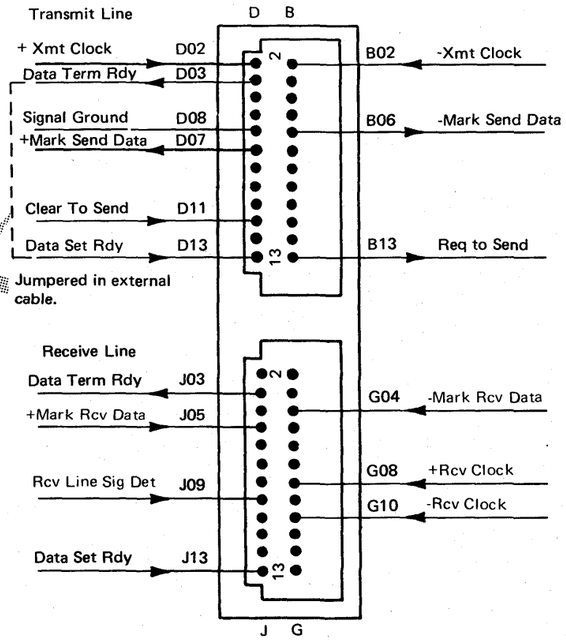
Line Set 1T or 1TA (Logic VA013)



Line Set 1K and 1S (Logic VA008)



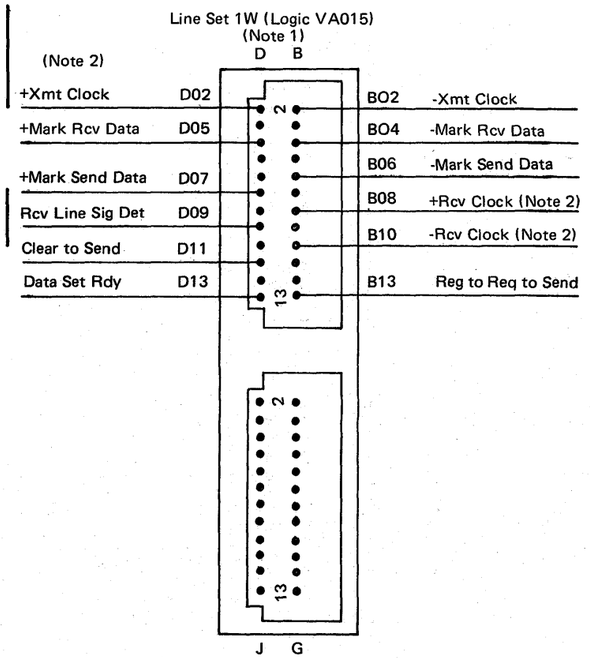
Line Set 1U (Logic VA014)



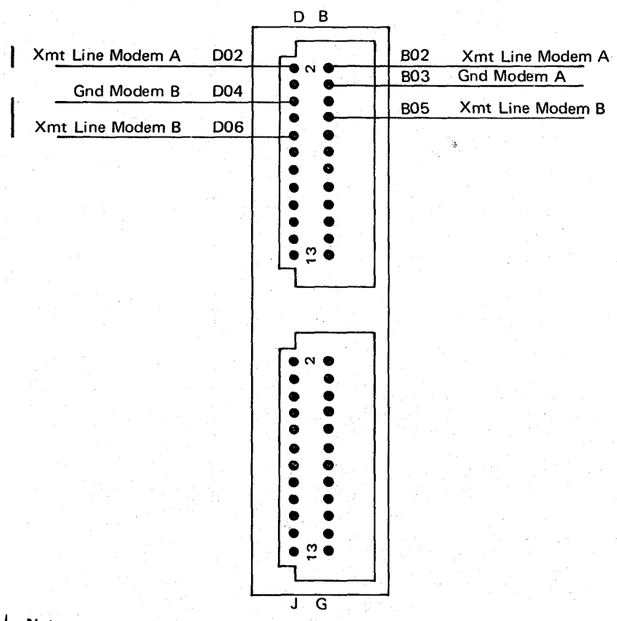
4. To wrap a pair of duplex lines, connect T (transmit) of position 0 to R (receive) of both position 0 and 1. Next, connect C (control) of position 0 to I (indicate) of both position 0 and 1. (Connect A to A and B to B.) Do not wrap S leads. Internal clock must be specified.
5. Line sets 1A, 1B, 1C, 1F, and 1H are no longer available for the IBM 3705. The functions provided by these line sets are now performed by line set 1D. However, appropriate cables must be attached to the 1D line set. Refer to "Line Set 1D" on C-002.

DIAGNOSTIC AIDS: TEST BLOCKS (PART 3)

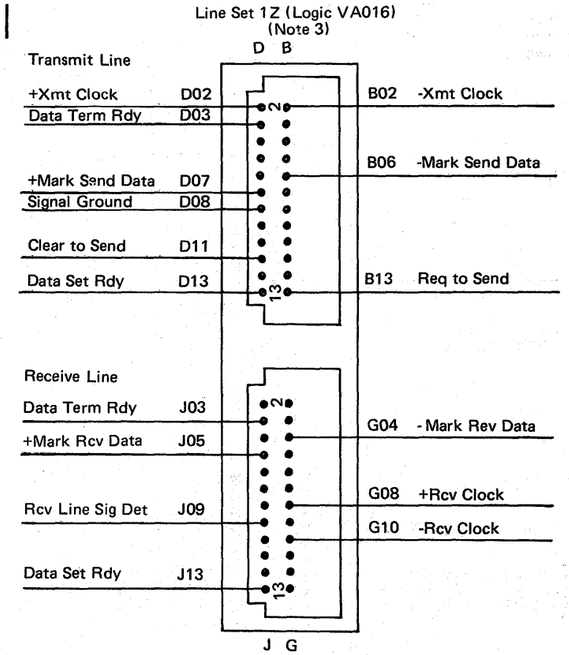
Line Set 1W (Logic VA015)
(Note 1)



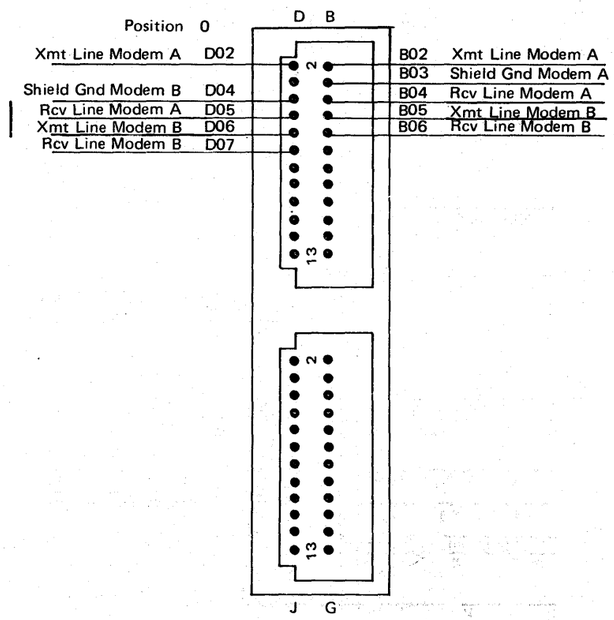
Line Set 4A & 4B (Logic VG003 & VG004)



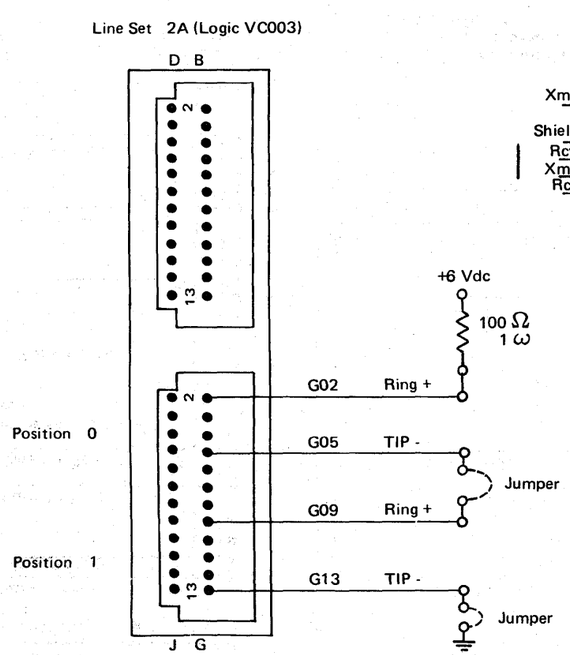
Line Set 1Z (Logic VA016)
(Note 3)



Line Set 4C (Logic VG005)

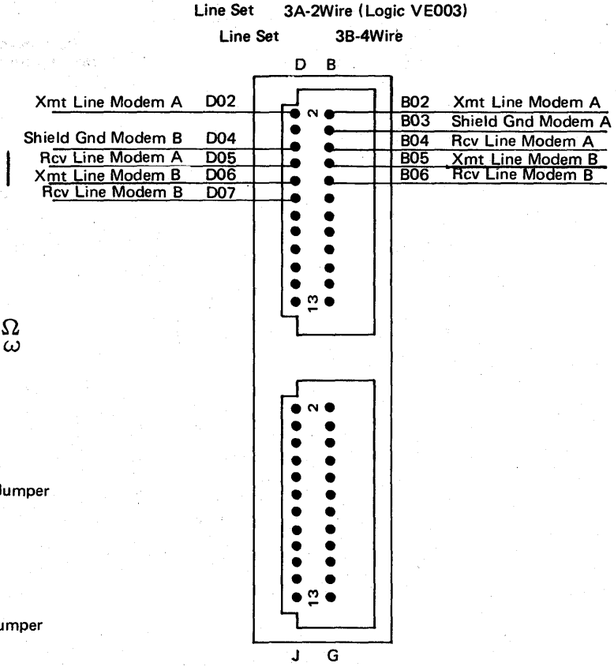


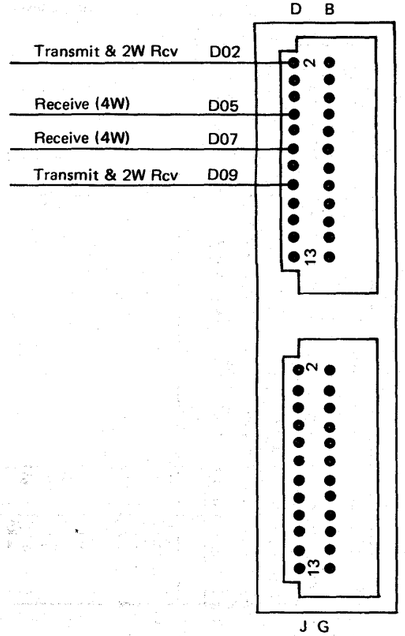
Line Set 2A (Logic VC003)



Line Sets 5A and 5B (Logic VJ400)

Line Set 3A-2Wire (Logic VE003)
Line Set 3B-4Wire





Notes:

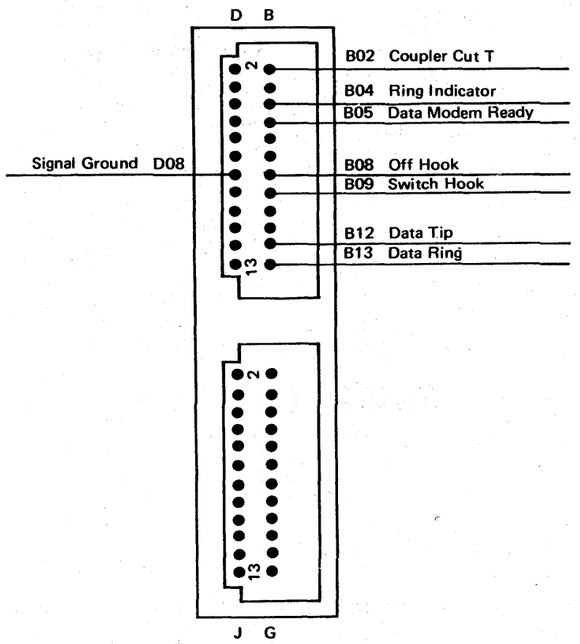
1. Line Set 1W must be wrapped to either a 1K/1S Line Set or a 1W Line Set on the same LIB with external clock option specified.
2. Wrap the clock leads as follows:

From 1W		To 1K/1S
-Xmt Clock (B02)	------	+Rcv Clock (B08)
+Xmt Clock (D02)	------	-Rcv Clock (B10)
-Rcv Clock (B10)	------	+Xmt Clock (D02)
+Rcv Clock (B08)	------	-Xmt Clock (B02)

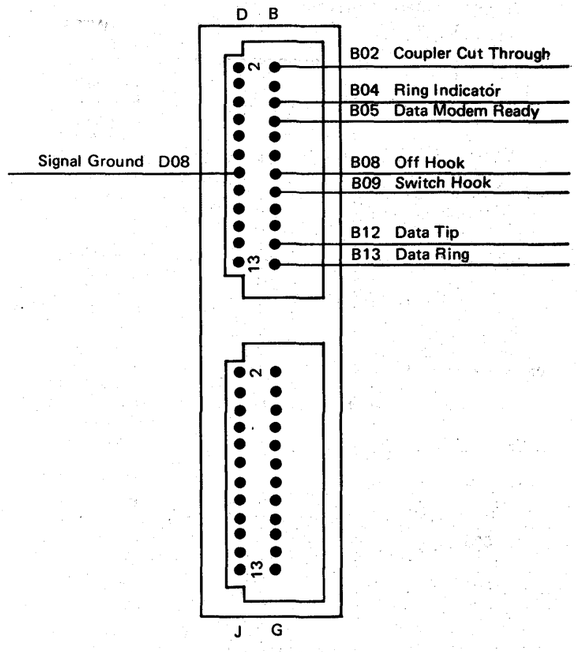
3. To use line set wrap on a 1Z Line Set, specify external clock option, and wrap the 1Z transmit line to the 1Z receive line. Do not wrap clock leads.

DIAGNOSTIC AIDS: TEST BLOCKS (PART 4)

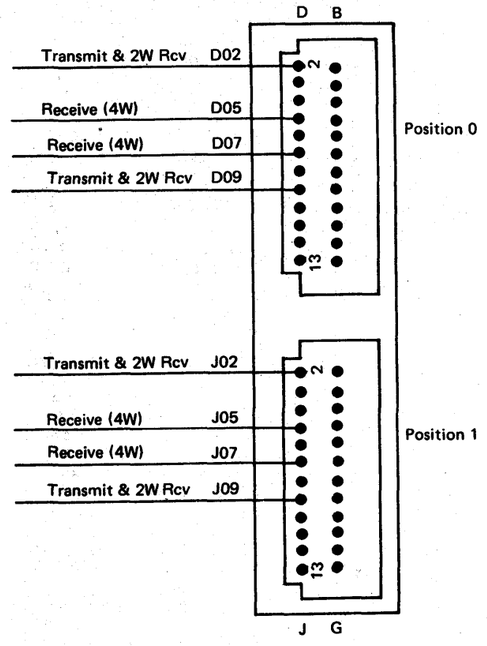
Line Set 6A (Logic VL026) and Line Set 9A (Logic VS025)



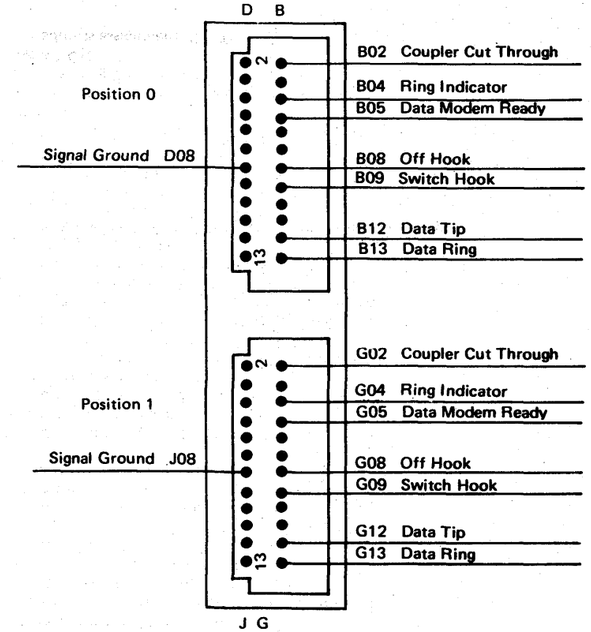
LIB 7 (Logic VN027)



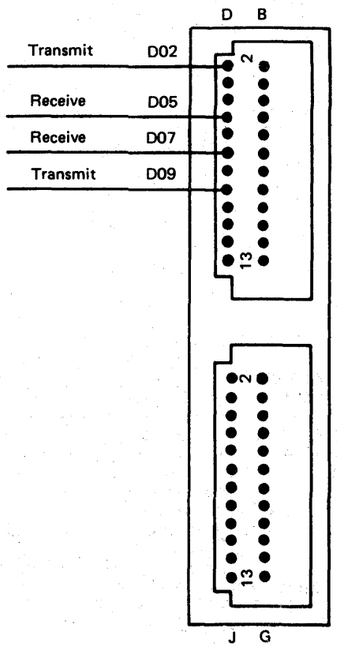
Line Set 8A (Logic VQ025/026)



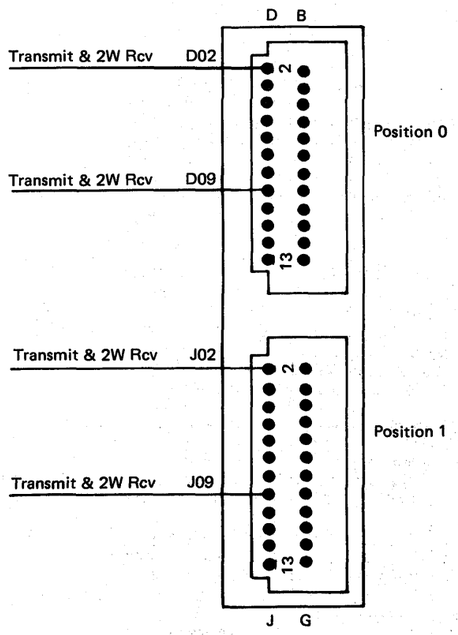
Line Set 8B (Logic VQ025/026) and
Line Set 12B (Logic VX025/026)



Line Sets 10A (Logic VU130), and 11A or 11B (Logic VW300)



Line Set 12A (Logic VX025/026)



ROS TEST

ROS Requirements Depending On Type of Channel Adapter and or Remote Program Loader.

Without Remote Program Loader (RPL) 3705-II only

		CA #2					CA #3	CA #4
		None	CA1	CA2	CA3	CA4	CA4	CA4
CA #1	CA1	1	X	D	D	X	X	X
	CA2	2	X	D	D	X	X	X
	CA3	2	X	D	D	X	X	X
	CA4	1	X	D	D	1 or N†	N	N

With Remote Program Loader (3705-II only)

		CA #2					CA #3
		None	CA1	CA2	CA3	CA4	CA4
CA #1	CA1	R and 1	X	R and D	R and D	X	X
	CA2	R and 2	X	R and D	R and D	X	X
	CA3	R and 2	X	R and D	R and D	X	X
	CA4	R and 1	X	R and D	R and D	R and (1 or N)†	R and N

3705 - II with only RPL uses the RPL ROS.
† 1 — Required for two CA4s with the IPL switch
N — Required for two CA4s without the IPL switch
1 = CA1 ROS (Mini)
2 = CA2 ROS (Maxi)
D = Dual ROS
N = CA4 ROS (3705-II only) see 2-120
R = RPL ROS (3705-II only)
X = Invalid configuration

TYPE 1 AND TYPE 4**CHANNEL ADAPTER

The instructions contained in the ROS program depend upon the type channel adapter that is installed in the 3705. The ROS code enables the controller to load its control program across the channel.

Before the ROS code attempts to transfer the data, it checks the functions and instructions it needs to complete the transfer. The functions tested are:

- Instructions
- Data path
- Channel adapter enable
- Channel adapter selection
- Channel adapter level 3 interrupt
- Receipt of an IPL command on each enabled channel adapter
- That a level 1 or level 3 interrupt was received from the channel adapter

Only the portion of the instructions needed to complete the transfer of the first program module across the channel is tested. The instructions tested are:

- ARI
- LRI
- ORI
- TRM
- LH
- STH
- ST
- BB
- BCL
- BZL
- B
- XR
- IN *, X'60,61,62,64,67,76,77,79,7D,7E'
- OUT *, X'60,62,63,64,66,67,77,79'

*Those input and output instructions associated with the CA and several of those necessary for CCU operation are used but are not thoroughly tested.

ROS checks the data path and uses some of the error detection circuits without testing them.

A listing of the ROS code is in the ALD's beginning on CW101. A flow chart showing the logical flow of ROS-channel adapter operations precedes the ROS listing in the ALDs.

SIMULATION RUN

Immediately following the ROS listing is a simulation run. The simulation run is a listing in instruction execution order showing the contents of the registers used.

Use the simulation run during instruction step procedures in the instruction test portion of ROS as a check for correct operation.

ERROR ANALYSIS PROCEDURE

Type 1 ROS code presents error indications to the control panel for CCU and channel adapter errors. Observe the error indications and follow the prescribed course of action for each indication.

CONTROL PANEL SWITCHES

During the IPL, the MODE SELECT switch and the DIAGNOSTIC CONTROL switch must be in the PROCESS position for the indicators to function correctly.

** See H-000 for the type 4 configurations that use this ROS Test

INSTRUCTION TESTING

Before trying to load data across the channel, ROS Program code tests the preceding instructions. The general procedure for locating an instruction execution failure is to step the instructions through the failing section of the instruction test portion of the code.

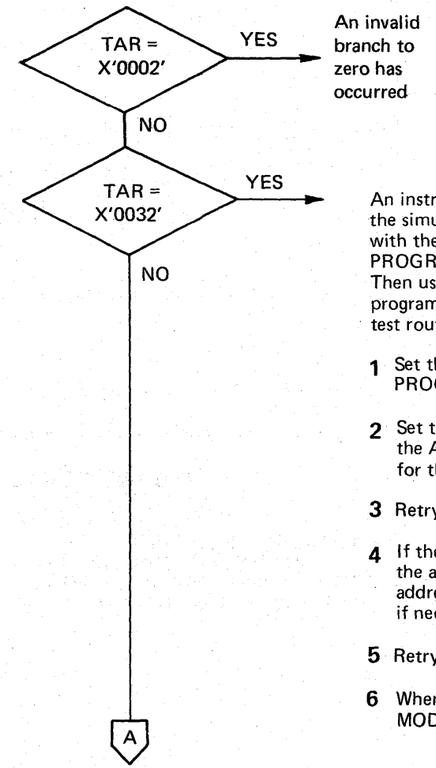
The simulation run following the ROS code listing in the ALD is to be used during the instruction step procedure as a check for correct operation.

The indications that appear on the control panel are:

IPL Phase III
Program Stop
Hard Stop
Load
Test

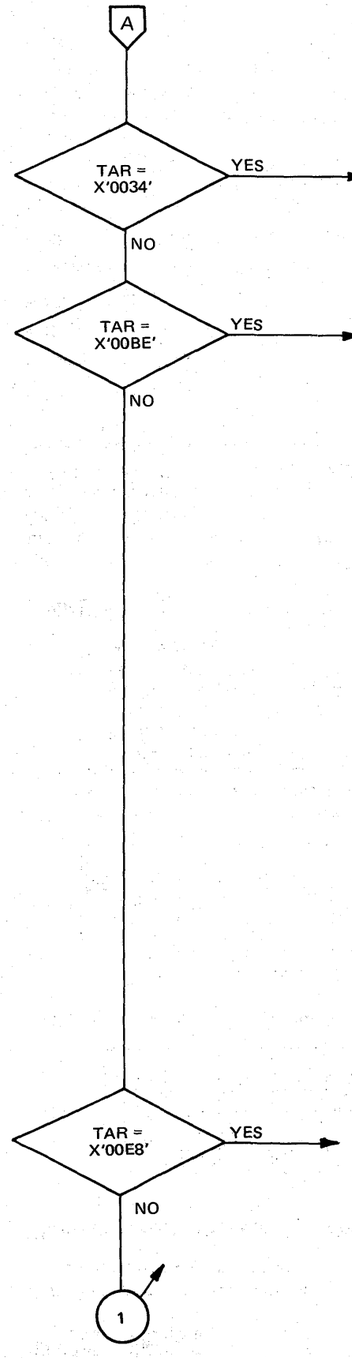
This is a CCU failure indication. TAR contains the address of the next instruction to be executed. This value is the address of the stop instruction +2. Check the contents of TAR against the following list; if it is equal to any value given, follow the indicated procedure.

See page 2-020
If these lamps are not on.



An instruction failed to execute. Using the ROS listing and the simulation run, use the *load address compare* procedure with the MODE SELECT switch set to ADDRESS COMPARE PROGRAM STOP to stop at various places in the program. Then use the *instruction step* procedure to step through the program and locate the failure addresses at the beginning of test routines in the listing as stopping points.

1. Set the MODE SELECT switch to ADDRESS COMPARE PROGRAM STOP.
2. Set the beginning address for one of the test routines in the ADDRESS/DATA switches. Refer to the ROS listing for the beginning addresses of the routines.
3. Retry the IPL.
4. If the same error occurs before the program stop, change the address in the ADDRESS/DATA switches to a previous address. The address of the first instruction may be used if necessary.
5. Retry until the program stop occurs.
6. When the program stops at the selected address, set the MODE SELECT switch to INSTRUCTION STEP.
7. Step through the code, following the listing and the simulation run, to locate the error. (See CW000.)



Output instruction failure.

A branch on bit failure or 'Z' latch failing to set caused this hard stop condition.

1 Set up to program stop at the beginning address of the Branch on Bit Test (X'00A4') from the ROS listing.

2 Retry the IPL.

3 When the Program Stop light comes on, set the MODE SELECT switch to INSTRUCTION STEP.

4 Step through the test. Register 1 contains the instruction and indicates what is being tested. Bit 0.7 on indicates that byte 1 is being tested, and bit 0.7 off indicates that byte 0 is being tested. Bits 0.2, 0.3, and 1.0 are a binary indication of the bit being tested within the byte. The bits are being tested for "solid" on and off conditions.

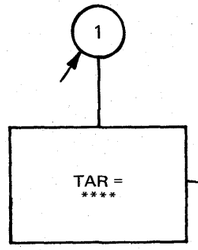
Register 1		Bits Being Tested	
Byte 0 01234567	Byte 1 01234567	Byte 0 01234567	Byte 1 01234567
XX00XXX0	0XXXXXXX	10000000	00000000
XX00XXX0	1XXXXXXX	01000000	00000000
XX01XXX0	0XXXXXXX	00100000	00000000
XX01XXX0	1XXXXXXX	00010000	00000000
XX10XXX0	0XXXXXXX	00001000	00000000
XX10XXX0	1XXXXXXX	00000100	00000000
XX11XXX0	0XXXXXXX	00000010	00000000
XX11XXX0	1XXXXXXX	00000001	00000000
XX00XXX1	0XXXXXXX	00000000	10000000
XX00XXX1	1XXXXXXX	00000000	01000000
XX01XXX1	0XXXXXXX	00000000	00100000
XX01XXX1	1XXXXXXX	00000000	00010000
XX10XXX1	0XXXXXXX	00000000	00001000
XX10XXX1	1XXXXXXX	00000000	00000100
XX11XXX1	0XXXXXXX	00000000	00000010
XX11XXX1	1XXXXXXX	00000000	00000001

X = don't care

A level 1 interrupt was requested by other than an IPL level 1 interrupt request. The IPL request was expected. Other conditions that could have caused the interrupt are:

Condition:

Address compare
Adapter check
In/out check
Address exception
Protect check



If TAR contains an address that has not been previously defined, a program load or execution failure probably occurred. To verify the program was loaded correctly, execute the ROS Data Transfer Test and the ROS Address Generation Test.

ROS Data Transfer Test

Display main storage addresses

1 location X'0032' → All bits should be off in Display B. Suspect any bit that is on in the display as being continuously on from storage (see 7-030 or 7-260). The bit can also be continuously on from ROS, (see 6-961).

2 location 0056 → All bits should be on in Display B. Suspect any bit that is not on as being continuously off from storage (see 7-030 or 7-260). The bit can also be continuously off coming from ROS, (see 6-961).

ROS Address Generation Test

Display main storage addresses

1 X'0000' should contain X'7004' →

If location X'0000' contains	Suspect SAR Bit	3705-I See	3705-II See
X'F6FF'	15 on	7-030	7-260
X'98B8'	14 on	7-030	7-260
X'810B'	13 on	7-030	7-260
X'0082'	12 on	7-030	7-260
X'0492'	11 on	7-030	7-260
X'F1FF'	10 on	7-030	7-260
X'1305'	9 on	7-030	7-260
X'6174'	8 on	7-030	7-260

2 X'01FE' should contain '0404' →

If location 01FE Contains	Suspect SAR Bit	See	See
X'1001'	15 off	7-030	7-260
X'81FE'	14 off	7-030	7-260
X'6124'	13 off	7-030	7-260
X'9813'	12 off	7-030	7-260
X'8602'	11 off	7-030	7-260
X'A8A3'	10 off	7-030	7-260
X'A863'	9 off	7-030	7-260
X'8160'	8 off	7-030	7-260

These charts are valid only for intermittent errors. ROS must load into storage correctly at least one time out of a number of Load pushbutton operations, for these charts to be valid. Otherwise, use control panel and display procedures (1-140) to determine if there is an addressing problem.

NOTE: Only SAR bits 8 through 15 are used to address low storage. The other SAR bits are not used.

If no discrepancy has been found in the ROS Data Transfer or Address Generation Test, verify that the control panel is set up properly and re-try the IPL.

CHANNEL CHECKING

IPL Phase III Load

This is an indication that communications between the channel adapter and the host CPU should be checked, using OLTEP or OLTSEP with the initial test, OLTs or IFTs. The customer's first program may be used if desired. Refer to the status and sense information chart at the end of this section if CA operation is possible but the load operation is not successful. If CA operation is not possible, proceed with the CA ROS checkout routines.

If the instruction testing has been completed, try the type 1 channel adapter ROS checkout routine when there is a problem.

Type 1 or Type 4 Channel Adapter ROS Checkout Routine

1 Disable all channel interfaces. Verify that the control panel INTERFACE ENABLED lights are off.

2 Press the RESET push button.

3 Press the LOAD push button.

4 Press the STOP push button.

5 Set the MODE SELECT switch to INSTRUCTION STEP.

6 Set the DISPLAY/FUNCTION select switch to TAR & OP REGISTER.

7 Press the START push button. Observe the address in display A.

8 Press the START push button several more times and observe the program looping through addresses X'00E8', '00EA', '00EC', '00EE', '00F0', '00F2', '00F4', and '00F6'

9 If this loop is not being executed, one of the following problems is indicated:

- An interface remained enabled.
- An incorrect branch occurred
- Contents of storage is incorrect.

To locate the failure

10 Use the *load address compare* procedure with the MODE SELECT switch set to ADDRESS COMPARE PROGRAM STOP to stop at X'00E4'. Then follow the ROS listing using the instruction step procedure.

Observe the normal program loop while the 3705 is waiting for initial selection. The host must be *unable* to select the 3705 for an IPL.

1 Enable an interface (more than one interface may be installed; enable only one). When an interface is enabled, ROS code may cause IPL phase 1 and 2 if certain conditions are present.

2 Press the CHECK RESET push button.

3 Press the LOAD pushbutton. Verify that the correct interface enabled light comes on.

4 Press the STOP pushbutton.

5 Set the MODE SELECT switch to INSTRUCTION STEP.

6 Set the DISPLAY/FUNCTION SELECT switch to TAR & OP REGISTER.

7 Press the START push button. Observe the address in display A. With the LOAD light on, continue to press the START push button to display the loop X'0124', '0126', '0128', '012A' and '012E'.

8 Set the MODE SELECT switch to PROCESS.

9 If the loop is incorrect, use the *load address compare* procedure with the MODE SELECT switch set to ADDRESS COMPARE PROGRAM STOP to stop at X'0122'. Then, following the program listing, use the instruction step procedure to locate the failure.

10 If the loop is correct, press the START push button to return to normal operation.

CHECK

Check to see that the initial test or first program module was loaded correctly. Use the *load address compare* procedure with the MODE SELECT switch set to ADDRESS COMPARE PROGRAM STOP to stop at address X'01FA.' This is the last ROS instruction before control is turned over to the next program. If this program stop occurs, it indicates that ROS is giving control to the next program correctly.

If the instruction test section of ROS is executed correctly, but control is not turned over to the next program correctly, check to see if the program loops within repeating major branches that match the list and indicate general areas of failure.

ROS repeating branches that may be caused by a channel adapter failure:

Repeating Branches	Probable Cause	Check the contents of		
		Reg.	Byte	Bit
00F6-00E8	Interface will not become enabled.	67	1	4
010E-0104	Cannot develop a level 1 or level 3 interrupt	60 67 76 77	0 0 1	0 5 4
011A-0124 0126-0110	A solid level 1 interrupt	76	0	5
012A-0144	A solid level 3 initial select interrupt occured	60 77	0 1	0 4
012C-01AA	A solid level 3 data service interrupt	60 77	0 1	0 4

Channel Checking (Part 2)

These steps indicate the general area of the program that should be checked for an apparent type 1 or type 4 channel adapter failure occurring after the CPU has issued an IPL command.

Use the *load address compare* procedure with the MODE SELECT switch set to ADDRESS COMPARE PROGRAM STOP to stop at the following addresses to determine to what extent the ROS program has completed the transfer of the first program or Initial Test.

Address X'0404'

This is the entry address for the initial test or first program. If this program stop occurs, refer to the initial test description in *IBM Maintenance Diagnostic Program 3705 Communications Controller On-Line Test and Internal Functional Test, D99-3705A,* or to the first program description, for additional information. The ROS program is no longer being executed.

Address X'01CA'

At this address, the program checks to verify that the IPL command was received. Register X'61', byte 1 contains the command.

Address X'0138'

Check the address that is requesting service. Register X'61' byte 0 should contain the single subchannel address that is requesting service.

Address X'01EA'

Compare the known byte count with the hardware byte count, after the initial test or first program data transfer. The contents of register 1 should equal the contents of register 5. Register 1 should contain a value of X'400' plus the byte count of the program (located in storage at X'0402'). Register 5 starts with a value of X'400' and increments by 2 as ROS loads the program, two bytes at a time.

The following status and sense combinations are developed by ROS for various conditions that occur when the ROS program is being executed:

0F Channel End, Device End, Unit Check, Unit Exception, and sense of IPL Required.

A byte count error occurred during the initial test or first program module transfer.

0E Channel End, Device End, Unit Check, sense of IPL Required, and Equipment Check

A false level 1 or level 3 interrupt occurred at initial selection time.

06 Device End, Unit Check, and Sense of IPL Required

Either an IPL is required because of normal conditions or a failure to recognize that the single subchannel is active.

00 Sense of IPL Required

A system reset has occurred.

TYPE 2 AND TYPE 3 CHANNEL ADAPTER

The instructions contained in ROS depend upon the type of channel adapter that is installed in the 3705. The ROS code enables the controller to load its control program across the channel.

Before the ROS code attempts the channel data transfer, it checks the functions and instructions it needs to complete the transfer. Tested are:

- Instructions
- Data path
- Channel adapter enable
- Channel adapter selection
- Channel adapter level 3 interrupt
- That the channel adapter received an IPL command
- That a level 1 or level 3 interrupt was received from the channel adapter

Only the portion of the instruction set needed to complete the transfer of the first program module across the channel is tested. The instructions tested are:

- ARI
- LRI
- ORI
- TRM
- LH
- STH
- ST
- BB
- BCL
- BZL
- B
- XR
- IN* X'52,55,58,59,5C,76,77,79,7D,7E'
- OUT* X'50,54,57,71,72,77,79'

*Those input and output instructions associated with the CA, and several of those necessary for CCU operations, are used but not thoroughly tested.

ROS checks the data path and uses some of the error detection circuits without testing them.

A listing of the ROS code is located in the ALDs, beginning on page CW201.

A flowchart showing the logical flow of ROS–channel adapter operations precedes the ROS listing in the ALDs.

SIMULATION RUN

Included with the ROS listing is a simulation run. The simulation run is a listing, in instruction execution order, showing the contents of the registers used.

Use the simulation run during instruction step procedures in the instruction test portion of ROS, as a check for correct operation.

ERROR ANALYSIS PROCEDURE

Type 2 ROS code presents error indications to the control panel for CCU and channel adapter errors. Observe the error indications and follow the prescribed course of action for each indication.

CONTROL PANEL SWITCHES

See page 2-070 if these lights are not on

During IPL, the MODE SELECT switch and the DIAGNOSTIC CONTROL switch must be in the PROCESS position for the indicators to function correctly. The STORE/LOAD COMPARE switch must be in the LOAD position.

INSTRUCTION TESTING

Before trying to load data across the channel, ROS code tests the preceding instructions. The general procedure for locating an instruction execution failure is to use the *instruction step* procedure to step through the failing section of the instruction test portion of the code.

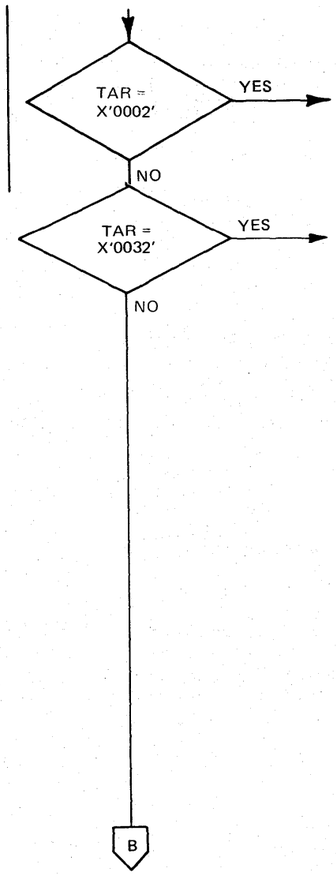
The simulation run, located following the ROS code listing in the ALDs, is to be used during the instruction step procedure as a check for correct operation.

The indications that appear on the control panel are:

IPL Phase III
Program Stop
Hard Stop
Load
Test

This is a CCU failure indication. TAR contains the address of the next instruction to be executed. This value is the address of the stop instruction +2. Check the contents of TAR against the following list. If it is equal to any value given, follow the indicated procedure.

See page 2-070 if these lights are not on

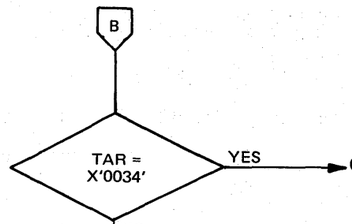


An invalid branch to zero has occurred.

An instruction failed to execute. Using the ROS listing and the simulation run, use the *load address compare* procedure with the MODE SELECT switch in ADDRESS COMPARE PROGRAM STOP to stop at various places in the program. Then use the *instruction step* procedure to step through, to locate the failure. Pick addresses at the beginning of test routines in the listing as stopping points.

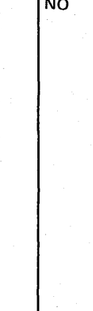
1. Set the MODE SELECT switch to ADDRESS COMPARE PROGRAM STOP.
2. Set the beginning address for one of the test routines in the ADDRESS/DATA switches. Refer to the ROS listing for the beginning addresses of the routines.
3. Retry the IPL.
4. If the same error occurs before the program stop, change the address in the ADDRESS/DATA switches to a previous address. The address of of the first instruction may be used, if necessary.
5. Retry until the program stop occurs.
6. When the program stops at the selected address, set the MODE SELECT switch to the INSTRUCTION STEP position.
7. Step through the code following the listing and the simulation run, to locate the error.

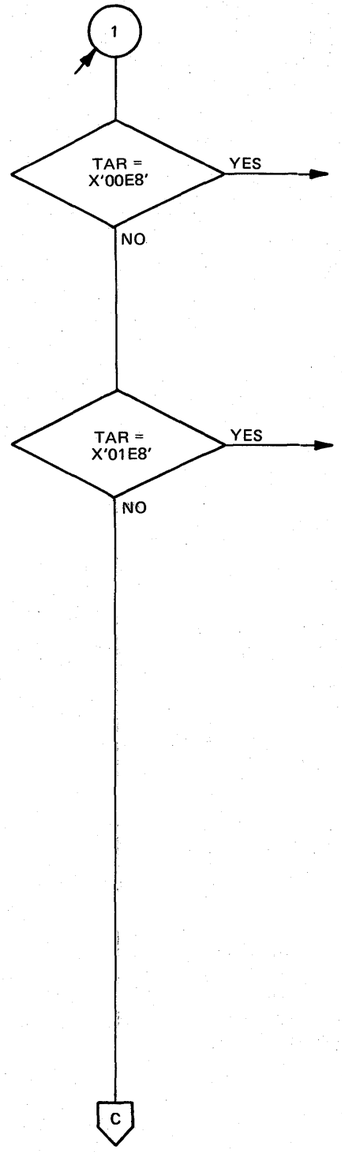
Instruction Testing (Part 2)



1. Set up the program stop at the beginning address of the Branch on Bit Test, (X'00A4'), from the ROS listing.
2. Retry the IPL
3. When the PROGRAM STOP light comes on, set the MODE SELECT switch to INSTRUCTION STEP.
4. Step through the test. Register 1 contains the instruction and indicates what is being tested. Bit 0.7 on indicates that byte 1 is being tested, and bit 0.7 off indicates that byte 0 is being tested. Bits 0.2, 0.3, and 1.0 are a binary indication of the bit that is being tested within the byte. The bits are being tested for "solid" on and off conditions.

Register 1		Bits Being Tested	
Byte 0 01234567	Byte 1 01234567	Byte 0 01234567	Byte 1 01234567
XX00XXX0	0XXXXXXX	10000000	00000000
XX00XXX0	1XXXXXXX	01000000	00000000
XX01XXX0	0XXXXXXX	00100000	00000000
XX01XXX0	1XXXXXXX	00010000	00000000
XX10XXX0	0XXXXXXX	00001000	00000000
XX10XXX0	1XXXXXXX	00000100	00000000
XX11XXX0	0XXXXXXX	00000010	00000000
XX11XXX0	1XXXXXXX	00000001	00000000
XX00XXX1	0XXXXXXX	00000000	10000000
XX00XXX1	1XXXXXXX	00000000	01000000
XX01XXX1	0XXXXXXX	00000000	00100000
XX01XXX1	1XXXXXXX	00000000	00010000
XX10XXX1	0XXXXXXX	00000000	00001000
XX10XXX1	1XXXXXXX	00000000	00000100
XX11XXX1	0XXXXXXX	00000000	00000010
XX11XXX1	1XXXXXXX	00000000	00000001



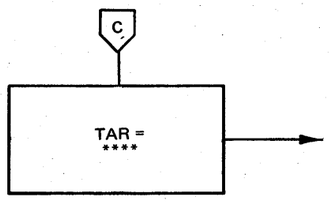


Address program stop at the continuity generation address.

Address	Register 5 Should be	Register 7 Should be
X'00EE'	X'FFFF'	X'FFFF'
X'00F0'	X'FF37'	X'FFFF'
X'01D8'	X'FF2F'	X'0018'
X'01DA'	X'FF2F'	X'0018'

If register 5 is wrong at a location, the check character generation failed in the preceding block of instructions. Check the instructions by using the *load address compare* procedure with the MODE SELECT switch in ADDRESS COMPARE PROGRAM STOP to stop at the beginning address of the failing block. Then compare the storage contents with the listing while using the *instruction step* procedure to step through the failing section.

Instruction Testing (Part 3)



If TAR contains an address that has not been previously defined, a program load or execution failure probably occurred. To verify that the program was loaded correctly, execute the ROS Data Transfer Test and the ROS Address Generation Test.

ROS Data Transfer Test

Display Main Storage Addresses

1. X'0032' — All bits should be off in display B. Suspect any bit that is on in the display as being continuously on from storage. (see 7-030). The bit can also be on continuously from ROS, (see 6-961).

2. X'0056' — All bits should be on in display B. Suspect any bit that is not on as being continuously off from storage, (see 7-030). The bit can also be continuously off, coming from ROS (see 6-961).

ROS Address Generation Test

Display Main Storage Addresses

1. X'0000' should contain X'7004'

If location X'0000' Contains	Suspect SAR Bit	See	
		3705-I	3705-II
X'F6FF'	15 on	7-030	7-260
X'98B8'	14 on	7-030	7-260
X'810B'	13 on	7-030	7-260
X'0082'	12 on	7-030	7-260
X'0492'	11 on	7-030	7-260
X'F1FF'	10 on	7-030	7-260
X'1305'	9 on	7-030	7-260
X'5774'	8 on	7-030	7-260

2. X'01FE' should contain X'0404'

If location X'01FE' Contains	Suspect SAR Bit	See	
		3705-I	3705-II
X'0400'	15 off	7-030	7-260
X'8FF8' or X'FE80'	14 off	7-030	7-260
X'A800'	13 off	7-030	7-260
X'1007'	12 off	7-030	7-260
X'81F8'	11 off	7-030	7-260
X'31C8'	10 off	7-030	7-260
X'F982'	9 off	7-030	7-260
X'8788'	8 off	7-030	7-260

Note: Only SAR bits 8 through 15 are used to address low storage. The other bits are not used.

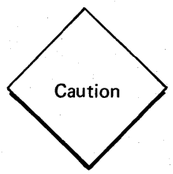
These charts are valid only for intermittent errors. ROS must load into storage correctly at least one time out of a number of LOAD push button operations for these charts to be valid. Otherwise, use manual store and display, 1-140, to determine an addressing problem.

If no discrepancy has been found in the ROS Data Transfer Test or the ROS Address Generation Test, check to verify that the control panel switches are set correctly and retry the IPL.

CHANNEL CHECKING

Indication:
IPL Phase III
Load
Program Display

This may be a channel adapter failure or it may indicate that some external action is necessary.



The DISPLAY/FUNCTION SELECT switch *must not* be in the STATUS or TAR & OP position, to get correct displays

The following displays that appear in display B indicate the probable failing condition.

Value in Display B

X'0001' The program is looping because the channel adapter could not be selected. The CA is selected by an Output X'57' instruction with byte 1, bit 4 on, in the register designated by, in the instruction. This sets the 'CA selected' latch in the CA mode register (CAMR), QH001. See 9-080 for additional CA selection information. (See the section labeled ROS 04 in the listing.)

The channel adapter mode is sensed by an Input X'55' instruction. When the CA is selected ('CA selected' latch set), byte 1, bit 7 will be returned to the CCU on the Inbus (see QH006 and 9-190 for additional information).

X'0002' The program is looping because the channel adapter interface was not enabled. Enable the interface using the procedure on 1-120. Display register X'58', byte 1, bit 4 or 5 should be on if an interface is enabled (label ROS 05 in the listing).

X'0004' The program is looping, waiting for a CA level 1 or level 3 interrupt that should have been set by the CA when CA1 mode was set by the program. The label ROS 03 in the ROS code listing is the beginning of the section in which the program is looping.

Value in Display B

X'0008' The program is looping, waiting for a level 3 interrupt from an IPL command or a level 1 interrupt indicating a CA error when the IPL command was received. The label ROS 16 in the ROS code listing is the beginning address of the routine in which the program is looping.

X'0402' The program is looping, waiting for a CA level 1 or level 3 interrupt indicating initial test or first program data transfer is completed. (see the section labeled ROS 19 in the listing).

X'0408' This is the same as loop X'0008' except that the "04" indicates that a level 1 interrupt occurred during the initial test or first program data transfer.

Indication:
IPL Phase III
Load

This indicates that communications between the channel adapter and the host CPU should be checked using OLTEP or OLTSEP with OLTs, IFTs, or initial test. User programs may be used, if necessary.

If a problem is indicated during the IPL (05) command data transfer, check the status returned and compare it with the following chart, to determine the problem condition.

If the status presented to the channel is:

0F CHANNEL END, DEVICE END, UNIT CHECK, UNIT EXCEPTION and SENSE of IPL required.

A byte count error occurred during the initia test (or first program) module transfer.

0E CHANNEL END, DEVICE END, UNIT CHECK and SENSE of IPL REQUIRED.

IPL, HIO or interface stop was issued during initial test or first program data transfer.

06 DEVICE END and UNIT CHECK with SENSE of IPL REQUIRED

Normal response when IPL request is initiated at the 3705 or failure to recognize that the single subchannel is active.

00 SENSE of IPL required.

A system or selective reset has occurred.

Indication:
Load

ROS code has turned over control either to initial test or first customer program at address X'0404'. (See "Initial Test" in :

IBM Maintenance Diagnostic Program
IBM 3705 Communications Controller
On-Line Test and Wrap All Lines Test, D99-3705C.

IBM Maintenance Diagnostic Program
IBM 3705 Communications Controller
Internal Functional Test Loader,
Diagnostic Control Panel Line Test, and
Initial Test, D99-3705D.

IBM Maintenance Diagnostic Program
IBM 3705 Communications Controller
Internal Functional Test Symptom Indexes, D99-3705E.

To verify that the ROS program is no longer in control, set the switches to address compare stop at X'0404'. If this stop occurs, the ROS program is no longer being executed.

DUAL CHANNEL ADAPTERS

The dual channel adapters ROS code enables the controller to load its control program across either channel. The instructions contained in ROS depend upon the type of channel adapters installed in the 3705.

Before the ROS code attempts the channel data transfer, it checks the functions and instructions it needs to complete the transfer. Tested are:

- Instructions
- Data path
- Channel adapter enable
- Channel adapter selection
- Channel adapter level 3 interrupt
- Receipt of an IPL command by the channel adapters
- Receipt of a level 1 or level 3 interrupt from the channel adapters

Only the portion of the instruction set needed to complete the transfer of the first program module across the channel is tested. The instructions tested are:

- ARI
- LRI
- ORI
- TRM
- LH
- STH
- ST
- BB
- BCL
- BZL
- B
- XR
- IN* X'52,55,58,59,5C,76,77,79,7D,7E'
- OUT* X'50,54,57,71,72,77,79'

If CA 1 is a type 1 or type 4, the following instructions are also used;

- IN* X'60,61,62,64,67'
- OUT* X'62,63,64,66,67'

*Those input and output instructions associated with the CA, and several of those necessary for CCU operations, are used but not thoroughly tested.

ROS checks the data path and uses some of the error detection circuits without testing them.

A listing of the ROS code is located in the ALDs, beginning of page CW401.

A flowchart showing the logical flow of ROS—channel adapter operations precedes the ROS listing in the ALDs.

SIMULATION RUN

Included with the ROS listing is a simulation run. The simulation run is a listing, in instruction execution order, showing the contents of the registers used.

The simulation run, located with the ROS code listing in the ALDs, is to be used during the instruction step procedure as a check for correct operation.

ERROR ANALYSIS PROCEDURE

Dual ROS code presents error indications to the control panel for CCU and channel adapter errors. Observe the error indications and follow the prescribed course of action for each indication.

CONTROL PANEL SWITCHES

During IPL, the MODE SELECT switch and the DIAGNOSTIC CONTROL switch must be in the PROCESS position for the indicators to function correctly. The STORE/LOAD COMPARE switch must be in the LOAD position.

INSTRUCTION TESTING

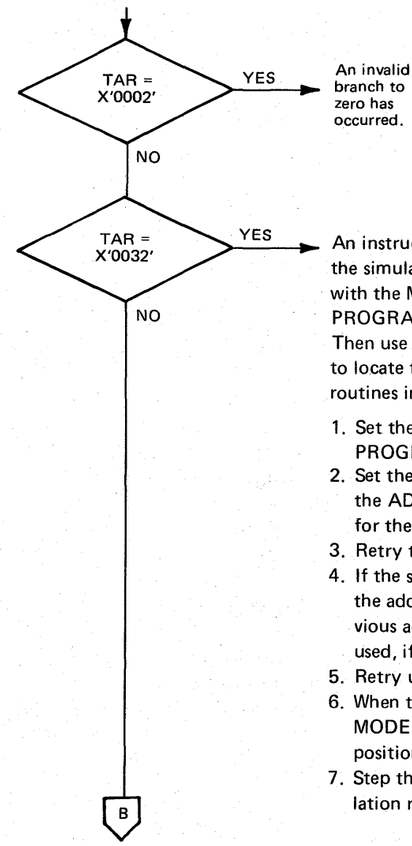
Before trying to load data across the channel, ROS code tests the previously listed instructions. The general procedure for locating an instruction execution failure is to use the *instruction step* procedure to step through the failing section of the instruction test portion of the code.

The indications that appear on the control panel are:

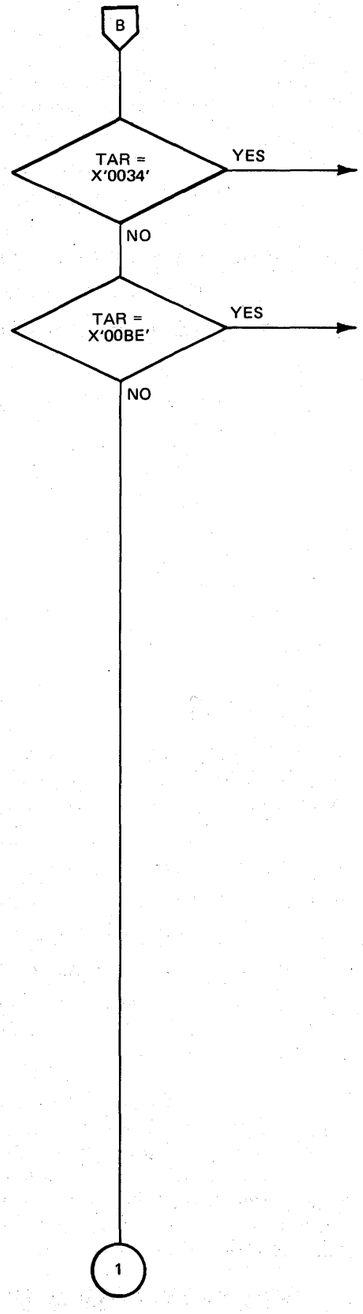
IPL Phase III
Program Stop
Hard Stop
Load
Test

This is a CCU failure indication. TAR contains the address of the next instruction to be executed. This value is the address of the stop instruction +2. Check the contents of TAR against the following list. If it is equal to any value given, follow the indicated procedure.

See pages 2-110 if these lights are not on.



Instruction Testing (Part 2)

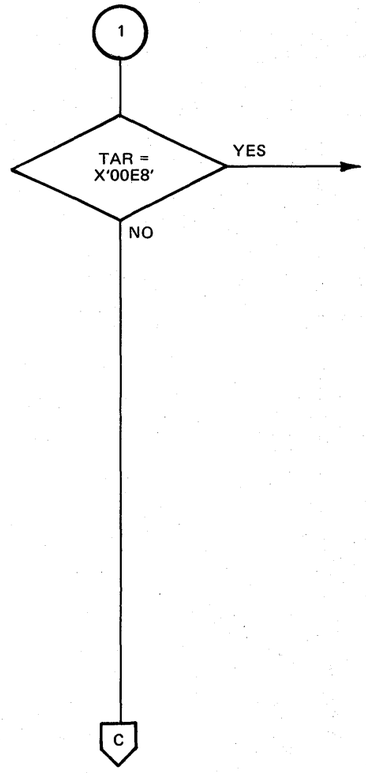


Output instruction failure.

A branch on bit failure or 'Z' latch failing to set caused this hard stop condition.

1. Set up the program stop at the beginning address of the Branch on Bit Test, (X'00A4'), from the ROS listing.
2. Retry the IPL.
3. When the PROGRAM STOP light comes on, set the MODE SELECT switch to INSTRUCTION STEP.
4. Step through the test. Register 1 contains the instruction and indicates what is being tested. Bit 0.7 on indicates that byte 1 is being tested, and bit 0.7 off indicates that byte 0 is being tested. Bits 0.2, 0.3, and 1.0 are a binary indication of the bit that is being tested within the byte. The bits are being tested for "solid" on and off conditions.

Register 1		Bits Being Tested	
Byte 0 0 1 2 3 4 5 6 7	Byte 1 0 1 2 3 4 5 6 7	Byte 0 01234567	Byte 1 01234567
XX 0 0 XXX 0	0XXXXXXX	10000000	00000000
XX 0 0 XXX 0	1XXXXXXX	01000000	00000000
XX 0 1 XXX 0	0XXXXXXX	00100000	00000000
XX 0 1 XXX 0	1XXXXXXX	00010000	00000000
XX 1 0 XXX 0	0XXXXXXX	00001000	00000000
XX 1 0 XXX 0	1XXXXXXX	00000100	00000000
XX 1 1 XXX 0	0XXXXXXX	00000010	00000000
XX 1 1 XXX 0	1XXXXXXX	00000001	00000000
XX 0 0 XXX 1	0XXXXXXX	00000000	10000000
XX 0 0 XXX 1	1XXXXXXX	00000000	01000000
XX 0 1 XXX 1	0XXXXXXX	00000000	00100000
XX 0 1 XXX 1	1XXXXXXX	00000000	00010000
XX 1 0 XXX 1	0XXXXXXX	00000000	00001000
XX 1 0 XXX 1	1XXXXXXX	00000000	00000100
XX 1 1 XXX 1	0XXXXXXX	00000000	00000010
XX 1 1 XXX 1	1XXXXXXX	00000000	00000001

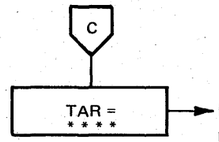


A level 1 interrupt was requested by other than an IPL level 1 interrupt request. The IPL request was expected. Other conditions that could have caused the interrupt are:

Condition:

Address Compare
Adapter Check
In/Out Check
Address Exception
Protect Check

Instruction Testing (Part 3)



If TAR contains an address that has not been previously defined, a program load or execution failure probably occurred. To verify that the program was loaded correctly, execute the ROS Data Transfer Test and the ROS Address Generation Test.

ROS Data Transfer Test

Display Storage Addresses

1. X'0032' All bits should be off in display B. Suspect any bit that is on in the display as being continuously on from storage. (See 7-030.) The bit can also be on continuously from ROS, (see 6-971).
2. X'0056' All bits should be on in display B. Suspect any bit that is not on as being continuously off from storage, (see 7-030). The bit can also be continuously off, coming from ROS (see 6-971).

ROS Address Generation Test

Display Storage Addresses

1. X'0000' should contain X'7004'

If location X'0000' Contains	Suspect SAR Bit	See	
		3705-I	3705-II
X'F6FF'	15 on	7-030	7-260
X'98B8'	14 on	7-030	7-260
X'810B'	13 on	7-030	7-260
X'0082'	12 on	7-030	7-260
X'0492'	11 on	7-030	7-260
X'F1FF'	10 on	7-030	7-260
X'1305'	9 on	7-030	7-260
X'8280'	8 on	7-030	7-260
X'5174' or X'D034'	7 on	7-030	7-260

2. X'03FE' should contain X'0400'

If location X'03FE' Contains	Suspect SAR Bit	See	
		3705-I	3705-II
X'8C80' or X'8FF8'	15 off	7-030	7-260
X'A808' or X'001C'	14 off	7-030	7-260
X'D720' or X'8004'	13 off	7-030	7-260
X'8780' or X'719C'	12 off	7-030	7-260
X'9817' or X'6124'	11 off	7-030	7-260
X'614C'	10 off	7-030	7-260
X'C910' or X'C9FD'	9 off	7-030	7-260
X'C814' or X'E8B6'	8 off	7-030	7-260
X'EC8C' or X'11C8'	7 off	7-030	7-260

Note: Only SAR bits 7 through 15 are used to address low storage. The other bits are not used.

These charts are valid only for intermittent errors. ROS must load into storage correctly at least one time out of a number of LOAD pushbutton operations for these charts to be valid. Otherwise, use manual store and display, 1-140, to determine an addressing problem.

If no discrepancy has been found in the ROS Data Transfer Test or the ROS Address Generation Test, check to verify that the control panel switches are set correctly and retry the IPL.

CHANNEL CHECKING

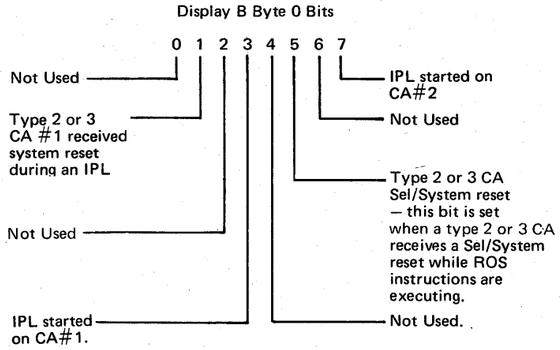
Indication:
IPL Phase III
Load
Program Display

This may be a channel adapter failure or it may indicate that some external action is necessary.

CAUTION

The DISPLAY/FUNCTION SELECT switch *must not* be in the STATUS or TAR & OP position, to get correct displays.

The displays that appear in display B indicate the following conditions:



IPL Phase III Load Program Display

This indicates that communications between the channel adapters and the host CPUs should be checked, using OLTEP or OLTSEP with initial test, OLTs or IFTs. The customer's first program may be used if desired. Refer to the status and sense information chart at the end of this section if CA operation is possible but the load operation is not successful. If CA operation is not possible, proceed with the CA ROS checkout routines.

If the instruction testing has been completed, try the channel adapter ROS checkout routines when there is a problem.

Channel Adapter ROS Checkout Routine #1

1. Disable all channel interfaces. Verify that the control panel INTERFACE ENABLED lights are off.
2. Press the RESET push button.
3. Press the LOAD push button.
4. Display B should indicate all zeros while ROS loops through the interrupt wait loop starting at label DROS15 in the program listing.
5. If the display is not correct, one of the following problems is indicated:
   - An interface remained enabled.
   - An incorrect branch occurred.
   - Contents of storage is incorrect.
   - A channel adapter malfunctioned.

To Locate A Failure

Use the Load Address Compare procedure with the mode select switch set to ADDRESS COMPARE PROGRAM STOP. Select the stop address according to the adapter. Follow the ROS listing using the Instruction Step procedure to determine the failing condition.

Adapter	Adapter Type	ROS Program Listing Label
CA Frame #1	Type 1 or 4	DROS30
CA Frame #1	Type 2 or 3	DROS03
CA Frame #2	Type 2 or 3	DROS086

Channel Adapter ROS Checkout Routine # 2

1. If the display and ROS loop are correct in step 4 of routine 1, enable either or both interfaces.
2. CAUTION

   This causes a Device End-Unit Check asynchronous status to be presented to the attached channel which has been enabled if an IPL has not started on the other channel with both channels enabled.
3. Until an IPL command (X'05') is detected by a CA1 or CA2, the only branch is from X'01CC' to X'01B4' or X'01BO'.
4. If any other repeating branch occurs, check the following list for general areas of channel adapter operation.

Repeating Branches	Probable Cause	Check the Contents of Reg	Byte	Bit
01B6-01D4 or 01B4-01D4	Solid CA1 Level 1 interrupt	76	0	5
01BA-01DC or 01B8-01E8	Solid CA2 Level 1 interrupt	76	0	6
01C2-01CE	Type 1 CA not enabled	67	1	4
01C6-0162 or 01C6-0166	Solid CA1 Level 3 interrupt (Type 2 or 3 CA1 not enabled and IPL not started on CA2)	77	1	4
0166-02E8 or 016A-02E4	Solid type 1 CA initial selection Level 3 interrupt	60	0	0-7
01C8-0178 or 01C8-017C	Solid type 1 CA data/status Level 3 interrupt	77 62 62	1 0 1	3 0-7 0-4
01CA-01FE or 01CA-0224	Solid CA2 Level 3 interrupt (CA2 not enabled and IPL not started on CA1)	77	1	2
Any address greater than 03FE	A branch out of ROS code occurred.			

Channel Adapter ROS Checkout Routine # 3

The following stop addresses provide checkpoints to determine the extent of IPL command completion.

Use the Load Address Compare procedure with the mode select switch set to ADDRESS COMPARE PROGRAM STOP to determine whether the described conditions occur.

Address X'0404'

This is the entry address for the initial test or first program. If this program stop occurs, refer to the initial test description in *IBM Maintenance Diagnostic Program IBM 3705 Communications Controller Internal Functional Test Loader, Diagnostic Control Module, Initial Test, and Panel Line Test, D99-3705D,* or to the first program description, for additional information. The ROS program is no longer being executed.

Label DROS55 *for type 1 or type 4* CA Frame #1 ONLY

Compare the known byte count with the hardware byte count, after the initial test or first program data transfer. The contents of register 1 should equal the contents of register 5. Register 1 should contain a value of X'400' plus the byte count of the program (located in storage at X'0402'). Register 5 starts with a value of X'400' and increments by 2 as ROS loads the program, two bytes at a time.

Label DROS50 *for type 1 or type 4* CA Frame #1 ONLY

An IPL command was received. Register X'61' Byte 1 contains the command.

Label DROS33 *for type 1 or type 4* CA Frame #1 ONLY

Check the address that is requesting service. Register X'61' Byte 0 should contain the native subchannel address.

Label DROS25 *for type 2 or 3* CA Frame #1 or CA Frame #2

Compare the hardware and program byte counts after the IPL data transfer. The contents of register 3 should equal the contents of register 5. Register 5 contains the program byte count (located at storage address X'0402') plus one and Register 3 contains a hardware byte count.

Label DROS245 *for type 2 or 3* CA Frame #1 ONLY

An IPL command has been received on CA1.

Label DROSZ415

(If listing does not include Label DROSZ415, use address X'0226' instead.)

An IPL command has been received on CA Frame #2. The following status and sense combinations are developed by ROS for various conditions that occur when the ROS program is being executed:

0F Channel End, Device End, Unit Check, Unit Exception, and sense of IPL Required.

A byte count error occurred during the initial test or first program module transfer.

0E Channel End, Device End, Unit Check, sense of IPL Required, and Equipment Check. (Equipment Check is present only if CA1 is a type 1.)

A false level 1 or level 3 interrupt occurred at initial selection time.

06 Device End, Unit Check, and Sense of IPL Required

Either an IPL is required because of normal conditions or, on a type 1 CA1, the single subchannel is not recognized as being active.

00 Sense of IPL Required

Status and sense is presented to a Sense command following a system reset, and IPL has not begun on other channel adapter.

Special Status Conditions to Handle Dual Channel IPL Contention

When an IPL has been started on one channel, a sense command issued by the other channel will receive an initial status of Unit Exception from a type 2 or 3 CA or an immediate final status of Channel End, Device End and Unit Exception from a type 1 or type 4 CA.
If an IPL on one channel fails to end within an allotted period of time, it may be overridden by an IPL on the other channel. The original IPL then ends with Channel End, Device End, and Unit Check.

N ROS TEST

N-CHANNEL ROS FOR THE TYPE 4 CA

The N-channel ROS is used when one to four type 4 CAs are installed without the IPL switch on the control panel and the control program is 'Advanced Communications Function for Network Control Program/VS'.

The N-channel ROS code allows the loading of the control program to occur across any installed type 4 CA. The N-channel ROS code:

1 Tests the CCU instructions.
2 Selects and enables the installed type 4 CAs.
3 Scans the installed type 4 CAs for an IPL command then begins the IPL on the CA with the IPL command.
4 Continuously scans each type 4 CA for interrupts.
5 Prepares each CA having an active command and while no IPL is in progress sends a final ending status of 'CE, DE, UC' with a sense byte of 'not initialized'.
6 Prepares each CA not having an active command and while no IPL is in progress sends an asynchronous status of 'DE, UC' with a sense byte of 'not initialized'.
7 Sends an ending status of 'CE, DE' to a Sense command if an IPL is not in progress.
8 Begins loading the control program through the first type 4 CA that ROS recognizes as having received an IPL command.
9 Prepares the other CAs to respond with an ending status of 'CE, DE, UE' to Sense commands once an IPL is in progress on any CA.
10 Allows a subsequent IPL command to override an existing IPL command in progress. A new IPL operation begins with the subsequent IPL command that can occur on any channel.
11 Handles all type 4 CA interrupts until control is passed to the loader.

Before the ROS code attempts to transfer the data, it checks the functions and instructions it needs to complete the transfer. Tested are:

- Instructions
- Data path
- Channel adapter enable
- Channel adapter selection
- Channel adapter level 3 interrupt
- Receipt of an IPL command on each enabled channel adapter
- That a level 1 or level 3 interrupt was received from the channel adapter

Only the portion of the instructions needed to complete the transfer of the first program module across the channel is tested. The instructions tested are:

- ARI
- LRI
- ORI
- TRM
- LH
- STH
- ST
- BB
- BCL
- BZL
- B
- XR
- IN *, X'60,61,62,64,67,76,77,79,7D,7E'
- OUT *, X'60',62,63,64,66,67,77,79'

*Those input and output instructions associated with the CA and several of those necessary for CCU operation are used but are not thoroughly tested.

ROS checks the data path and uses some of the error detection circuits without testing them.

A listing of the ROS code is in the ALD's beginning on CW501. A flowchart showing the logical flow of ROS-channel adapter operations precedes the ROS listing in the ALDs (CW500).

SIMULATION RUN

The simulation run starts on CW301.
The simulation run is a listing in instruction execution order showing the contents of the registers used.

Use the simulation run during instruction step procedures in the instruction test portion of ROS as a check for correct operation.

ERROR ANALYSIS PROCEDURE

N ROS code presents error indications to the control panel for CCU and channel adapter errors. Observe the error indications and follow the prescribed course of action for each indication.

CONTROL PANEL SWITCHES

During the IPL, the MODE SELECT switch and the DIAGNOSTIC CONTROL switch must be in the PROCESS position for the indicators to function correctly.

INSTRUCTION TESTING

Before trying to load data across the channel, ROS Program code tests the preceding instructions. The general procedure for locating an instruction execution failure is to step the instructions through the failing section of the instruction test portion of the code.

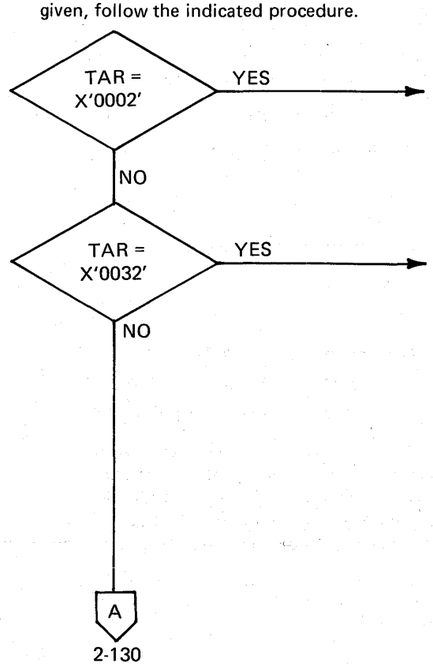
The simulation run following the ROS code listing in the ALD is to be used during the instruction step procedure as a check for correct operation.

The indications that appear on the control panel are:

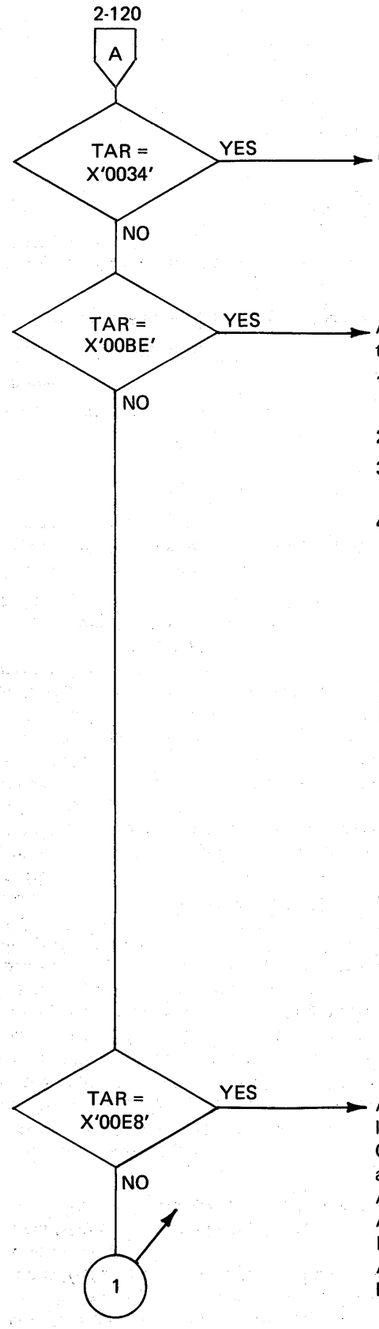
IPL Phase III
Program Stop
Hard Stop
Load
Test

This is a CCU failure indication. TAR contains the address of the next instruction to be executed. This value is the address of the stop instruction +2. Check the contents of TAR against the following list; if it is equal to any value given, follow the indicated procedure.

See page 2-020
If these lamps are not on.



1 Set the MODE SELECT switch to ADDRESS COMPARE PROGRAM STOP.
2 Set the beginning address for one of the test routines in the ADDRESS/DATA switches. Refer to the ROS listing for the beginning addresses of the routines.
3 Retry the IPL.
4 If the same error occurs before the program stop, change the address in the ADDRESS/DATA switches to a previous address. The address of the first instruction may be used if necessary.
5 Retry until the program stop occurs.
6 When the program stops at the selected address, set the MODE SELECT switch to INSTRUCTION STEP.
7 Step through the code, following the listing and the simulation run, to locate the error. (See CW000.)



Output instruction failure.

A branch on bit failure or 'Z' latch failing to set caused this hard stop condition.

1 Set up to program stop at the beginning address of the Branch on Bit Test (X'00A4') from the ROS listing.

2 Retry the IPL.

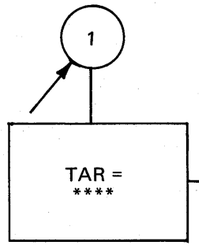
3 When the Program Stop light comes on, set the MODE SELECT switch to INSTRUCTION STEP.

4 Step though the test. Register 1 contains the instruction and indicates what is being tested. Bit 0.7 on indicates that byte 1 is being tested, and bit 0.7 off indicates that byte 0 is being tested. Bits 0.2, 0.3, and 1.0 are a binary indication of the bit being tested within the byte. The bits are being tested for "solid" on and off conditions.

Register 1		Bits Being Tested	
Byte 0	Byte 1	Byte 0	Byte 1
0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	01234567	01234567
XX00XXX0	0XXXXXXX	10000000	00000000
XX00XXX0	1XXXXXXX	01000000	00000000
XX01XXX0	0XXXXXXX	00100000	00000000
XX01XXX0	1XXXXXXX	00010000	00000000
XX10XXX0	0XXXXXXX	00001000	00000000
XX10XXX0	1XXXXXXX	00000100	00000000
XX11XXX0	0XXXXXXX	00000010	00000000
XX11XXX0	1XXXXXXX	00000001	00000000
XX00XXX1	0XXXXXXX	00000000	10000000
XX00XXX1	1XXXXXXX	00000000	01000000
XX01XXX1	0XXXXXXX	00000000	00100000
XX01XXX1	1XXXXXXX	00000000	00010000
XX10XXX1	0XXXXXXX	00000000	00001000
XX10XXX1	1XXXXXXX	00000000	00000100
XX11XXX1	0XXXXXXX	00000000	00000010
XX11XXX1	1XXXXXXX	00000000	00000001

X = don't care

A level 1 interrupt was requested by other than an IPL level 1 interrupt request. The IPL request was expected. Other conditions that could have caused the interrupt are:
Address compare
Adapter check
In/out check
Address exception
Protect check



If TAR contains an address that has not been previously defined, a program load or execution failure probably occurred. To verify the program was loaded correctly, execute the ROS Data Transfer Test and the ROS Address Generation Test.

ROS Data Transfer Test

Display main storage addresses

1 location X'0032' → All bits should be off in Display B. Suspect any bit that is on in the display as being continuously on from storage (see 7-030 or 7-260). The bit can also be continuously on from ROS, (see 6-961).

2 location 0056 → All bits should be on in Display B. Suspect any bit that is not on as being continuously off from storage (see 7-030 or 7-260). The bit can also be continuously off coming from ROS, (see 6-961).

ROS Address Generation Test

Display main storage addresses

1 X'0000' should contain X'7004' →

If location X'0000' contains	Suspect SAR Bit	3705-II. See
X'F6FF'	15 on	7-260
X'98B8'	14 on	7-260
X'810B'	13 on	7-260
X'0082'	12 on	7-260
X'0492'	11 on	7-260
X'F1FF'	10 on	7-260
X'1305'	9 on	7-260
X'66C8'	8 on	7-260
X'4303'	7 on	7-260

2 X'03FE' should contain X'03E8' →

If location X'03FE' contains	Suspect SAR Bit	See
X'0708'	15 off	7-260
X'0006'	14 off	7-260
X'0608'	13 off	7-260
X'0002'	12 off	7-260
X'7004'	11 off	7-260
X'7004'	10 off	7-260
X'003C'	9 off	7-260
X'717C'	8 off	7-260
X'88DB'	7 off	7-260

These charts are valid only for intermittent errors. ROS must load into storage correctly at least one time out of a number of Load pushbutton operations, for these charts to be valid. Otherwise, use control panel and display procedures (1-140) to determine if there is an addressing problem.

NOTE: Only SAR bits 7 through 15 are used to address low storage. The other SAR bits are not used.

If no discrepancy has been found in the ROS Data Transfer or Address Generation Test, verify that the control panel is set up properly and re-try the IPL.

CHANNEL CHECKING (Part 1)

IPL Phase III Load

This is an indication that communications between the channel adapter and the host CPU should be checked, using OLTEP or OLTSEP with the initial test, OLTs or IFTs. The customer's first program may be used if desired. Refer to the status and sense information chart at the end of this section if CA operation is possible but the load operation is not successful. If CA operation is not possible, proceed with the CA ROS checkout routines.

If the instruction testing has been completed, try the type 4 channel adapter N ROS checkout routine when there is a problem.

Type 4 Channel Adapter N ROS Checkout Routine

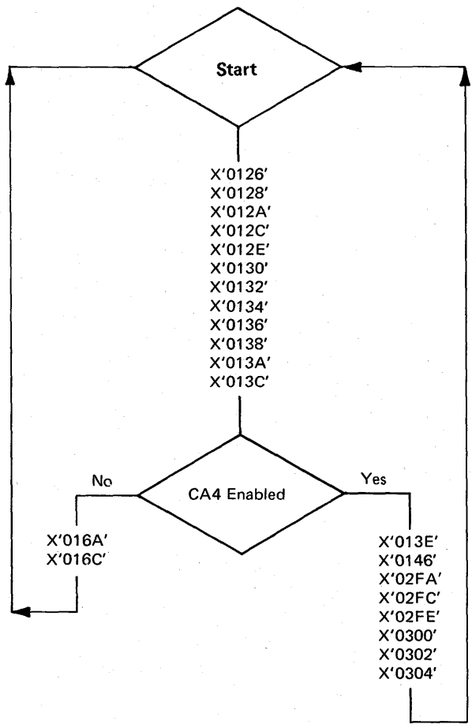
1. Disable all channel interfaces. Verify that the control panel INTERFACE ENABLED lights are off.
2. Press the RESET PUSH BUTTON.
3. Press the LOAD push button.
4. Press the STOP push button.
5. Set the MODE SELECT switch to INSTRUCTION STEP.
6. Set the DISPLAY/FUNCTION select switch to TAR & OP REGISTER.
7. Press the START push button. Observe the address in display A.
8. Press the START push button several more times and observe the program looping through addresses X'0126', X'0128', X'012A', X'012C', X'012E', X'0130', X'0132', X'0134', X'0136', X'0138', X'013A', X'013C', X'016A' and X'016C'.
9. If this loop is not being executed, one of the following problems is indicated:
   - An interface remained enabled.
   - An incorrect branch occurred
   - Contents of storage is incorrect.

To locate the failure

10. Use the *load address compare* procedure with the MODE SELECT switch set to ADDRESS COMPARE PROGRAM STOP to stop at X'0126'. Then follow the ROS listing using the instruction step procedure.

    Observe the normal program loop while the 3705 is waiting for initial selection. The host must be *unable* to select the 3705 for an IPL.

1. Enable one or more interfaces. When an interface is enabled, ROS code may cause IPL phase 1 and 2 if certain conditions are present.
2. Press the CHECK RESET push button.
3. Press the LOAD push button. Verify that the correct interface enabled lights come on.
4. Press the STOP push button.
5. Set the MODE SELECT switch to INSTRUCTION STEP.
6. Set the DISPLAY/FUNCTION SELECT switch to TAR & OP REGISTER.
7. Press the START push button. Observe the address in display A. With the LOAD light on, continue to press the START push button to display the loop.



8. Set the MODE SELECT switch to PROCESS.
9. If the loop is incorrect, use the *load address compare* procedure with the MODE SELECT switch set to ADDRESS COMPARE PROGRAM STOP to stop at X'0126'. Then, following the program listing, use the instruction step procedure to locate the failure.
10. If the loop is correct, press the START push button to return to normal operation.

CHECK

Check to see that the initial test or first program module was loaded correctly. Use the *load address compare* procedure with the MODE SELECT switch set to ADDRESS COMPARE PROGRAM STOP to stop at address X'037C'. This is the last ROS instruction before control is turned over to the next program. If this program stop occurs, it indicates that ROS is giving control to the next program correctly.

Channel Checking (Part 2)

These steps indicate the general area of the program that should be checked for an apparent type 4 channel adapter failure occurring after the CPU has issued an IPL command.

Use the *load address compare* procedure with the MODE SELECT switch set to ADDRESS COMPARE PROGRAM. STOP to stop at the following addresses to determine to what extent the ROS program has completed the transfer of the first program or Initial Test.

Address X'0404'

This is the entry address for the initial test or first program. If this program stop occurs, refer to the initial test description in *IBM Maintenance Diagnostic Program 3705 Communications Controller On-Line Test and Internal Functional Test, D99-3705A,* or to the first program description, for additional information. The ROS program is no longer being executed.

Address X'0268'

At this address, the program checks to verify that the IPL command was received. Register X'61', byte 1 contains the command.

Address X'01AE'

Check the address that is requesting service. Register X'61' byte 0 should contain the single subchannel address that is requesting service.

Address X'0364'

Compare the known byte count with the hardware byte count, after the initial test or first program data transfer. The contents of register 1 should equal the contents of register 5. Register 1 should contain a value of X'400' plus the byte count of the program (located in storage at X'0402'). Register 5 starts with a value of X'400' and increments by 2 as ROS loads the program, two bytes at a time.

The following status and sense combinations are developed by ROS for various conditions that occur when the ROS program is being executed:

0F Channel End, Device End, Unit Check, Unit Exception, and sense of IPL Required.

A byte count error occurred during the initial test of first program module transfer.

0E Channel End, Device End, Unit Check, sense of IPL Required, and Equipment Check

A false level 1 or level 3 interrupt occurred at initial selection time.

06 Device End, Unit Check, and Sense of IPL Required

Either an IPL is required because of normal conditions or a failure to recognize that the single subchannel is active.

00 Sense of IPL Required

A system reset has occurred.

B4S2

B4J2

B4K2

B_4N_2

CENTRAL CONTROL UNIT

CAUTION

Touching the pin side of the CCU board while the 3705 is running can cause CCU errors.

The Central Control Unit (CCU) contains all the circuits and data flow paths necessary to execute the instruction set and to control storage and the attached adapters. The CCU, controlled by a program in storage, contains 32 general registers and various hardware registers that the control program uses for instruction execution and data handling.

The CCU can execute 51 instructions, which can be used to transfer data from one register to another, to store data from a register in 3705 storage, to load data from storage into a register, and to perform various arithmetic and hardware functions. Some of the CCU hardware registers can be addressed as external registers by 'input' and 'output' instructions. (The 'input' or 'output' instruction is indicated beside the register in the data flow on page 6-020.)

The 3705 has a basic 16-bit address structure. When a 3705 has more than 48K (3705-I) or 64K (3705-II) bytes of storage, additional address bits are needed. The additional bits are designated as byte X, bit 4, 5, 6 and 7. The addition of byte X is referred to as the Extended Addressing feature.

Each program, CCU, or adapter request has an assigned priority for use of the CCU. When any control program or hardware function requests use of the 3705 (an interrupt request), the priority system determines when the CCU will handle the interrupt request.

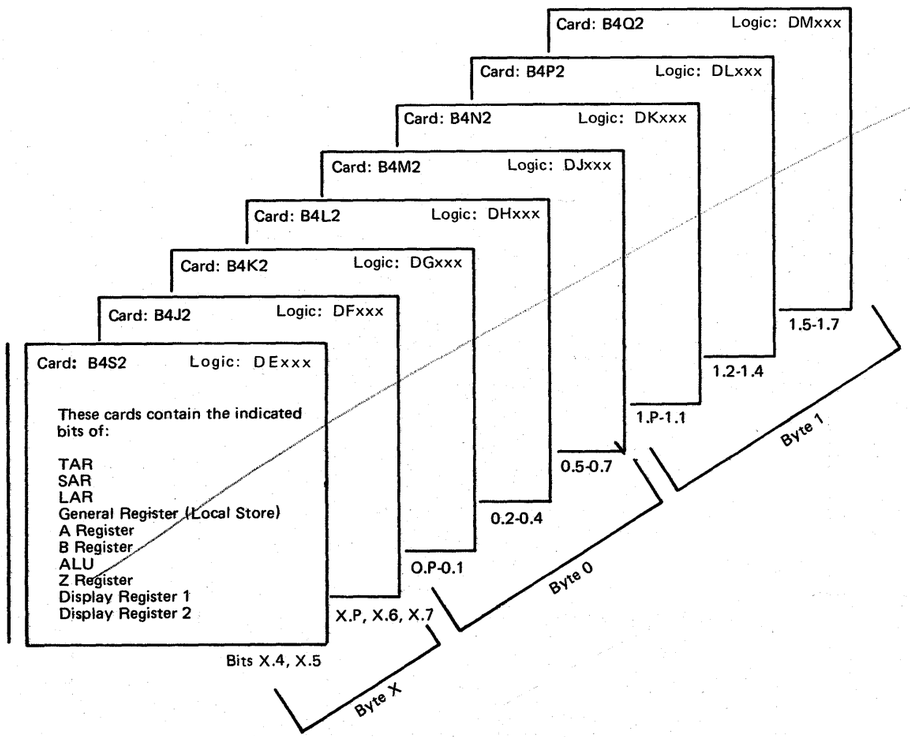
Each of the interrupt requests is assigned to one of five program levels. Program level 1 has the highest priority and program level 5, the lowest. The machine priority controls determine when an interrupt can occur.

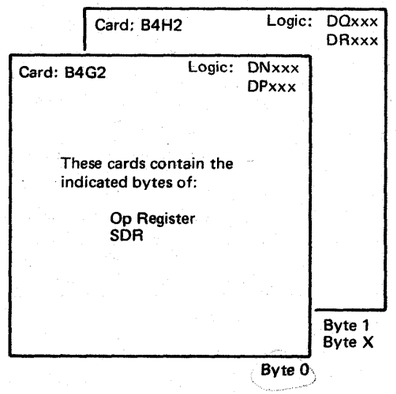
The CCU has a storage protection mechanism that monitors attempts either to modify storage or to execute instructions in protected storage. Storage protection causes a check when the contents of storage are accessed for unauthorized modification.

Page 6-020 shows the general data flow for the CCU. Data flow for a particular operation is determined by the instruction, cycle steal, or control operation being performed.

Abbreviations Used in This Section

ALU	– Arithmetic Logic Unit
CUCR	–Cycle Utilization Counter Register
IAR	– Instruction Address Register
LAR	– Lagging Address Register
Op Reg	– Operation Register
PC	– Parity Check
PG	– Parity Generation
SAR	– Storage Address Register
SDR	– Storage Data Register
TAR	– Temporary Address Register





3705-I (BRIDGE STORAGE)

Cards That Can Be Swapped In The CCU

- B4J2, B4K2, and B4N2
- B4L2, B4M2, B4P2, and B4Q2
- B4H2 and B4G2
- B4A2, B4A3, B4A4, and B4A5
- B4B2, B4B3, B4B4, and B4B5
- B4C2, B4C3, B4C4, and B4C5
- B3T2 and B3T3
- B3U2, B3U3, and B3U4
- B4U2 and B4U3

3705-II (FET STORAGE)

Cards That Can Be Swapped In The CCU

- B4J2, B4K2, B4N2, and B4S2
- B4L2, B4M2, B4P2, and B4Q2
- B4H2 and B4G2
- B4A4, and B4B2
- B4A2 and B4A3
- B3U2, B3U3, and B3U4
- B3T2 and B3T3
- B4U2, B4U3

CCU

3705-I CARD FUNCTIONS

See page 6-000 also.

Card Location	ALD Pages	Card Function
B3F2	CS002-CS004 CS006-CS007	Part of Data Flow Register Controls
B3G2	CZ001-CZ005	C and Z Condition Code Latches and the Generation of Their Sets and Gates
	CQ001	Part of Adapter Interface Controls
	CQ004-CQ005	Pulsed Inputs and Outputs
	CD001	Part of Instruction Decode
B3H2	CD001-CD004	Part of Instruction Decode
	CS003	Part of Data Flow Register Controls
B3J2	CA001-CA004	ALU Controls
	CD001	Part of Instruction Decode
B3K2	CL001-CL005	Local Store Controls
B3L2	CU005-CU006 CU009-CU010 CU014	Part of Panel Controls
	CK007	Second Error Detection
	CP006-CP007	Meter and Interval Timer
	CU005	Test Mode and Check Stop Mode
B3M2	CU014-CU015	Part of Panel Controls
	CP002-CP005	Part of Priority Controls, Program Level Select, Program Level Masks and 'Program L Entered' Latches
	CS001	Set LAR
B3N2	CK003-CK007	Error Detection, Error Register
	CU001	Part of Panel Controls
	CU013	Part of CCU Indata Bus
B3P2	CU003-CU007	Part of Panel Controls

Card Location	ALD Pages	Card Function
B3Q2	CC002-CC003	Instruction and Cycle-Steal Times
	CC004-CC005	Instruction and Cycle-Steal Counter and Cycle Counter Error Detection
	CC008	Instruction Starts and Cycle Stops
	CS001	Maintenance Condition
	CQ001-CQ002	Part of Adapter Interface Controls
B3R2	CS007	Set SAR, DR1, and DR2
	CC001	ABCD Counter
	CC006	Local Store Address Register
	CC007	T Times Clock and machine oscillator
	CQ001-CQ002	Part of Adapter Interface Controls
B3S2	CK001-CK002	Force Errors
	CR001-CR008	BSC and SDLC CRC Generation
	CU013	Part of CCU Indata Bus
B3T2	AP001-AP008	Part of Control Panel Switches and Push Buttons
B3T3	AP001-AP008	Part of Control Panel Switches and Push Buttons
B3T4	CP001	Part of Priority Controls
B3U2	AP001-AP008	Part of Control Panel Switches and Push Buttons
B3U3	AP001-AP008	Part of Control Panel Switches and Push Buttons
B3U4	AP001-AP008	Part of Control Panel Switches and Push Buttons
B4A2	DS004-DS005	Frame 1 SDR Drivers and Receivers for Byte 1
B4A3	DT004-DT005	Frame 2 SDR Drivers and Receivers for Byte 1
B4A4	DU004-DU005	Frame 3 SDR Drivers and Receivers for Byte 1

Card Location	ALD Pages	Card Function
B4A5	DV004-DV005	Frame 4 SDR Drivers and Receivers for Byte 1
B4B2	DS002-DS003	Frame 1 SDR Drivers and Receivers for Byte 0
B4B3	DT002-DT003	Frame 2 SDR Drivers and Receivers for Byte 0
B4B4	DU002-DU003	Frame 3 SDR Drivers and Receivers for Byte 0
B4B5	DV002-DV003	Frame 4 SDR Drivers and Receivers for Byte 0
B4C2	DS001	Frame 1 SAR Drivers
B4C3	DT001	Frame 2 SAR Drivers
B4C4	DU001	Frame 3 SAR Drivers
B4C5	DV001	Frame 4 SAR Drivers
B4D2	CV001-CV061	Storage Protect and Error Detection
B4E2	CS005	Part of M Bus Assembler Controls
	CM002-CM003	Read Call/Write Call and Storage Size Input
	CM003	Address Exception Detection
B4F2	CW001-CW012	Read-Only Storage
B4F5	DW001	Control Signal Terminators
B4P2	CS005	Part of M Bus Assembler Controls
B4R2	CF001-CF002 CF003	Force Constants Bit Filter and Parity Generator
	CF004	Shift Right Controls
	CF004	Add Constants
B4U2	AP012-AP015	Part of Panel Indicator Circuits
B4U3	AP009-AP011	Part of Panel Indicator Circuits

3705-II CARD FUNCTIONS

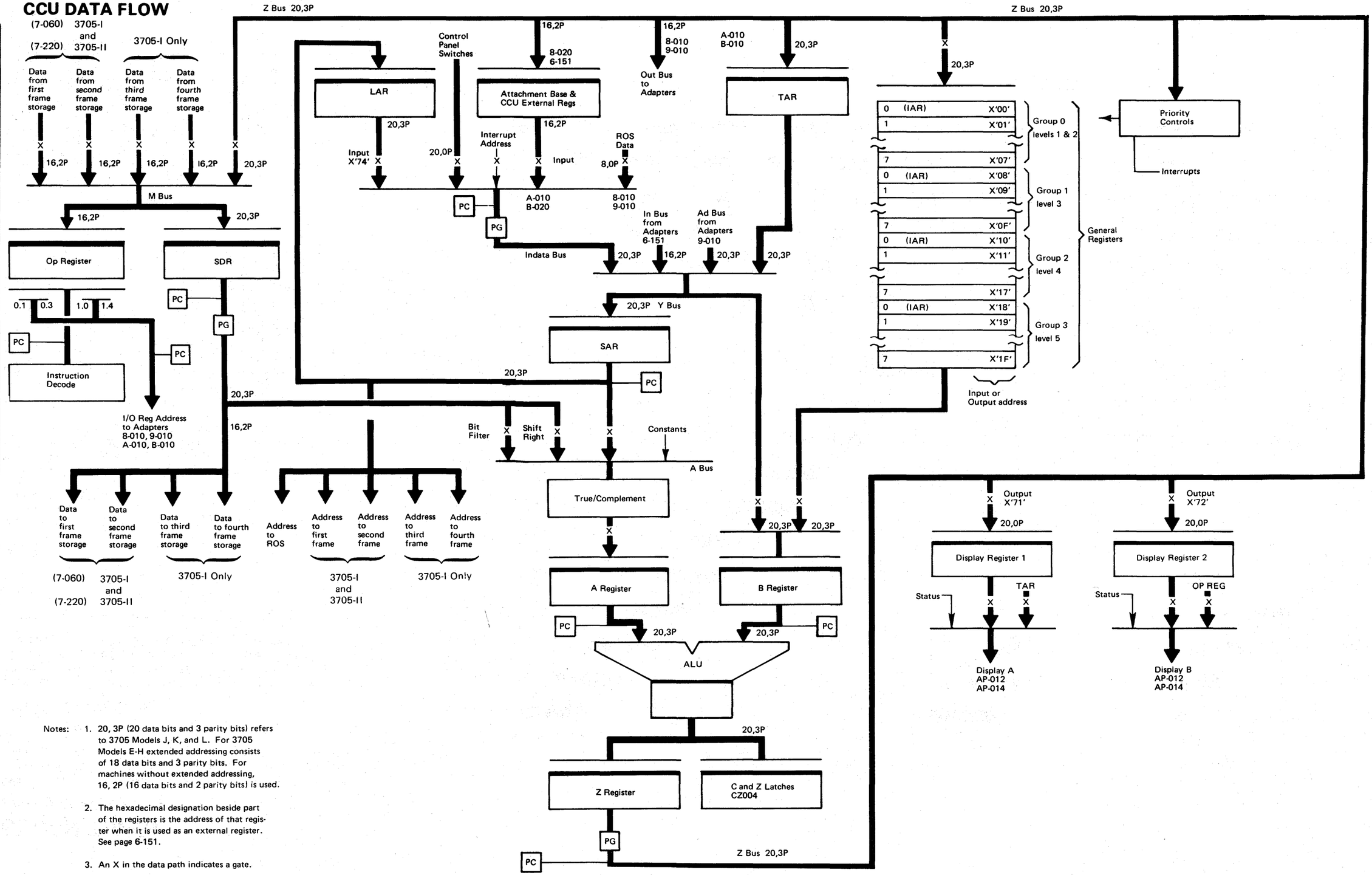
See page 6-000 also.

Card Location	ALD Pages	Card Function
B3F2	CS002, CS004 CS006-CS007	Part of Data Flow Register Controls Data Flow Register Control Timing
B3G2	CZ001-CZ005	C and Z Condition Code Latches and the Generation of Their Sets and Gates
	CQ001	Part of Adapter Interface Controls
	CQ004-CQ005	Pulsed Inputs and Outputs
	CD001	Part of Instruction Decode
B3H2	CD001-CD004	Part of Instruction Decode
	CS003	Part of Data Flow Register Controls
B3J2	CA001-CA004	ALU Controls
	CD001	Part of Instruction Decode
B3K2	CL001-CL005	Local Store Controls
B3L2	CU005-CU006 CU009-CU010 CU014	Part of Panel Controls
	CK007	Prog Level 1 Prog Check Detection
	CP006-CP007	Meter and Interval Timer
	CU005	Test Mode and Check Stop Mode
B3M2	CU014-CU015	Part of Panel Controls
	CP002-CP005	Part of Priority Controls, Program Level Select, Program Level Masks and 'Program Level Entered' Latches
	CS001	Set LAR
B3N2	CK003-CK007	Error Detection, Error Register
	CU001	Part of Panel Controls
	CU013	Part of CCU Indata Bus
B3P2	CU003-CU004 CU006-CU007	Part of Panel Controls
	CS005	M Bus Assembler Control

Card Location	ALD Pages	Card Function
B3Q2	CC002-CC003	Instruction and Cycle-Steal Times
	CC004-CC005	Instruction and Cycle-Steal Counter and Cycle Counter Error Detection
	CC008	Instruction Starts and Cycle Stops
	CS001	Maintenance Condition
	CQ001-CQ002	Part of Adapter Interface Controls
B3R2	CS007	Set SAR, DR1, and DR2
	CC001	ABCD Counter
	CC006	Local Store Address Register and T Times
	CC007	Clock and machine oscillator
	CQ001-CQ002	Part of Adapter Interface Controls
B3S2	CK001-CK002	Force Errors
	CR001-CR008	BSC and SDLC CRC Generation (Type 2 scanner only)
	CU013	Part of CCU Indata Bus
B3T2	AP001-AP008	Part of Control Panel Switches and Push Buttons
B3T3	AP001-AP008	Part of Control Panel Switches and Push Buttons
B3T4	CP001 CM001	Part of Priority Controls Memory Reset
B3U2	AP003-AP015	Part of Control Panel Switches and Push Buttons
B3U3	AP004-AP011	Part of Control Panel Switches and Push Buttons
B3U4	AP001-AP008	Part of Control Panel Switches and Push Buttons
B3U5	CC007 AP008	8 or 8.889 MHz Oscillator Lamp Test
B4A2	DS004	Frame 1 SDR Drivers and Receivers for Byte 1

Card Location	ALD Pages	Card Function
B4A3	DS002	Frame 1 SDR Drivers and Receivers for Byte 0
B4A4	DB101	Memory Control Cable Drivers
B4B2 B4B3	DS001 DT001	Frame 1 SAR Drivers Frame 2 SAR Drivers
B4C2	CG001 CM002	Fet Memory Installed Address Exception
B4D2	CV001-CV061	Storage Protect and Error Detection
B4E2	AJ002	Memory Size Jumper
	CM002-CM003	Read Call/Write Call, Storage Size Input and Allow Set Memory Diagnostic Register
	CM002	Address Exception Detection
B4F2	CW011-CW012	Read-Only Storage
B4F4	CW001	Alternate ROS Feature
B4F5	DW001	Control Signal Terminators
B4R2	CF001-CF002 CF003	Force Constants Bit Filter and Parity Generator
	CF004	Shift Right Controls
	CF004	Add Constants
B4T2	CN001	Cycle Utilization Counter
B4U2	AP012-AP015	Part of Panel Indicator Circuits
B4U3	AP009-AP011	Part of Panel Indicator Circuits
B4U4	AP001	Panel Rotor Switches

CCU DATA FLOW



Notes:

1. 20, 3P (20 data bits and 3 parity bits) refers to 3705 Models J, K, and L. For 3705 Models E-H extended addressing consists of 18 data bits and 3 parity bits. For machines without extended addressing, 16, 2P (16 data bits and 2 parity bits) is used.
2. The hexadecimal designation beside part of the registers is the address of that register when it is used as an external register. See page 6-151.
3. An X in the data path indicates a gate.

CLOCK TIMES

3705-I (BRIDGE STORAGE)

Each 1.2 microsecond machine cycle is divided into six time slots of 200 ns each. The A, B, C, and D times are used for ALU operations. The E and F times are necessary because of bridge storage read-write requirements.

3705-II (FET STORAGE)

Each 1.0 or 900 ns for Models J-L microsecond machine cycle is divided into four time slots of 250 ns each (225 ns for Models J-L). The A, B, C, and D times are used for ALU operations. The E and F times (which occur simultaneously with B and C time, respectively) are used to:

- Synchronize cycle times with the 'gate A time' signal.
- Generate the 'mem store new time' signal.
- Detect a CCU clock error.

CLOCK TIME LIGHTS IN DISPLAY A

If the DISPLAY/FUNCTION SELECT switch is in the STATUS position, display A bit lights 1.4, 1.5, 1.6, and 1.7 show the CCU clock times.

NOTE: When the 3705 is running, the bit 1.7 light does not come on because the firing time is not long enough to heat the light . With the 3705 in clock step mode, the light does comes on.

3705-I only

Cycle Time	A				E				B			
Clock Time	T0	T1	T2	T3	T0	T1	T2	T3	T0	T1	T2	T3
Bit 1.4 of Display A	0	0	0	0	0	0	0	0	0	0	0	0
Bit 1.5 of Display A	0	0	0	0	0	0	0	0	1	1	1	1
Bit 1.6 of Display A	0	0	1	1	0	0	1	1	0	0	1	1
Bit 1.7 of Display A	0	1	0	1	0	1	0	1	0	1	0	1

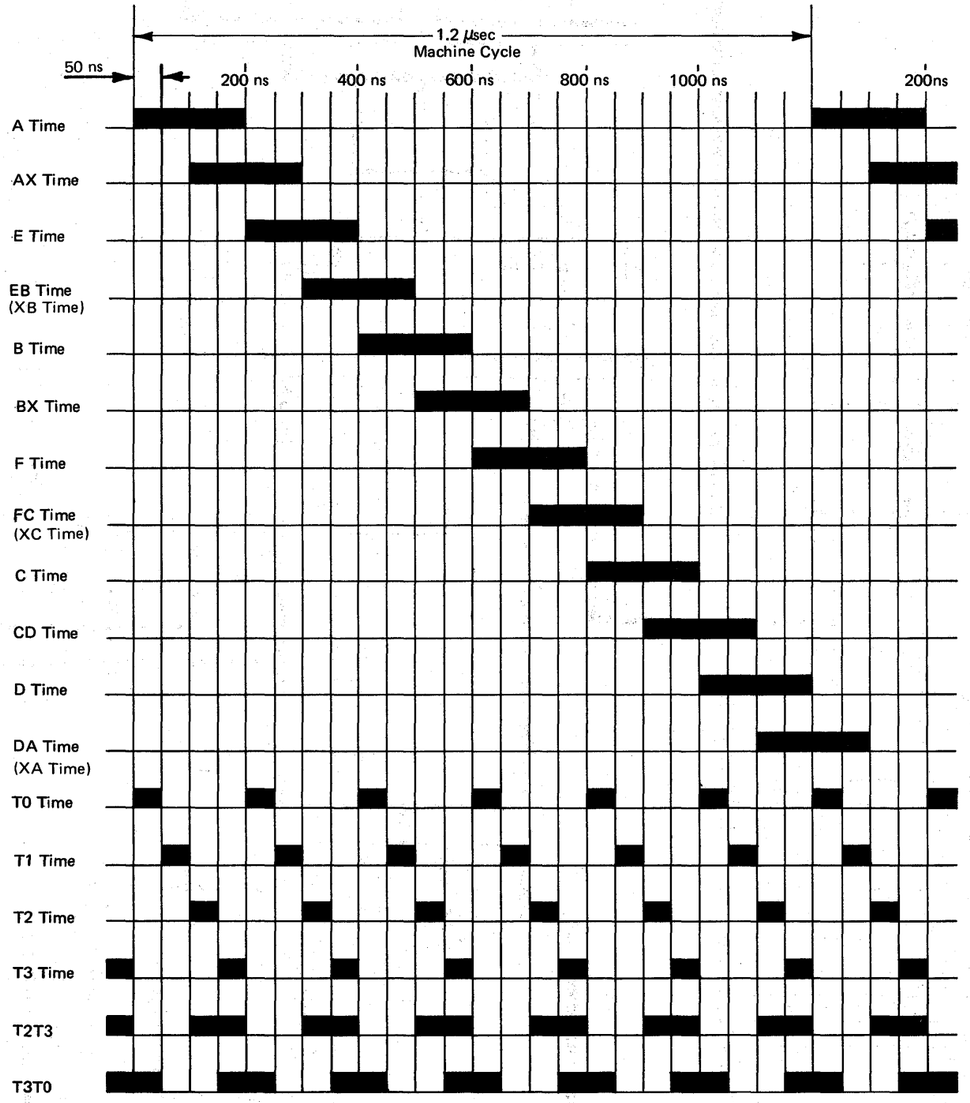
3705-I only

Cycle Time	F				C				D			
Clock Time	T0	T1	T2	T3	T0	T1	T2	T3	T0	T1	T2	T3
Bit 1.4 of Display A	0	0	0	0	1	1	1	1	1	1	1	1
Bit 1.5 of Display A	1	1	1	1	0	0	0	0	1	1	1	1
Bit 1.6 of Display A	0	0	1	1	0	0	1	1	0	0	1	1
Bit 1.7 of Display A	0	1	0	1	0	1	0	1	0	1	0	1

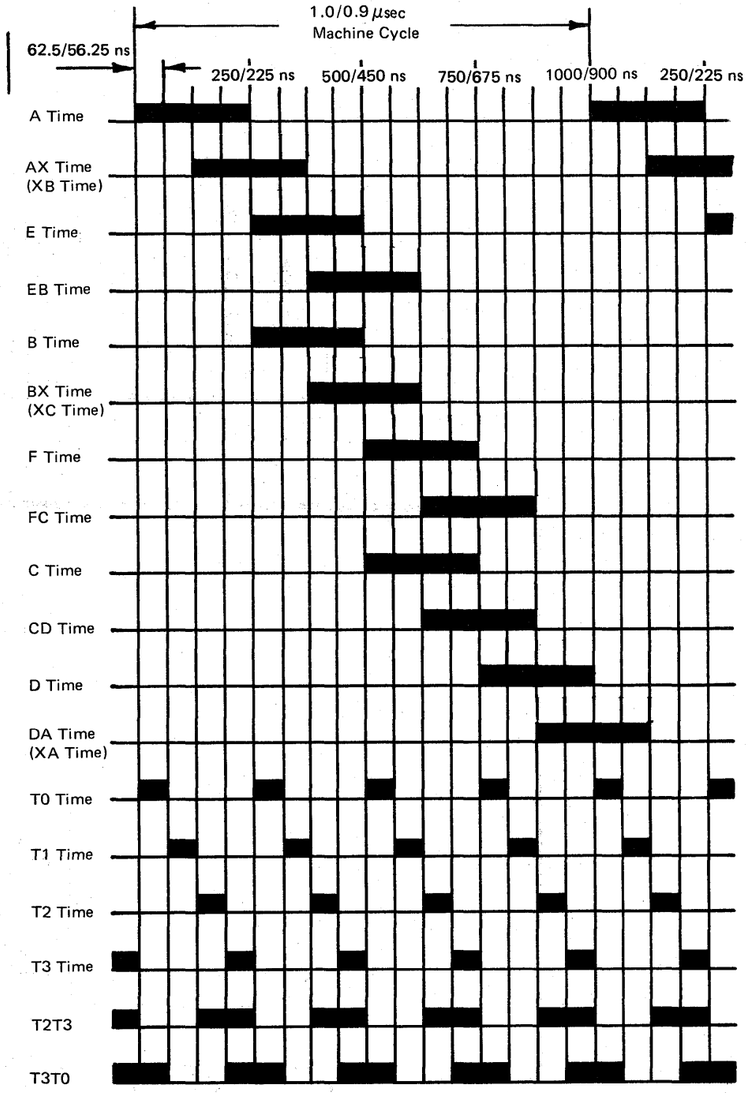
NOTE: Lights indicate the clock time that was just completed.

0 = Off
1 = On

3705-I (Bridge Storage)



3705-II (FET Storage)



ALD Pages CC001 and CC006
Card Location 01A-B3R2

STORAGE PROTECTION

By comparing a three bit protect key with a three bit storage key, storage protection makes it possible to protect the contents of storage from an unauthorized attempt to address storage. Specifically, storage protection does not allow instruction fetching from unauthorized storage and does not allow data modification at an unauthorized address; however it does allow data loading from any storage location any time.

The protect keys are located in an 8 key address bit by 3 key address bit local storage area, and the storage keys are located in a (256 for Models J-L) key address bit by 3 key address bit local storage area. One storage key is assigned to each 2,048 bytes of storage. The protect keys and storage keys are set by an Output X'73' instruction containing the respective key address. (For more information on the Output X'73' instruction, see page 6-880.)

To execute an instruction that does not modify storage, the protect key must be equal to the storage key. If the keys do not match, a protection exception L1 interrupt is set.

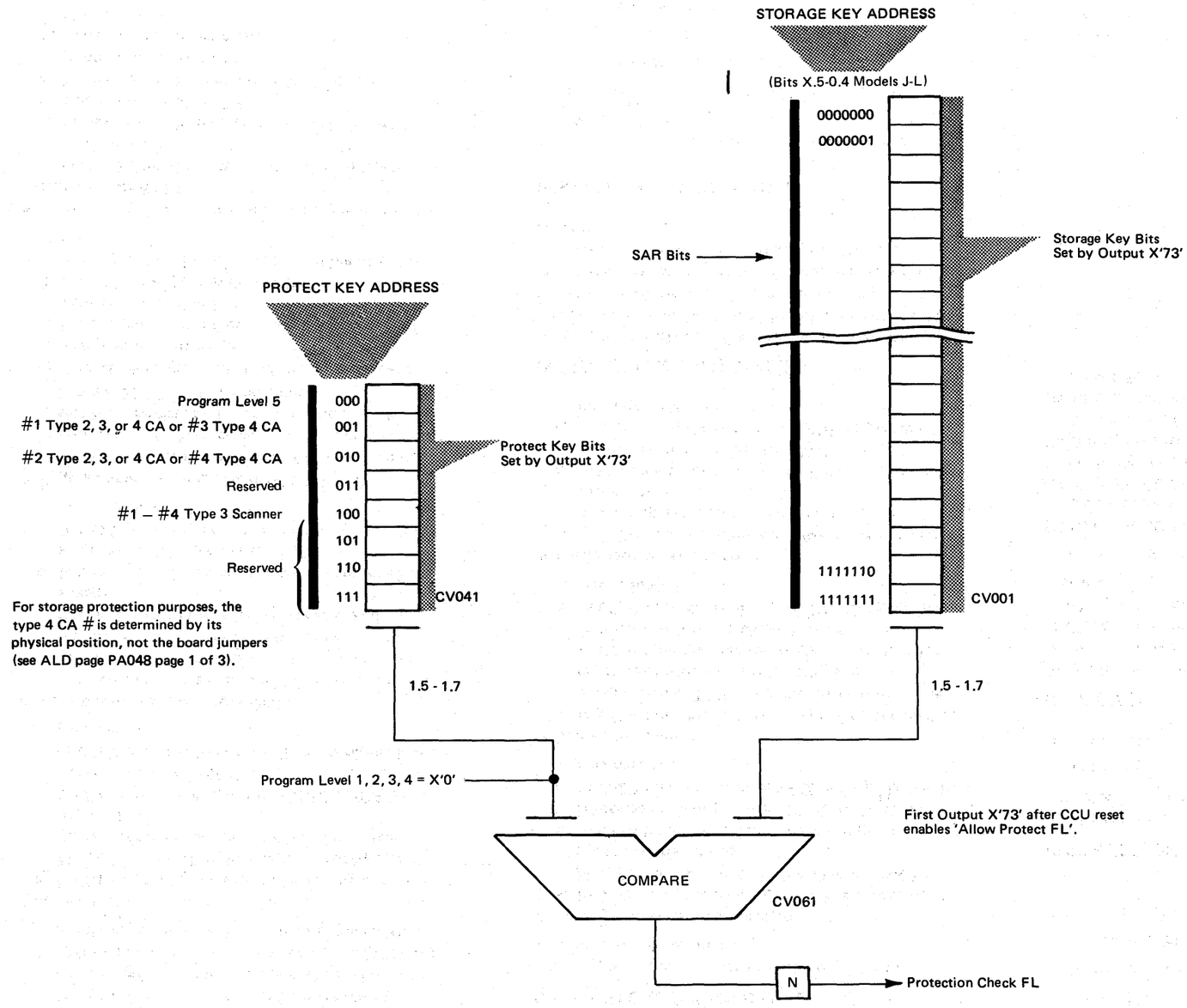
To modify a storage location, one of three conditions must be met:

- The protect key must be equal to the storage key.
- The protect key is X'0', that is, Program Level 1, 2, 3, or 4.
- The storage key is X'7', meaning unprotected storage.
- If none of the conditions are met, the keys are considered not match, and a protection exception L1 interrupt is set.

When the CCU is reset, storage protection is disabled. Therefore, any instruction fetch is valid, and any attempt to modify storage is permitted. The first Output X'73' instruction executed after a reset enables storage protection. This instruction must set a storage key of X'0' at the key address that corresponds to the storage block where the instruction execution is taking place. Otherwise, a protection check occurs if the storage key is not already X'0'.

When the 3705 power is turned on, the bits in the settable protect keys and storage keys assume a random bit pattern. Each key must be initialized by an Output X'73' containing its key address and key type. Until each key is initialized, caution must be used in the control of program levels and I/O activity that may depend on storage protection.

A store storage operation from the control panel cannot cause a storage protection check.



MACHINE CYCLES

The 3705 uses six types of machine cycles: cycle steal 1, cycle steal 2, instruction 1, instruction 2, instruction 3, and idle.

CYCLE STEAL 1 (CS1) CYCLE

CS1 cycles are used for type 3 communication scanner and type 2, 3, or 4 CA cycle-steal operations. They are also used as maintenance cycles in the following control panel operations.

- ROS bootstrap program load (see page 6-961).
- Display register. (See page 6-052.)
  a. In CS1A time, the address in the ADDRESS/DATA switches is placed in the Op register and in display register 1. The address is also placed in TAR if the 3705 is stopped.
  b. In CS1C time, the contents of the external register addressed by bits 0.1-0.3 and bits 1.0-1.3 of the Op register are placed in SDR if the external register is a general register.
  c. In CS1D time, the contents of the 'in bus' (for adapter register), of the 'indata bus' (for CCU register), or of SDR (for CCU general register) are placed in display register 2.
- Display storage. (See page 6-056.)
  a. In CS1A time, the address in the ADDRESS/DATA switches is placed in SAR and in display register 1. The address is also placed in TAR if the 3705 is stopped. The address in SAR is used to address storage.
  b. In CS1B time, the contents of the storage location addressed by SAR are placed in SDR.
  c. In CS1D time, the contents of SDR are placed in display register 2.
- START pushbutton operations. (See page 6-069).
  a. In CS1A time, the address in TAR is placed in SAR and in display register 1.
  b. In CS1B time, the contents of the Z bus are placed in SDR. (This occurs by default and has no effect on the start cycle or on the following cycle.)
  c. In CS1D time, the address in the active IAR is placed in TAR and in display register 2.
- Storing in a register. (See page 6-054.)
  a. In CS1A time, the contents of TAR are placed in display register 1. (TAR should contain a register address.)
  b. In CS1C time, the data in the ADDRESS/DATA switches is placed in SDR and on the 'out bus' to the adapters.
  c. In CS1D time, the contents of SDR are placed in display register 2. If the register designated by the set address and display register procedure is a CCU register, the contents of SDR are placed in the register.
- Storing in storage. (See page 6-057.)
  a. In CS1A time, the address in TAR is placed in SAR. The address in TAR is then incremented by 2, and the new address is placed in TAR and in display register 1.
  b. In CS1B time, the data in the ADDRESS/DATA switches is placed in SDR.
  c. In CS1D time, the contents of SDR are placed in display register 2.
- Storage scanning. (See page 6-063.)
  a. In CS1A time, the address in TAR is placed in SAR. The address in TAR is then incremented by 2, and the new address is placed in TAR and in display register 1. The address in SAR is used to address storage.
  b. In CS1B time, the contents of the storage location addressed by SAR are placed in SDR.
  c. In CS1D time, the contents of SDR are placed in display register 2.
- Single address scanning. (See page 6-067.)
  a. In CS1A time, the contents of TAR are placed in display register 1. The address in SAR is used to address storage. (The first cycle does not address the location in the ADDRESS/DATA switches.)
  b. In CS1B time, the contents of the storage location addressed by SAR are placed in SDR.
  c. In CS1C time, the address in the ADDRESS/DATA switches is placed in TAR.
  d. In CS1D time, the contents of SDR are placed in display register 2. The contents of TAR are placed in SAR.
- Storage test pattern (page 6-060) and single address test pattern (page 6-064).
  a. In CS1A time, the contents of TAR are placed in display register 1.
  b. In CS1B time, the data in the ADDRESS/DATA switches is placed in SDR.
  c. In CS1C time, the contents of SDR are stored in the location addressed by SAR.
  d. In CS1D time, the contents of SDR are placed in display register 2.

CS1 cycles can occur between instruction cycles because CS1 cycles have higher priority.

CYCLE STEAL 2 (CS2) CYCLE

A CS2 cycle is required after each CS1 cycle for the following control panel operations.

- Storing data in a storage location
  a. In CS2A time, the contents of TAR are placed in display register 1 and in SAR. The address in SAR is used to address storage.
  b. In CS2B time, the contents of the storage location addressed by SAR (original +2) are read into SDR.
  c. In CS2D time, the contents of SDR are placed in display register 2.
- Storage test pattern
  a. In CS2A time, the address in TAR is incremented by 2 and placed in TAR and in display register 1. The contents of SAR are used to address storage.
  b. In CS2B time, the contents of the storage location addressed by SAR are placed in SDR.
  c. In CS2D time, the contents of SDR are placed in display register 2.
- Single address test pattern
  a. In CS2A time, the address in TAR is placed in TAR and in display register 1. (The address is not incremented.)
  b. In CS2B time, the contents of SDR are stored at the storage location addressed by SAR.
  c. In CS2D time, the contents of SDR are placed in display register 2.

INSTRUCTION 1 (I1) CYCLE

An I1 cycle is used as the first machine cycle taken to execute an instruction. The first 16 bits of the instruction are placed in the Op register. Most instructions require only an I1 cycle for execution. Instructions that require additional machine cycles for execution are listed in the next paragraph.

INSTRUCTION 2 (I2) CYCLE

The I2 cycle is used as the second machine cycle for the following instructions.

- 'Insert character and count' (ICT)
- 'Store character and count' (STCT)
- 'Insert character' (IC)
- 'Store character' (STC)
- 'Load' (L)
- 'Store' (ST)
- 'Branch and link register' (BALR)
- 'Branch and link' (BAL)
- 'Load address' (LA)

INSTRUCTION 3 (I3) CYCLE

An I3 cycle is required as the third machine cycle for the following instructions if the 3705 has extended addressing.

- 'Load' (L)
- 'Store' (ST)

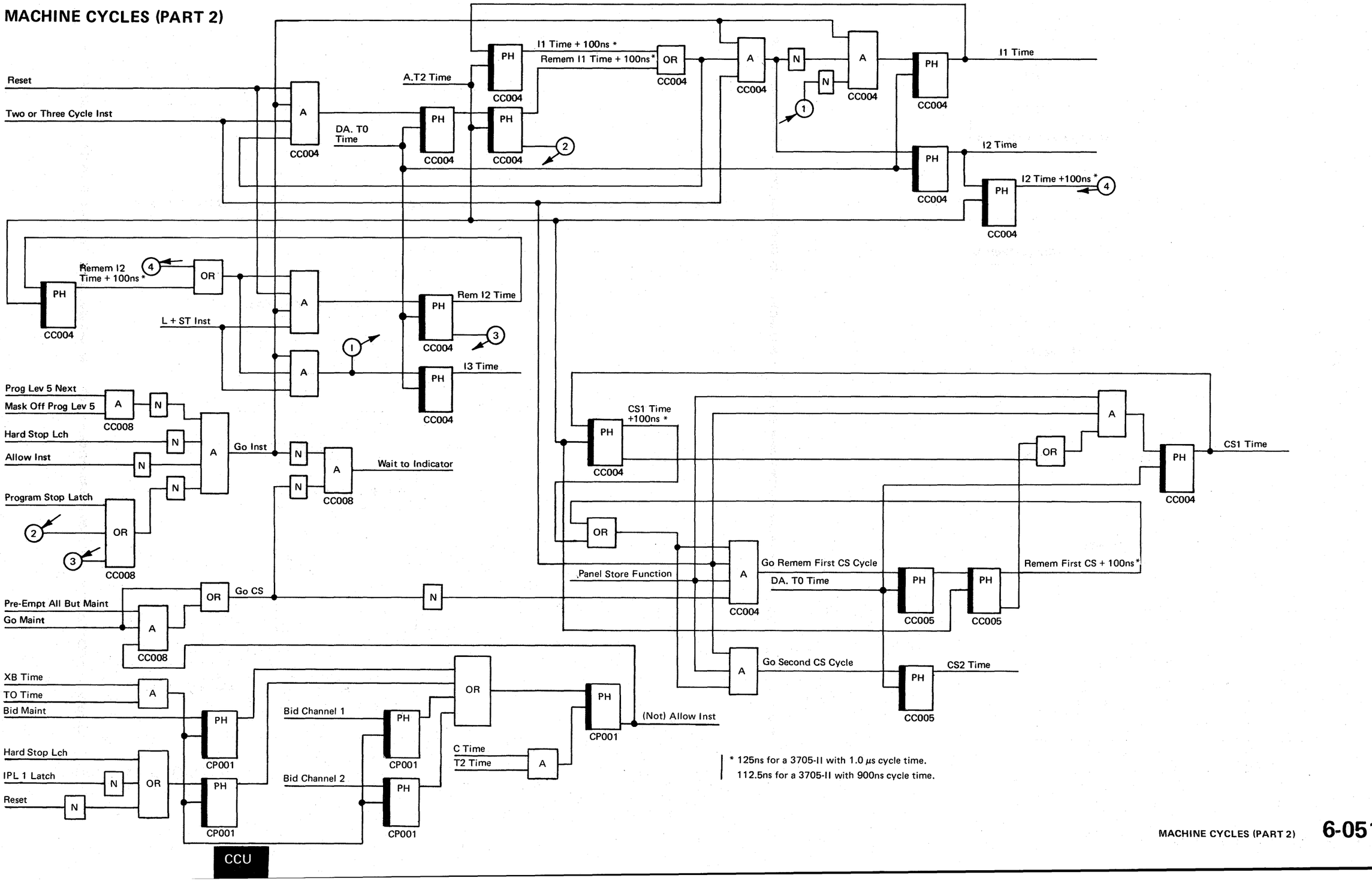
IDLE CYCLE

An idle cycle occurs whenever CS1, CS2, I1, I2, or I3 cycles are not being executed. When an idle cycle occurs, the WAIT light turns on, and the 3705 is in the wait state. The WAIT light turns off when a CS1, CS2, I1, I2, or I3 cycle is executed.

Idle cycles are those cycle time slots that occur:

(1) When the CCU is hardstopped and no panel functions are being used.
(2) When the CCU is program stopped, no panel functions are being used, and no adapter is cycle-stealing.
(3) During the first cycle of a START push button operation (also known as 'dummy' cycles).
(4) After an exit instruction when level 5 is masked off and no bids for any level are pending, until an interrupt occurs.

MACHINE CYCLES (PART 2)



* 125ns for a 3705-II with 1.0 μs cycle time.
112.5ns for a 3705-II with 900ns cycle time.

DISPLAY REGISTER

Procedure on page 1-130

CS1A time:
- Places the register address from the ADDRESS/DATA switches into the Op Register and Display Reg 1.
- Places the address into TAR if the 3705 is stopped.

Address/Data Sw

X Gate Hex SW B and D (CS004)
X Gate CCU Indata to Y Bus (CS004)
X Gate Y Bus to B Reg (CS004)
X T0 +T1 Time Set A-B Reg (CS004)

B Register — DE002 DF002 DG002

ALU — B Reg Direct

DE008 DF008 DG008

Z Register — DE974 DF974 DG974

X Set DR1 (CS007)
X Set Op Reg (CS007)
X Set TAR (CS007) (If Stopped)

Display Register 1 — DE003 DF003 DG003

Op Register — DN001

TAR — DE971 DF971 DG971

X Gate Displ Reg 1 to Ind (CU001)

Display A — AP011 AP012

I/O Reg Address Bus to all external registers (CCU and adapters)

CS

CS1E — 3705-I Only

CS1E time is necessary because of bridge storage characteristics

CS1B

No Action

CS1F — 3705-I Only

CS1F time is necessary because of bridge storage characteristics

CS1C time:
- Places the contents of a general register into SDR if the Op Reg addresses X'00'-X'1F'

CS1C

General Register — Specified by bits 0.1-0.3 and 1.0-1.3 of Op Register

X T0+T1 Time Set A-B Reg (CC007)

B Register — DE002 DF002 DG002

ALU — B Reg Direct

DE008 DF008 DG008

Z Register — DE974 DF974 DG974

X Gate Z Bus Byte to M Bus (CS005)
X Set SDR Byte (CS007) (Display Push button)

SDR — DN001

A — To Next Page

To Next Page

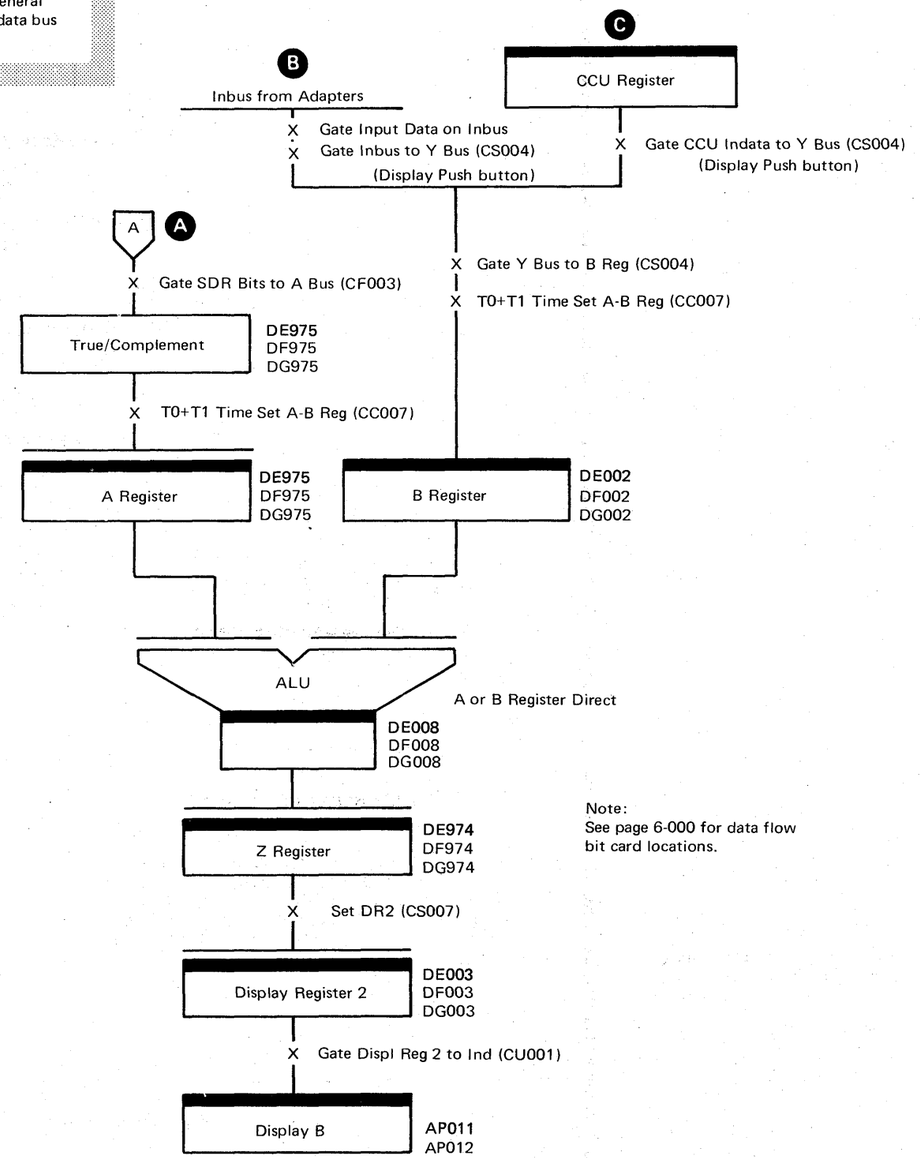
Note:
See Page 6-000 for data flow bit card locations.

From Preceding Page

One of the following occurs during CS1D time:

- **A** If the addressed register is a general register, the contents of SDR (contents of the register) are placed in Display Register 2.
- **B** If the addressed register is an adapter register, the contents of the register are gated on the Inbus and placed in Display Register 2.
- **C** If the addressed register is a CCU register (other than a general register), the contents of the register are gated on the Indata bus and placed in Display Register 2.

CS1D



Note:
See page 6-000 for data flow bit card locations.

End of Cycle

STORE REGISTER (3705 STOPPED)

Procedure on page 1-130

CS1A time Places contents of TAR into Display Register 1.

Op Reg and TAR should contain the register address entered in the SET ADDRESS/DISPLAY push button operation. The address in the Op register is placed on the Op Reg I/O Address Bus to all external Registers (CCU and adapter.)

TAR — DE971 DF971 DG971

X Gate TAR to Y Bus((CS004)

X T0+T1 Time Set A-B Reg (CC007)

B Register — DE002 DF002 DG002

ALU — B Reg Direct

DE008 DF008 DG008

Z Register — DE974 DF974 DG974

X Set DR1 (CS007)

Display Register 1 — DE003 DF003 DG003

X Gate Displ Reg 1 to Ind (CU001)

Display A — AP011 AP012

CS1A

CS1 E — 3705-I Only

CS1E time is necessary because of bridge storage characteristics

CS1B

No Action

To Next Column

CS1F — 3705-I Only

CS1F time is necessary because of bridge storage characteristics

CS1C time:

- Places data from ADDRESS/DATA switches into SDR.
- Places data from ADDRESS/DATA switches on 'out bus' to adapters

CS1C

Address/Data SW

X Gate Hex Sw A and C and E (CS004)

X Gate Hex Sw B and D (CS004)

X Gate CCU Indata to Y Bus (CS004)

X Gate Y Bus to B Reg (CS004)

X T0+T1 Time Set A-B Reg (CC007)

B Register — DE002 DF002 DG002

ALU — B Reg Direct

DE008 DF008 DG008

Note:
See page 6-000 for data flow bit card locations.

Z Register — DE974 DF974 DG974

X Set SDR Byte (CS007)

X Sample Output Data (CQ001)

Out bus to Adapter

SDR — DN001

Perform output function specified by value in data switches during CD time (summarized on page 6-151)

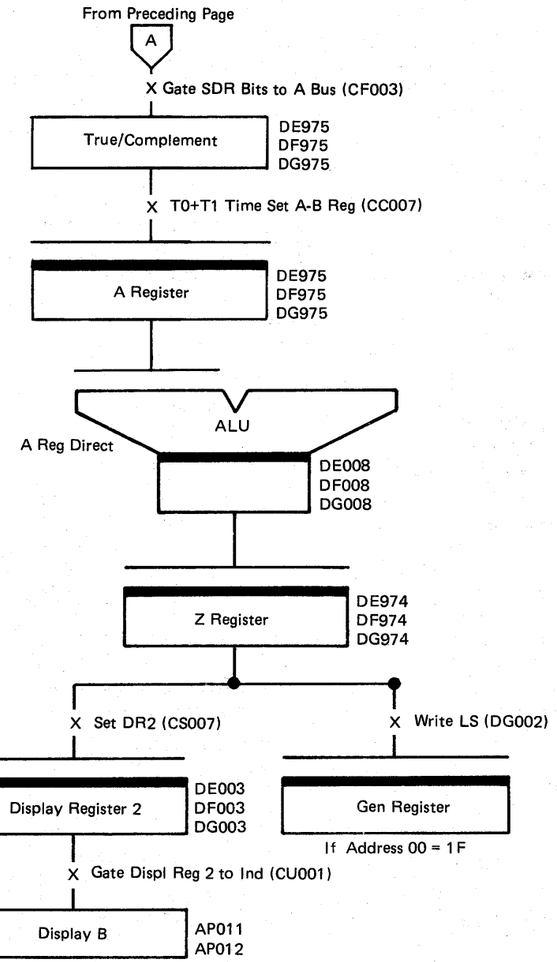
A

To Next Page

To Next Page

From Preceding Page

CS1D time:
- Places the contents of SDR into Display Register 2.
- Places the contents of SDR into the Register designated by TAR.



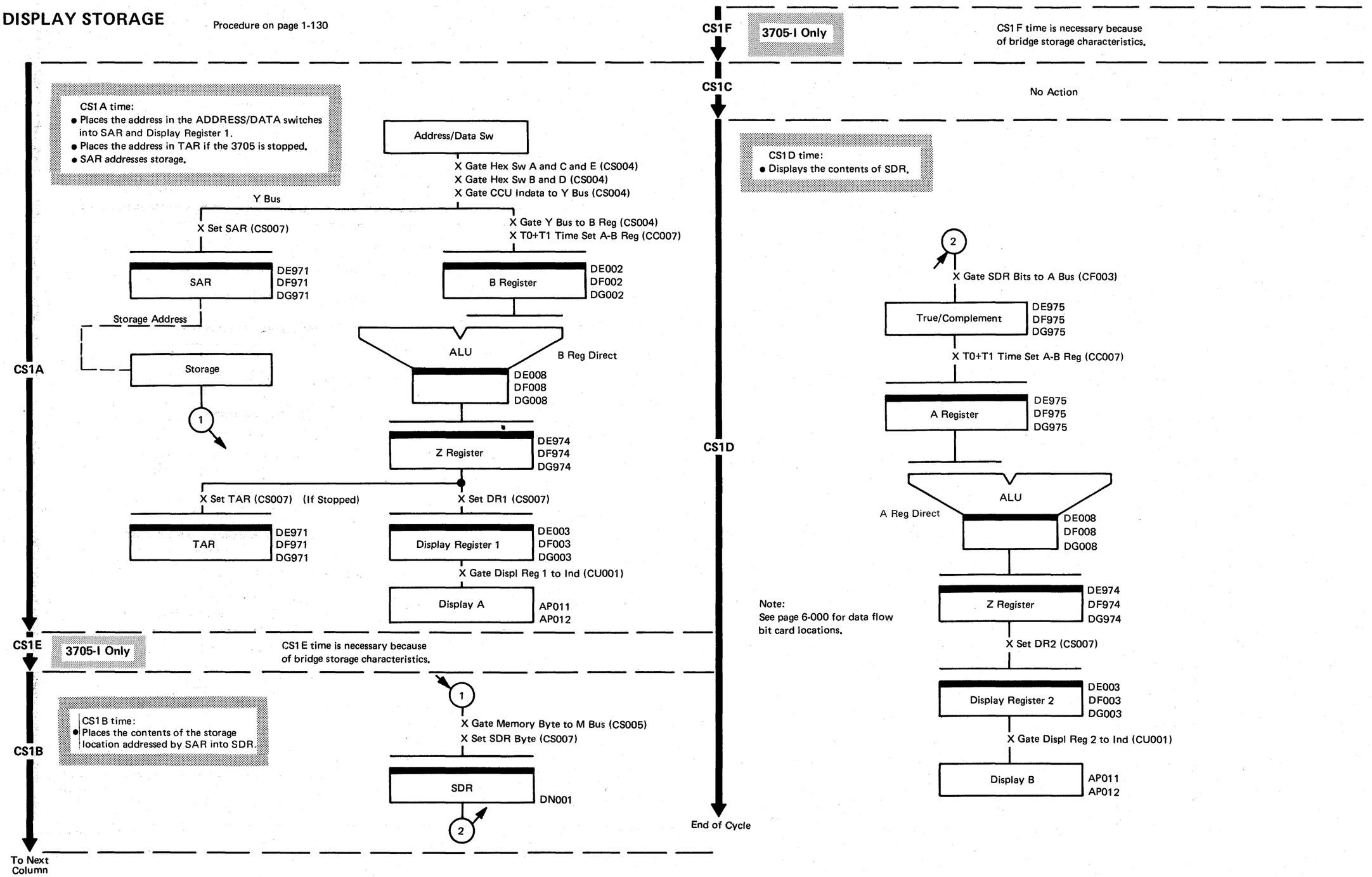
CS1D

Note:
See page 6-000 for data flow bit card locations.

End of Cycle

DISPLAY STORAGE

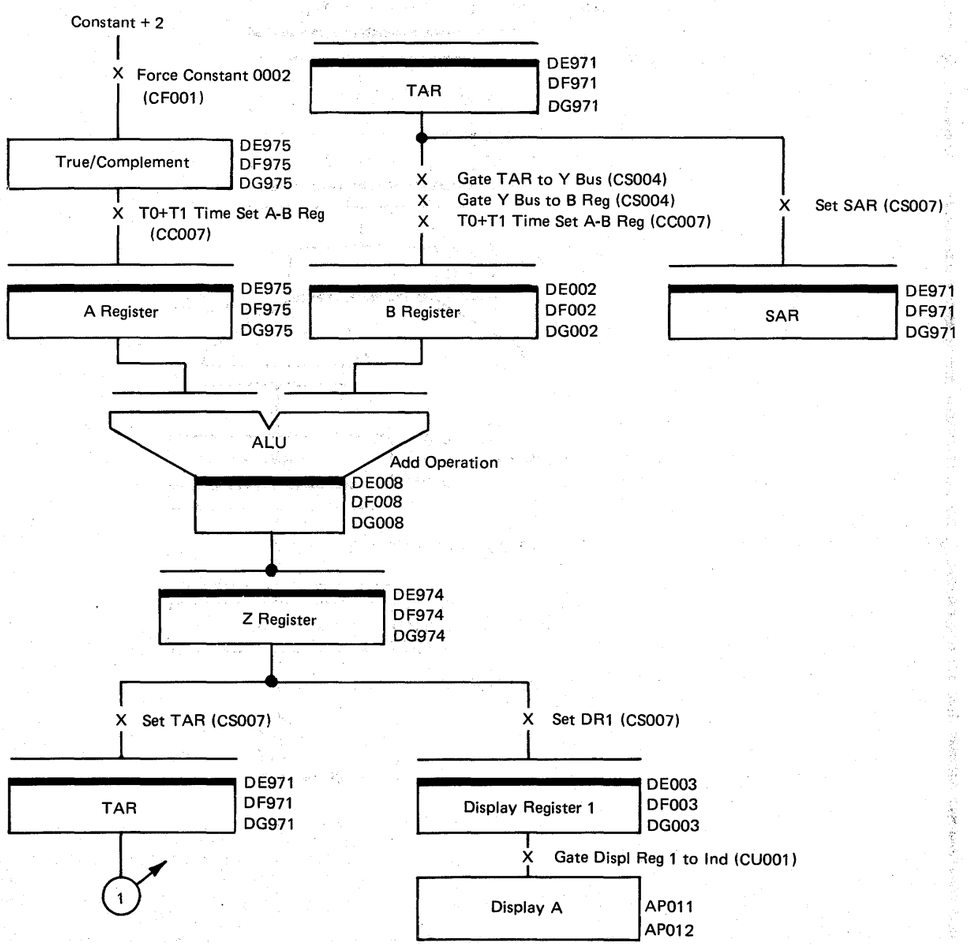
Procedure on page 1-130



STORING DATA IN A STORAGE LOCATIONS WITH THE 3705 STOPPED (PART 1)

Procedure on page 1-140

CS1A time:
- Places the address from TAR into SAR.
- Increments the address in TAR by 2.
- Places the new address into TAR and Display Register 1.



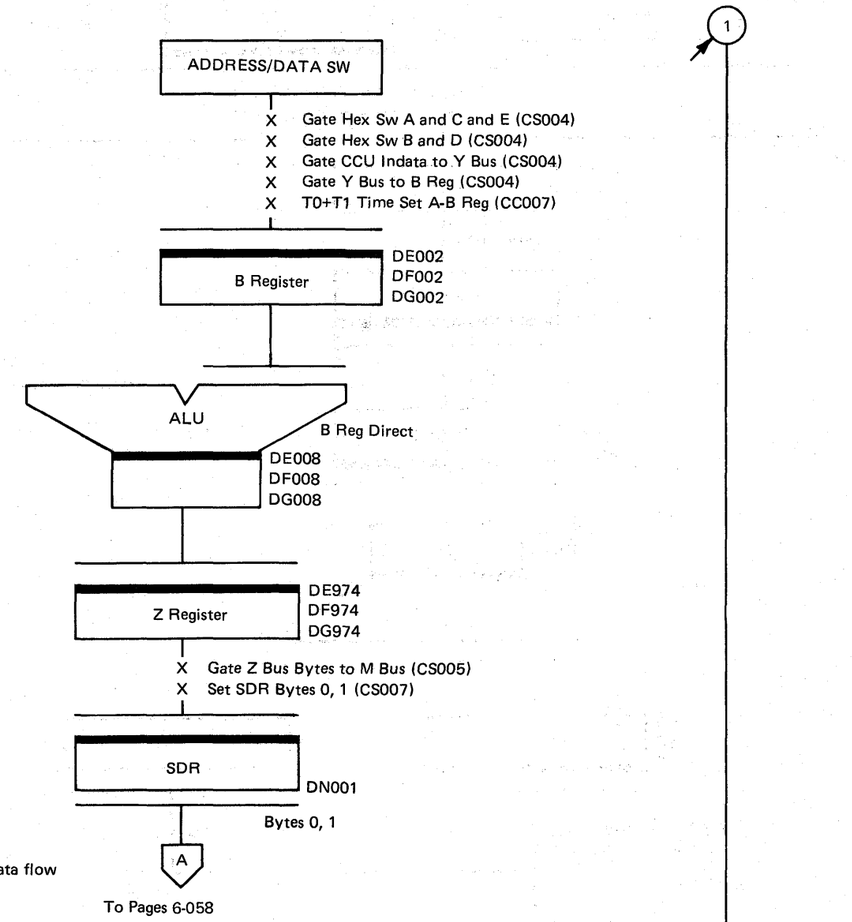
CS1A

CS1E — 3705-I Only

CS1E time is necessary because of bridge storage characteristics.

To Next Column

CS1B time:
- Places the data in the ADDRESS/DATA switches into SDR.



CS1B

Note:
See page 6-000 for data flow bit card locations.

CS1F — 3705-I Only

The write cycle begins. The contents of SDR are stored in location addressed by SAR.

CS1C

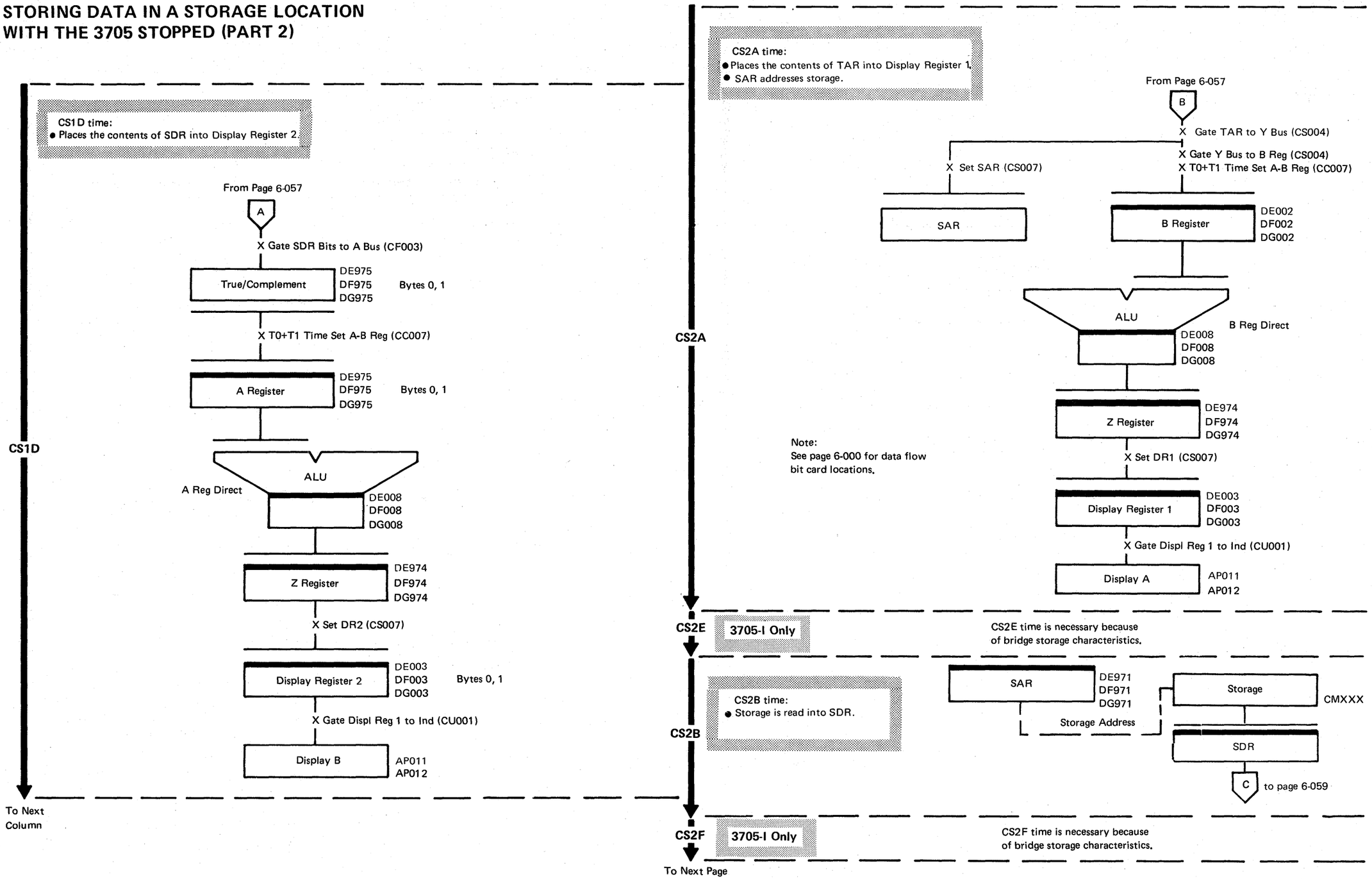
3705-I
No Action

3705-II
The write cycle begins. The contents of the SDR are stored in the location addressed by SAR.

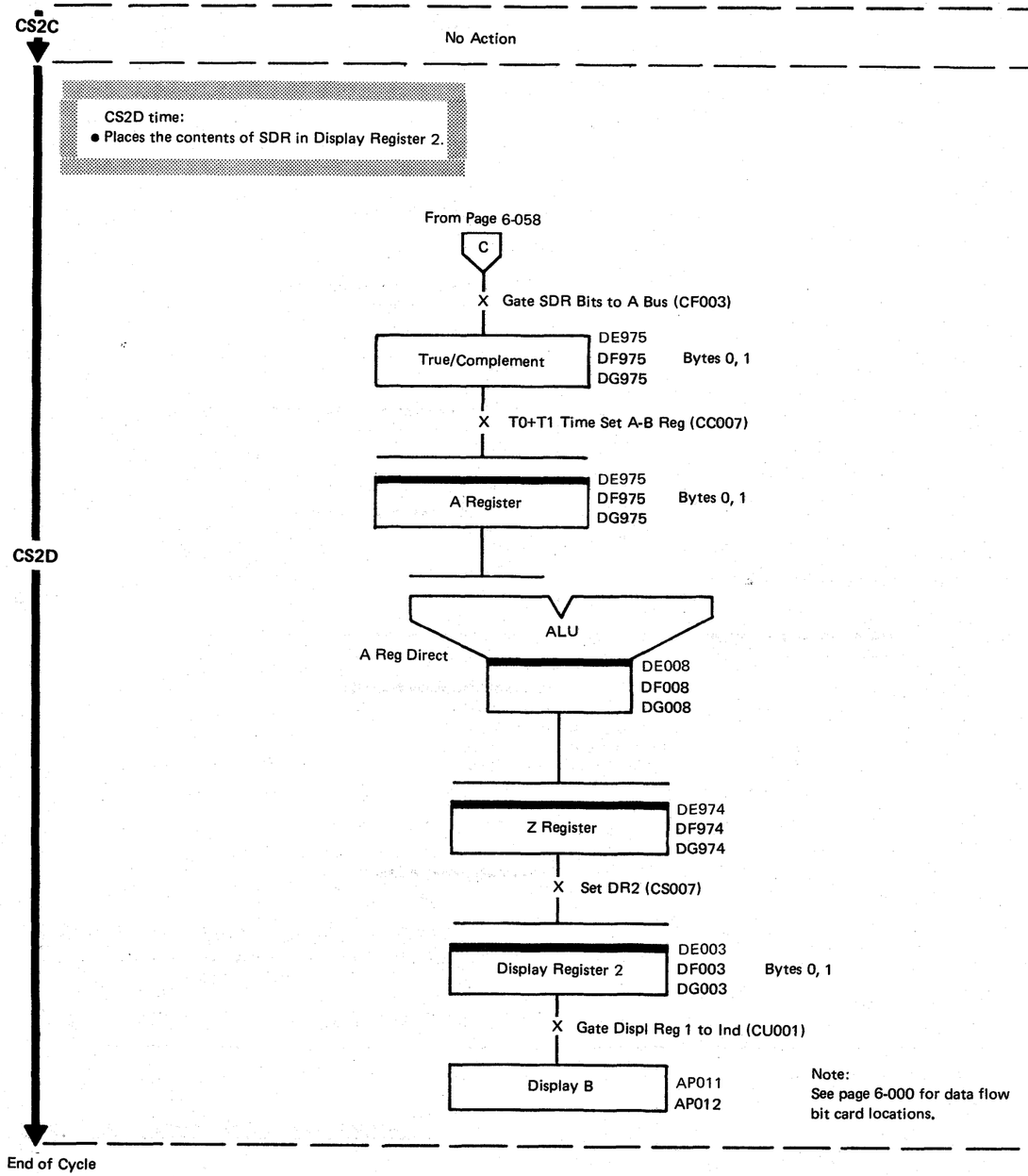
B
To Next Page

To Next Page

STORING DATA IN A STORAGE LOCATION WITH THE 3705 STOPPED (PART 2)



STORING DATA IN A STORAGE LOCATION WITH THE 3705 STOPPED (PART 3)



STORAGE TEST PATTERN (PART 1)

Procedure on page 1-140

CS1A time:
- Places the contents of TAR into SAR.
- Places the contents of TAR into Display Register 1.

CS1A

TAR — DE971, DF971, DG971

X Gate TAR to Y Bus (CS004)
X Gate Y Bus to B Reg (CS004)
X T0+T1 Time Set A-B Reg (CC007)

B Register — DE002, DF002, DG002

X Set SAR (CS007)

SAR — DE971, DF971, DG971

Storage Address

Storage — CM001, CM002, CM003

ALU

B Reg Direct

DE008, DF008, DG008

Z Register — DE974, DF974, DG974

X Set DR1 (CS007)

Display Reg 1 — DE003, DF003, DG003

X Gate Displ Reg 1 to Ind (CU001)

Display A — AP011, AP012

CS1E — 3705-I Only

CS1E time is necessary because of bridge storage characteristics.

To Next Column

CS1B time:
- Places data bytes 0 and 1 of the ADDRESS/DATA switches into SDR.

CS1B

Note:
See page 6-000 for data flow bit card locations.

ADDRESS/DATA SW

X Gate Hex Sw A and C and E (CS004)
X Gate Hex Sw B and D (CS004)
X Gate CCU Indat to Y Bus (CS004)
X T0+T1 Time Set A-B Reg (CC007)

B Register — DE002, DF002, DG002

ALU

B Reg Direct

DE008, DF008, DG008

Z Register — DE974, DF974, DG974

X Set SDR Byte (CS007)

Bytes 0, 1

SDR — DN001, Bytes 0, 1

A

To Pages 6-061 and 6-062

CS1F — 3705-I Only

CS1F time is necessary because of bridge storage characteristics.

CS1C time:
- Places the contents of SDR into the storage location addressed by SAR.

CS1C

SDR — DN003

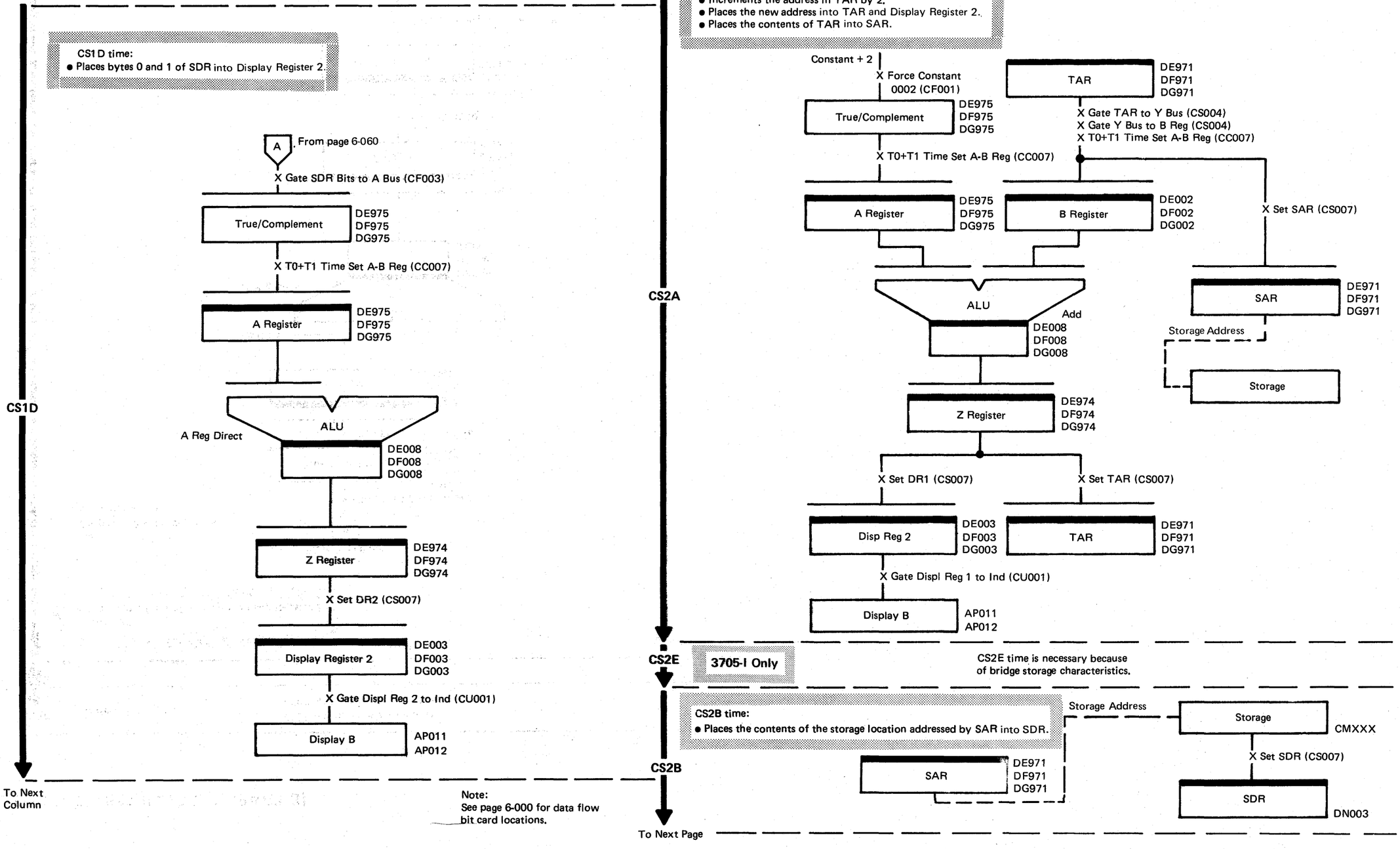
SAR — DE971, DF971, DG971

Storage Address

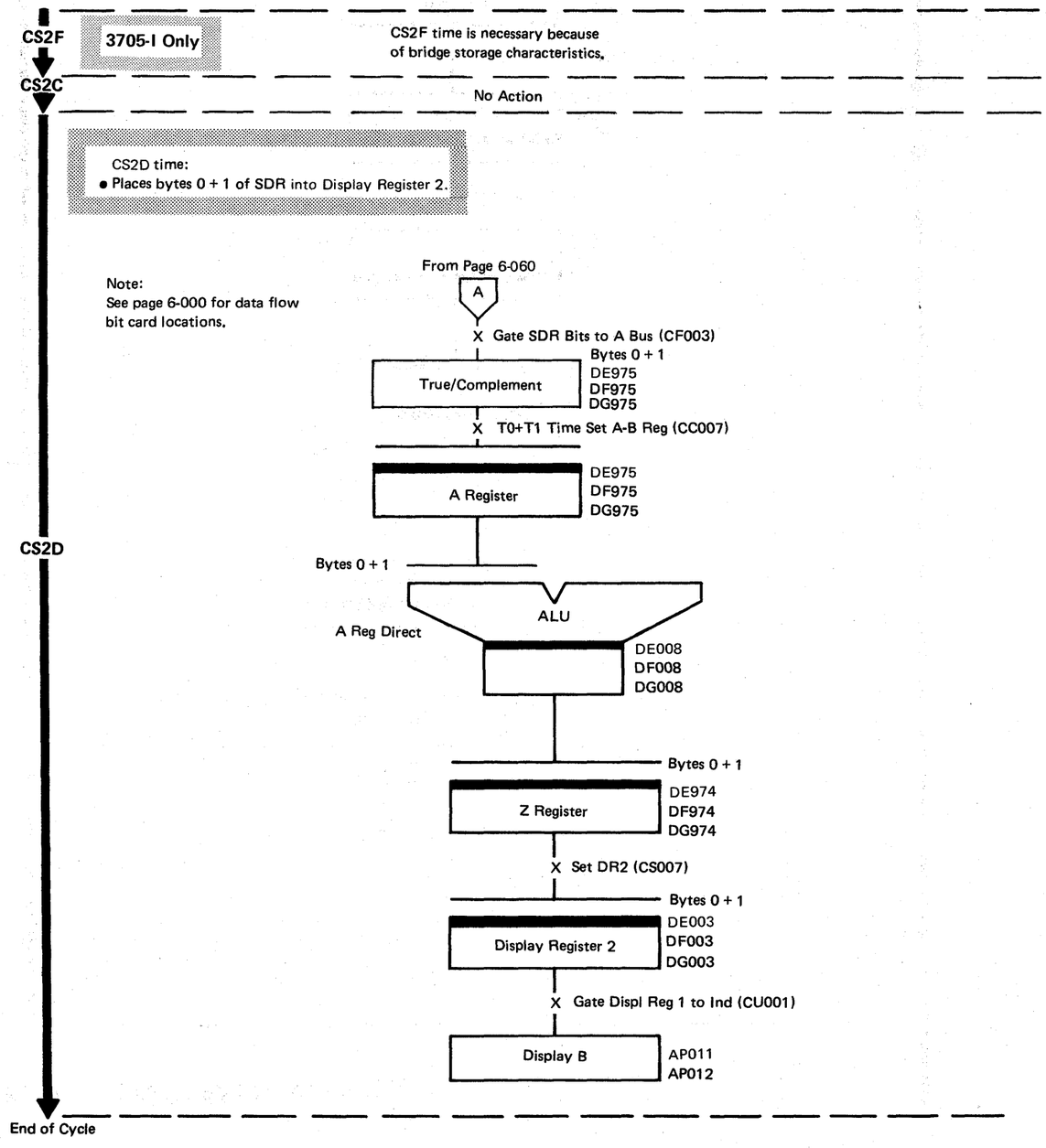
Storage — CMXXX

To Next Page

STORAGE TEST PATTERN (PART 2)

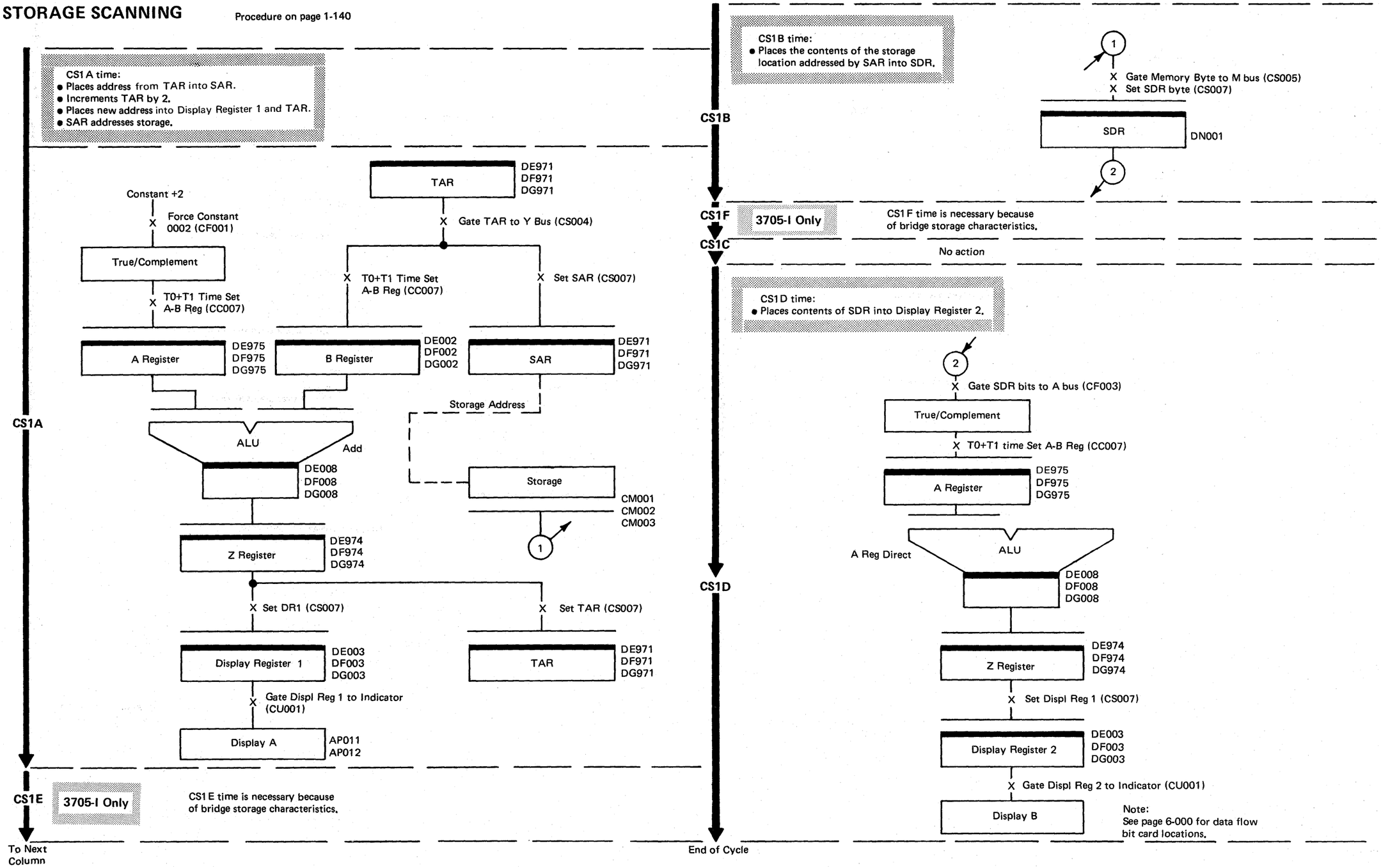


STORAGE TEST PATTERN (PART 3)



STORAGE SCANNING

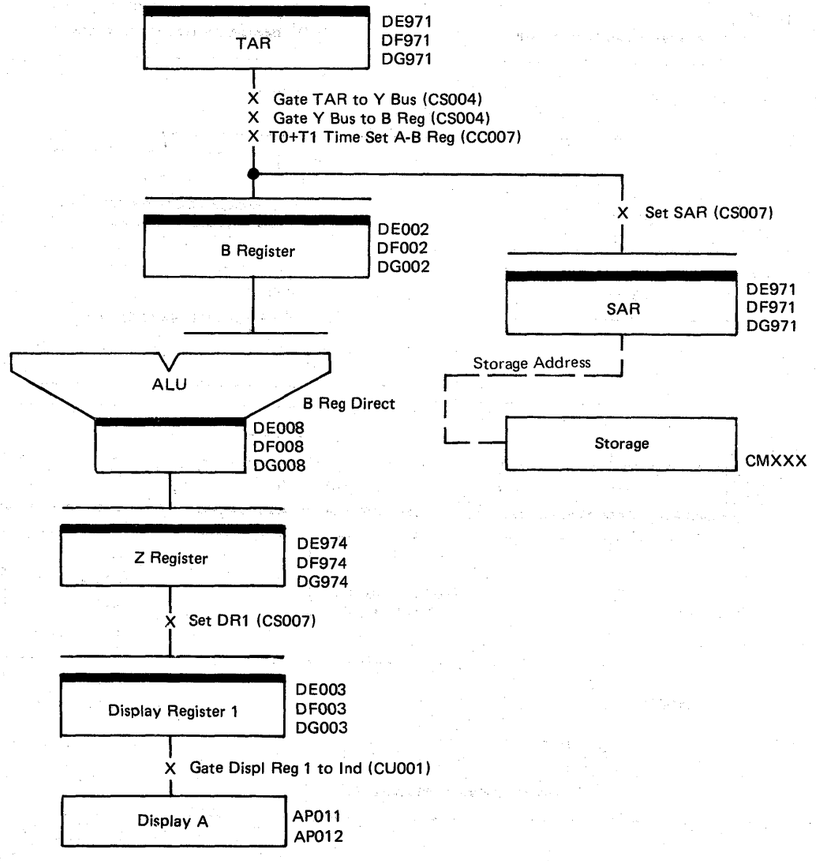
Procedure on page 1-140



SINGLE ADDRESS TEST PATTERN (PART 1)

Procedure on page 1-150

CS1A time:
- Places the contents of TAR into Display Register 1.
- Places the contents of TAR into SAR.



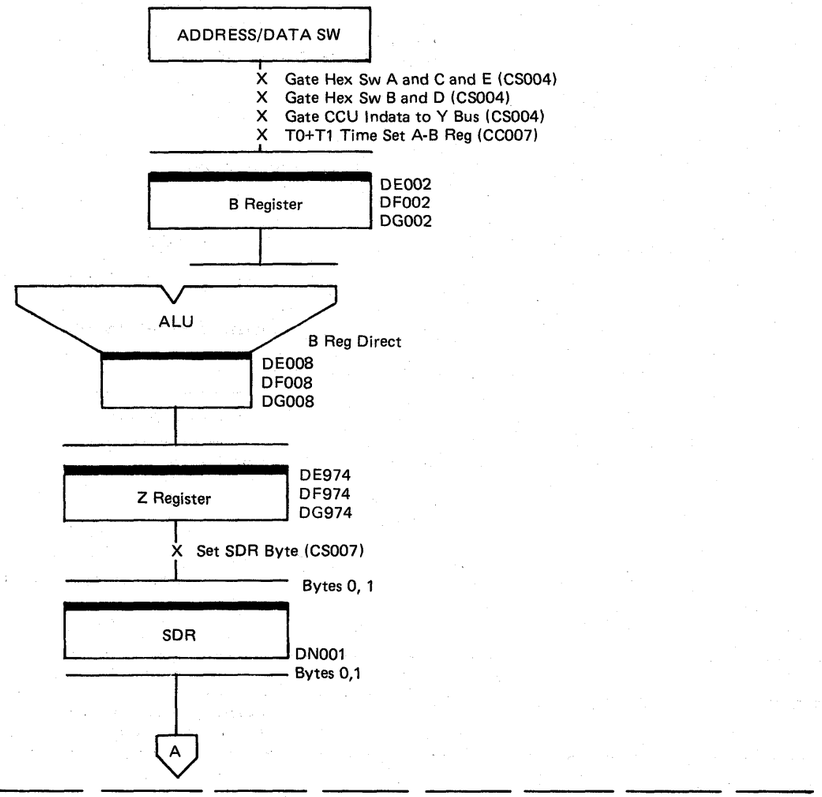
CS1E **3705-I Only**

CS1E time is necessary because of bridge storage characteristics.

To Next Column

CS1B time:
- Places the data bytes 0 and 1 of the ADDRESS/DATA switches into SDR.

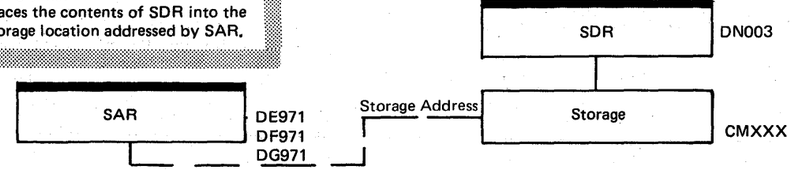
Note:
See page 6-000 for data flow bit card locations.



CS1F **3705-I Only**

CS1F time is necessary because of bridge storage characteristics.

CS1C time:
- Places the contents of SDR into the storage location addressed by SAR.

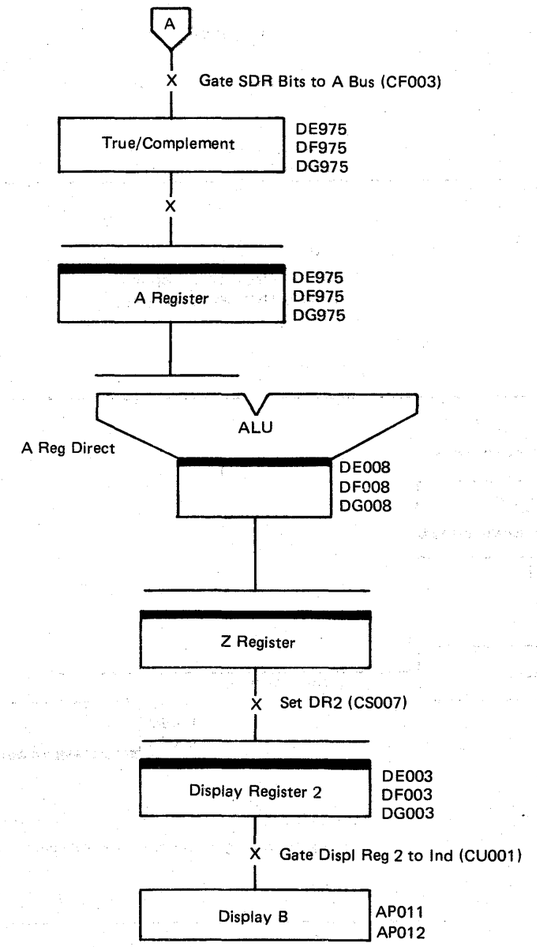


To Next Page

SINGLE ADDRESS TEST PATTERN (PART 2)

CS1D

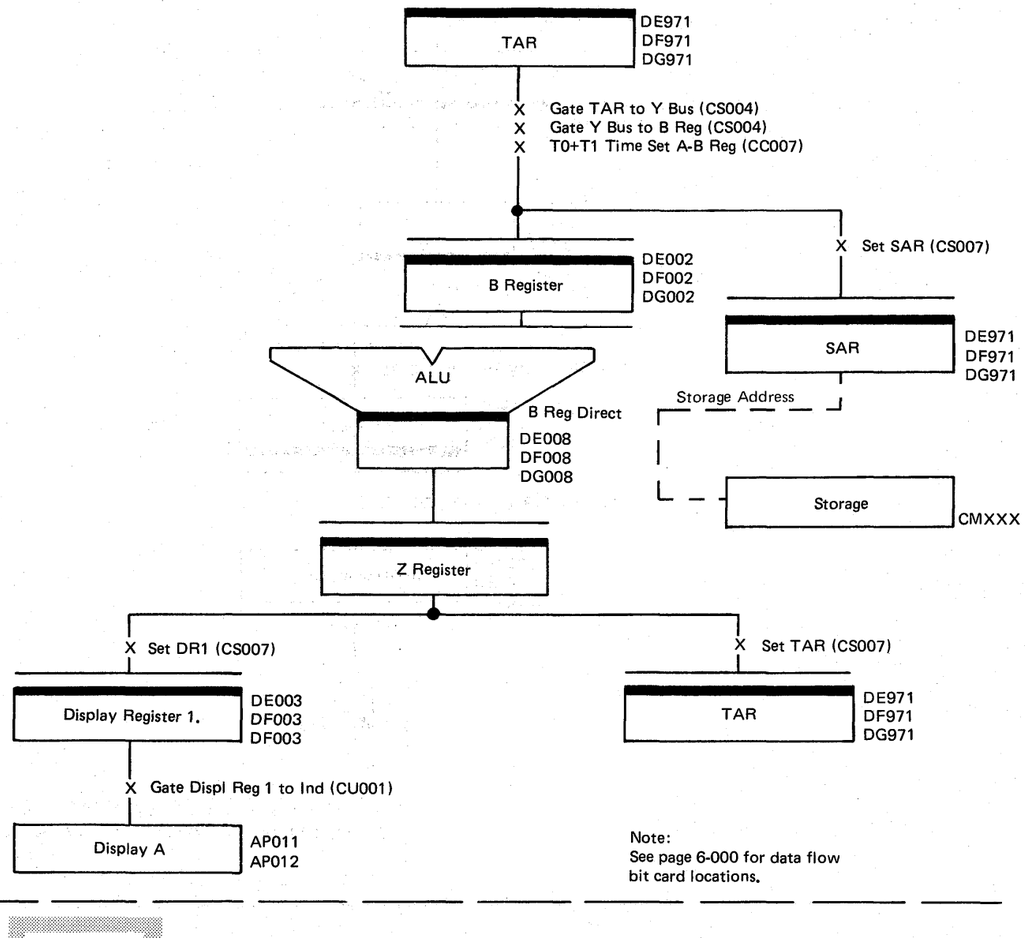
CS1D time:
- Places bytes 0 and 1 of SDR into Display Register 2.



To Next Column

CS2A

CS2A time:
- Places the address from TAR into TAR and Display Register 1.
- Places the address from TAR into SAR.



Note:
See page 6-000 for data flow bit card locations.

CE2E

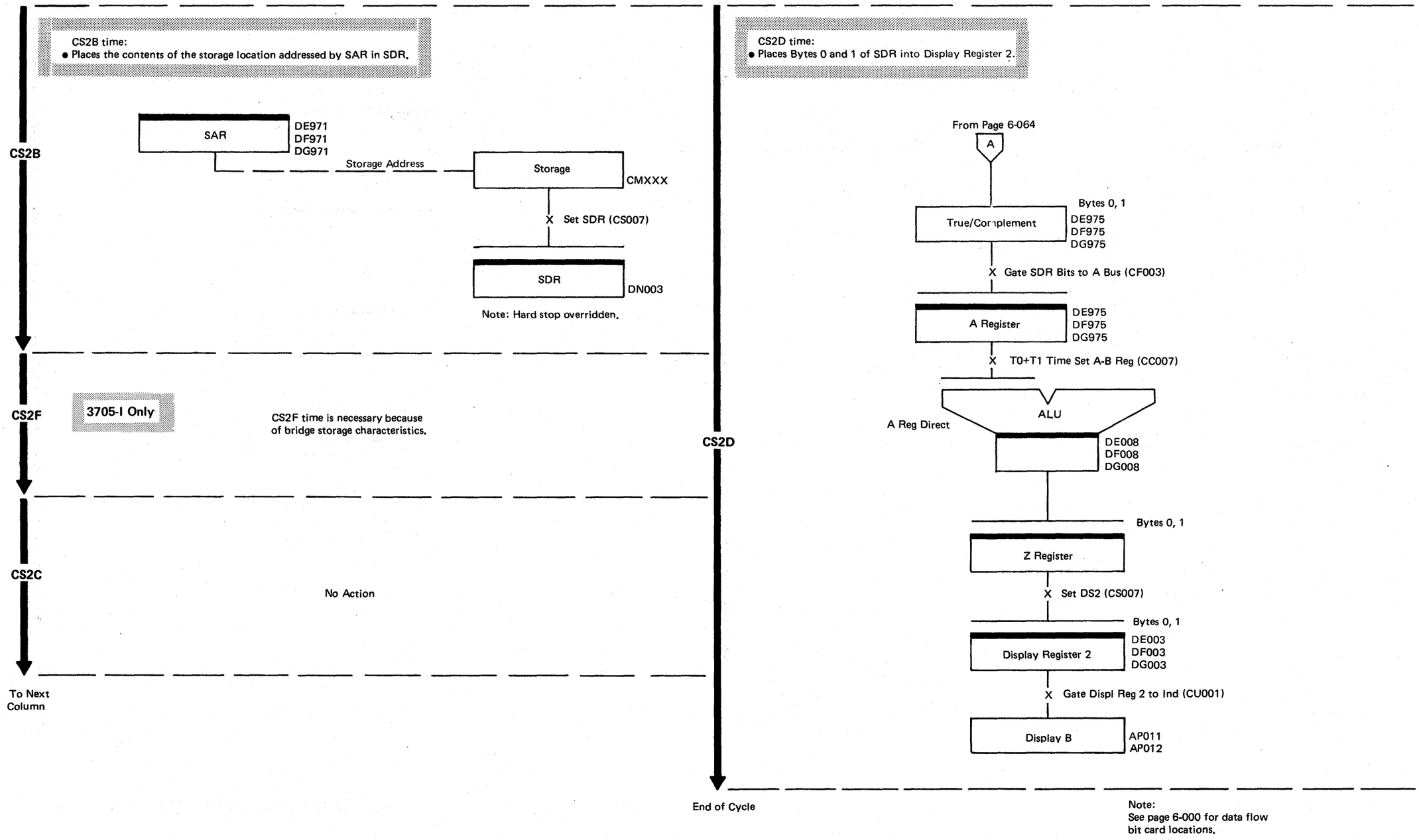
3705-I Only

CS2E time is necessary because of bridge storage characteristics.

To Next Page

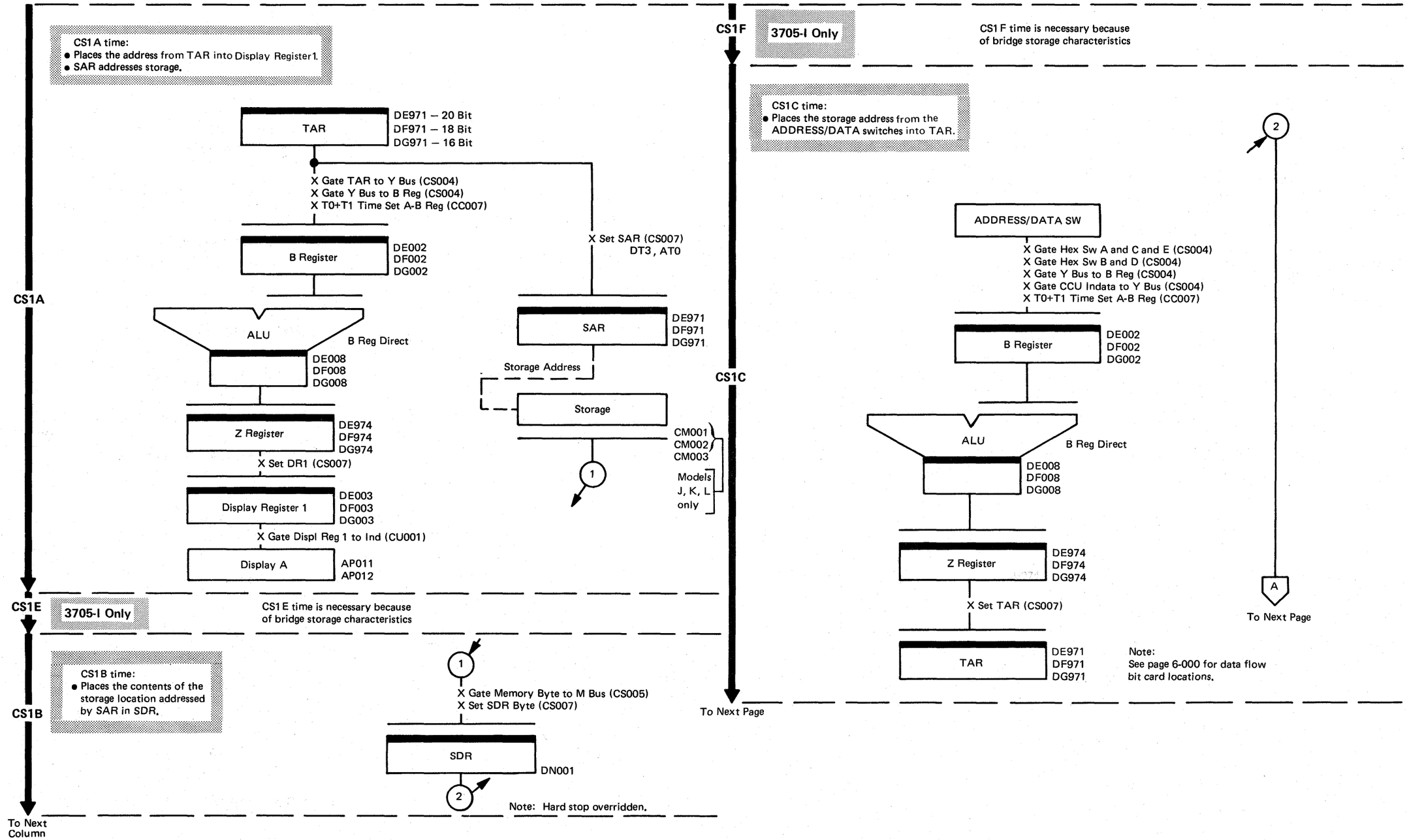
CCU

SINGLE ADDRESS TEST PATTERN (PART 3)



SINGLE ADDRESS SCANNING

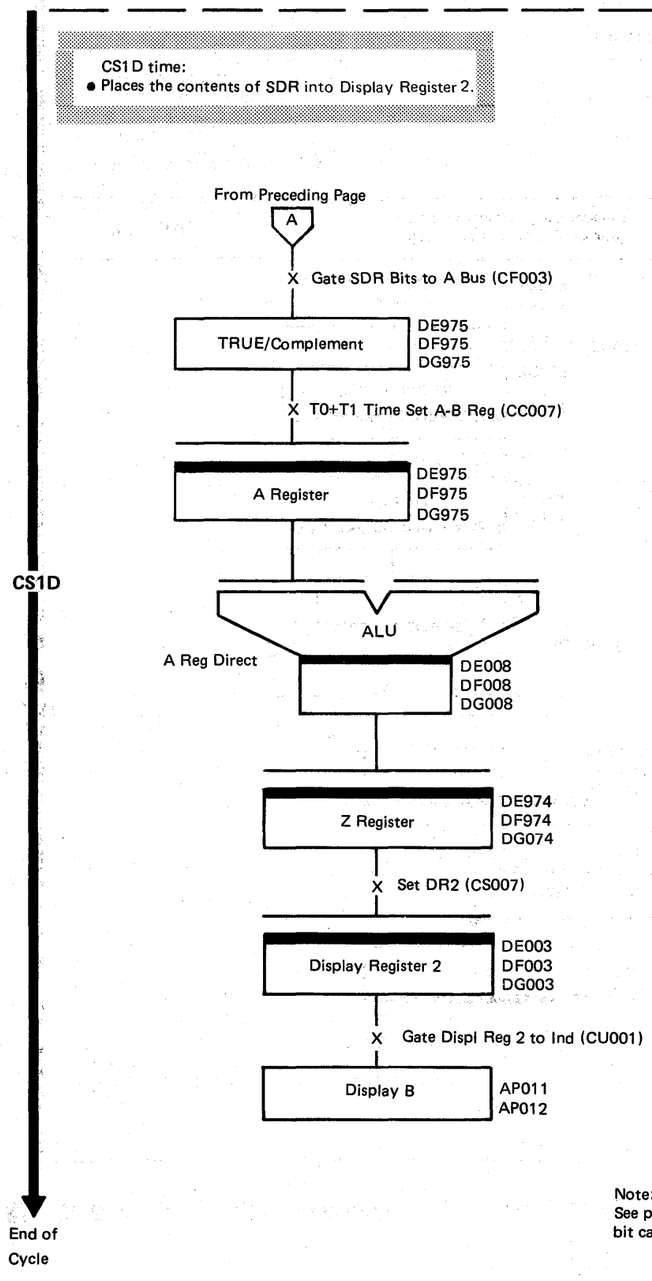
Procedure on page 1-150



CCU

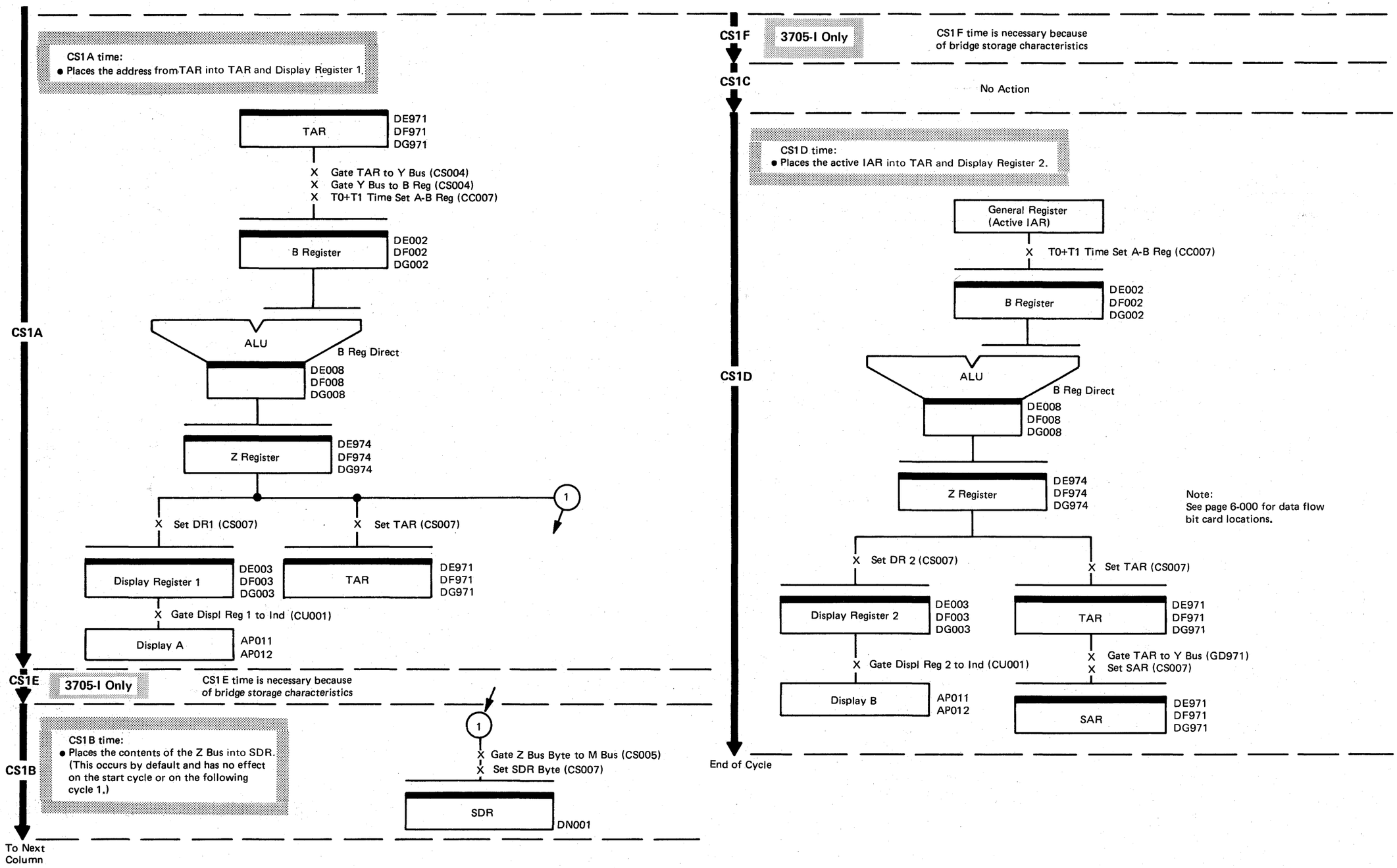
SINGLE ADDRESS SCANNING (PART 1 OF 2)

SINGLE ADDRESS SCANNING (PART 2)

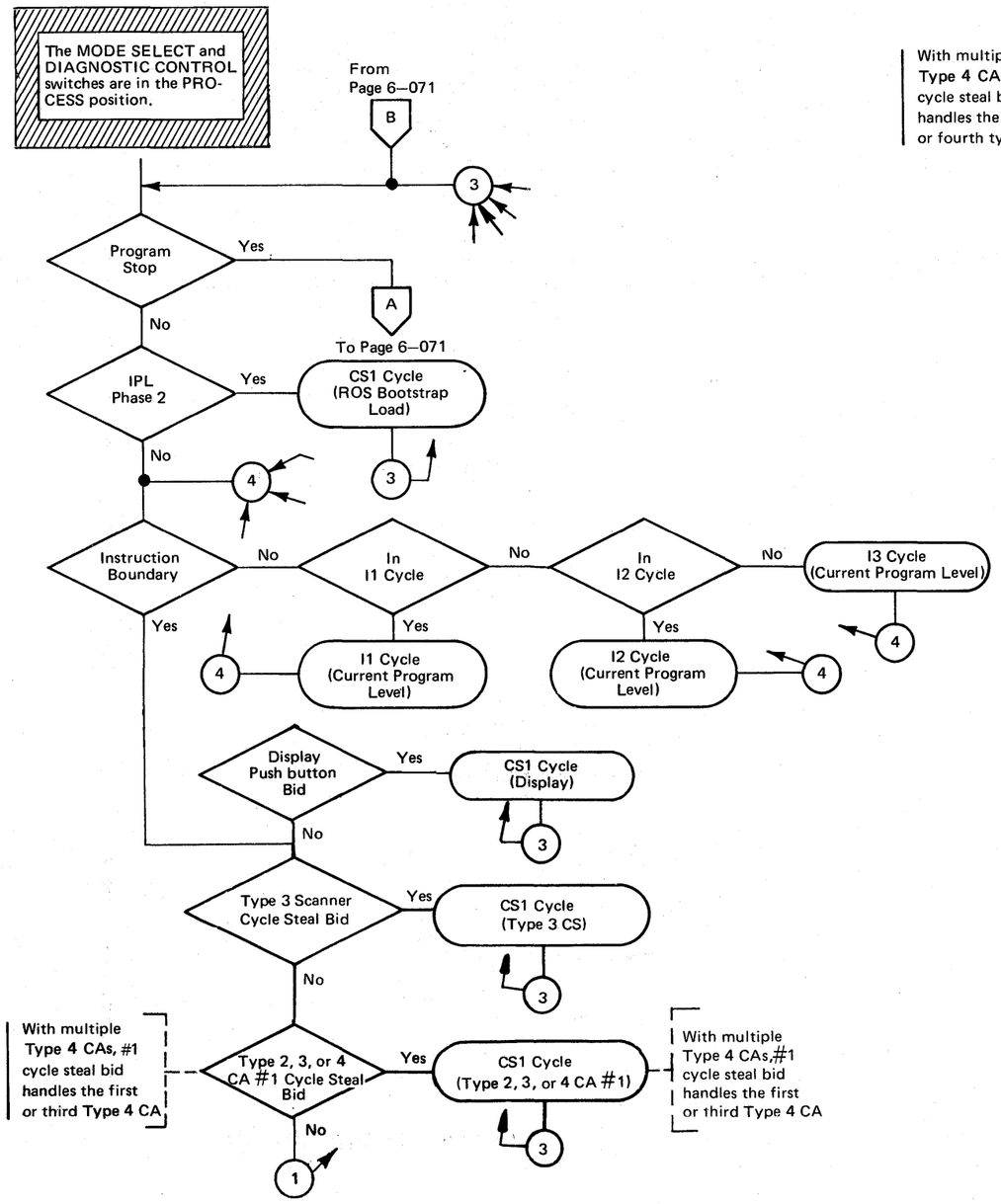


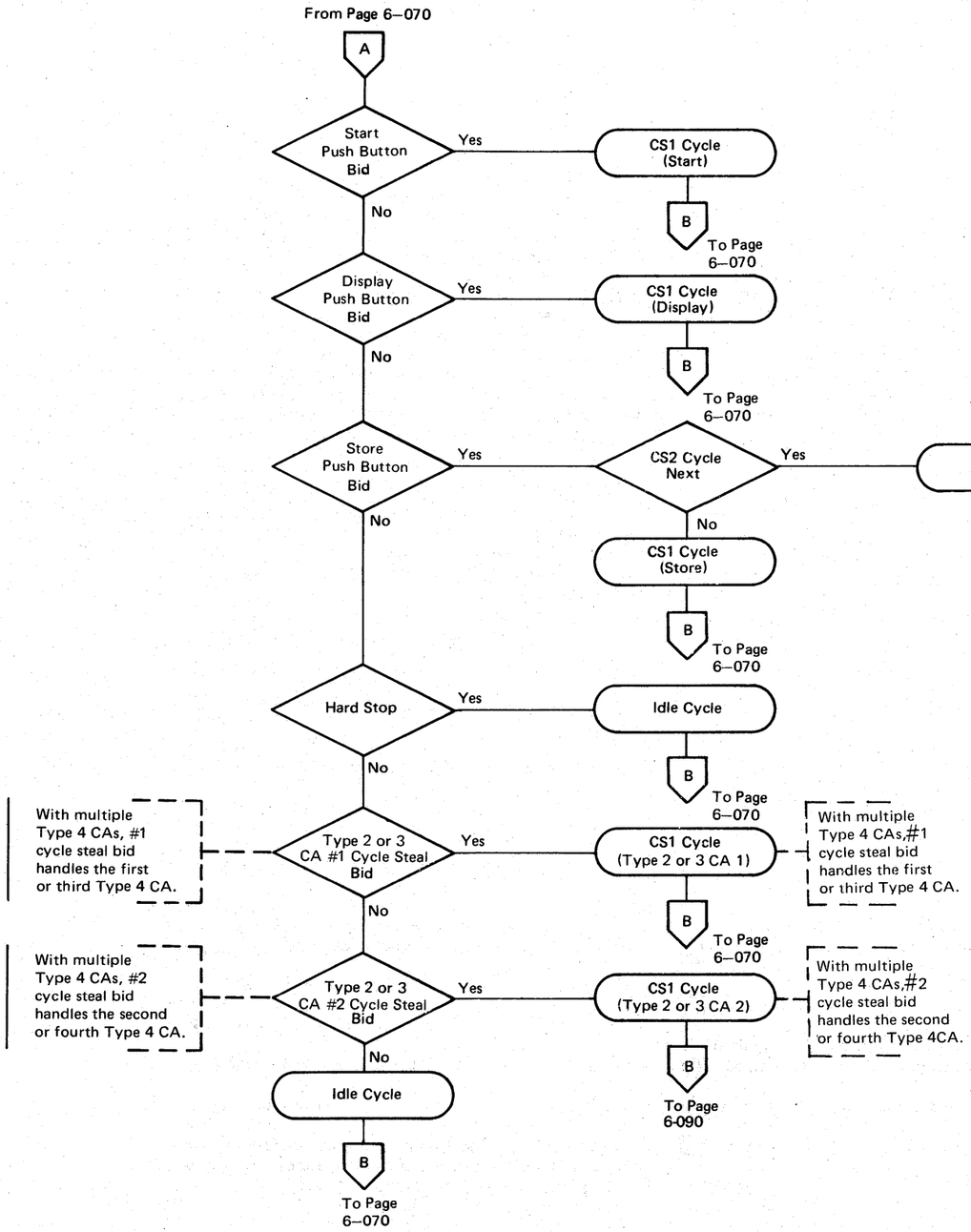
Note:
See page 6-000 for data flow bit card locations.

START PUSHBUTTON OPERATIONS



MACHINE CYCLE PRIORITIES





Changing Machine Priorities
(Masking Program Levels)

CAUTION

Be careful about masking program levels because it disrupts the normal priority structure. It could cause overrun conditions or delay hardware error indications.

Output X'7E' Set Mask Bits (page 6-950) and Output X'7F' Reset Mask Bits (page 6-960) can change the priority structure if they are executed with certain bits on.

When a program level is masked, machine cycles cannot be used for instruction execution at that program level. If level 2, 3, or 4 is active, instruction execution at that program level is allowed to finish before a mask of that level is effective. Only adapter interrupts can be masked in program level 5.

NOTE: The CE can execute Outputs X'7E' and X'7F' from the control panel. (See page 1-160.)

PROGRAM LEVEL PRIORITIES AND INTERRUPTS

Interrupts are caused by adapters or programs initiating hardware-forced branches from lower-priority program levels to higher program levels. The interrupts occur because of:

- Hardware errors
- Hardware service requests
- Program errors
- Program service requests

Machine cycle priorities determine when a level n interrupt can occur. A level n interrupt can occur when all of the following conditions are met:

- No cycle-steal requests are present.
- The program is at the end of an instruction execution (instruction boundary).
- No interrupt requests at a higher priority level are present.
- Program level n is not masked.
- Program level n is not active.

NOTE: Level 1 interrupts in program level 1 cause a re-IPL the first time they occur and a hard stop the second time.

When a level n interrupt occurs, the 'level n interrupt entered' latch sets. Instruction execution at the interrupted level is temporarily suspended until instruction execution is completed at the higher priority level.

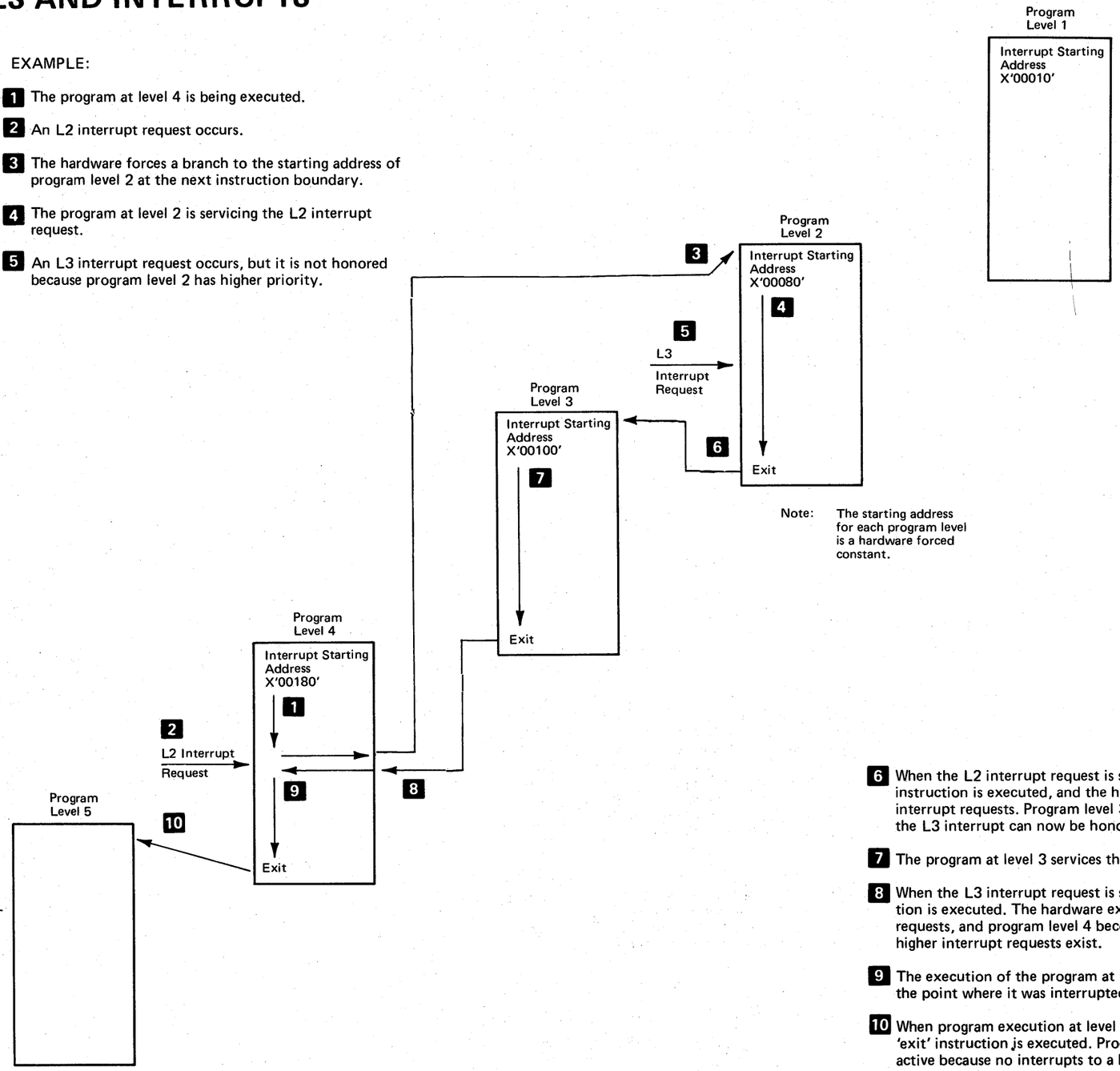
The hardware forces a branch to the storage location that is the starting address for level n.

An 'exit' instruction is executed when the interrupt request has been serviced. The instruction resets the 'level n interrupt entered' latch and allows the machine priority controls to determine which program level should be active next. If no other interrupt requests are pending at a higher priority level, the interrupted program is allowed to continue from the point where it was interrupted. If no interrupt requests are pending at any level, program level 5 becomes active. If level 5 is masked off and no interrupt requests are pending at any level, then an 'exit' instruction will cause the CCU to go into the Wait state (take Idle cycles) until an interrupt occurs. An 'exit' instruction while in level 5 will set a SVC supervisor Call program interrupt to level 4.

The example at the right shows a possible sequence of interrupts.

EXAMPLE:

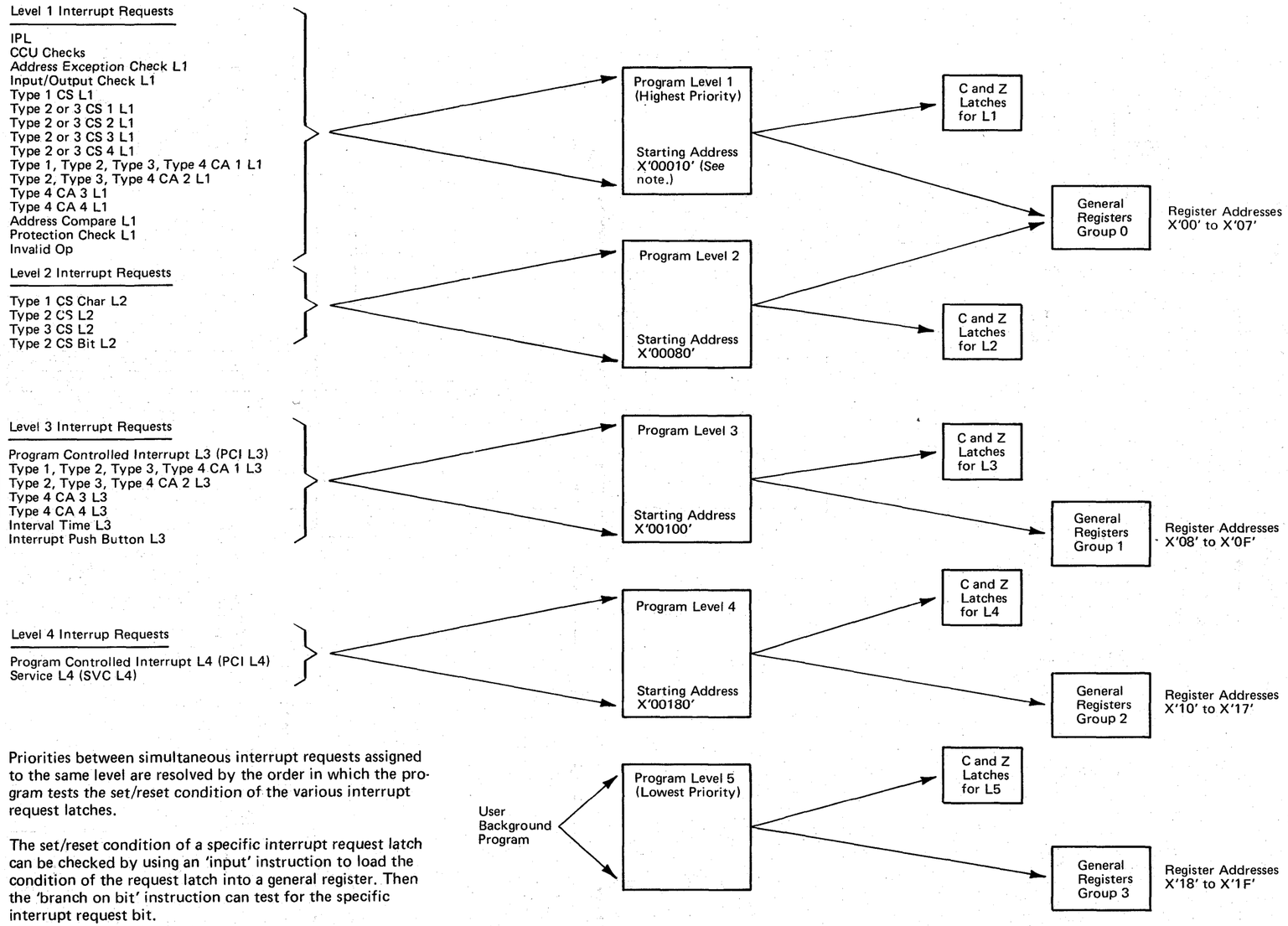
1. The program at level 4 is being executed.
2. An L2 interrupt request occurs.
3. The hardware forces a branch to the starting address of program level 2 at the next instruction boundary.
4. The program at level 2 is servicing the L2 interrupt request.
5. An L3 interrupt request occurs, but it is not honored because program level 2 has higher priority.



Note: The starting address for each program level is a hardware forced constant.

6. When the L2 interrupt request is serviced, an 'exit' instruction is executed, and the hardware examines the interrupt requests. Program level 3 becomes active since the L3 interrupt can now be honored.
7. The program at level 3 services the L3 interrupt request.
8. When the L3 interrupt request is serviced, an 'exit' instruction is executed. The hardware examines the interrupt requests, and program level 4 becomes active since no higher interrupt requests exist.
9. The execution of the program at level 4 continues from the point where it was interrupted.
10. When program execution at level 4 is completed, an 'exit' instruction is executed. Program level 5 is now active because no interrupts to a higher level are pending.

PROGRAM LEVEL PRIORITIES AND INTERRUPTS (PART 2)



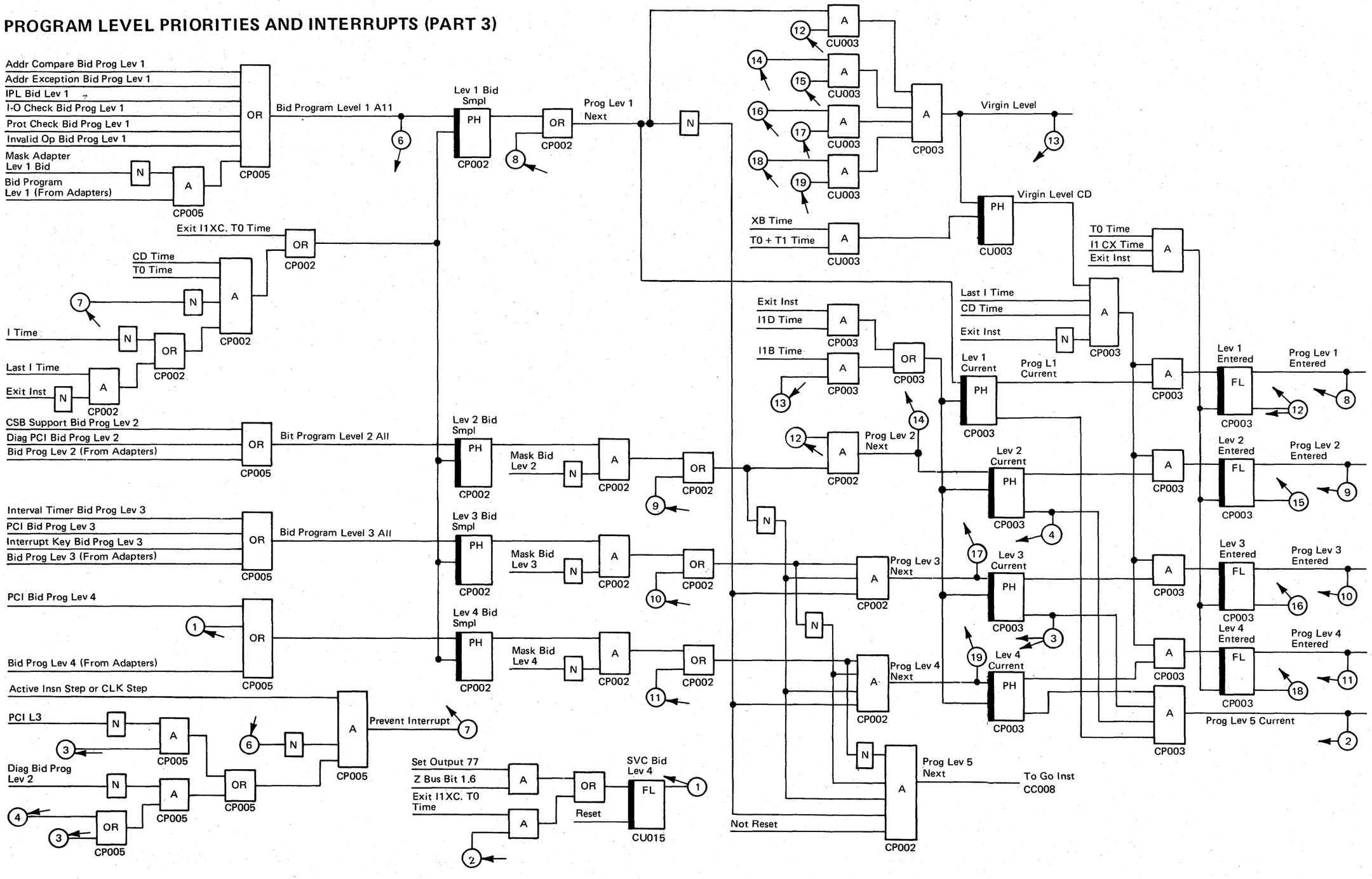
Note: On all IBM programs, Address X'00010' contains a 'store' instruction with the R and B fields equal to 0. This instruction causes the address in the IAR to be placed at the storage location specified by the sum of the displacement field D and the constant X'00780'. Seven more 'store' instructions follow the first 'store' instruction. They store the other seven general registers in the next consecutive address because of the D field value. This allows program levels 1 and 2 to share the same group of general registers See page 6-430 for an explanation of the 'store' instruction.

Priorities between simultaneous interrupt requests assigned to the same level are resolved by the order in which the program tests the set/reset condition of the various interrupt request latches.

The set/reset condition of a specific interrupt request latch can be checked by using an 'input' instruction to load the condition of the request latch into a general register. Then the 'branch on bit' instruction can test for the specific interrupt request bit.

Input X'7E' (page 6-850) loads CCU Interrupt Request Group 1 into a general register; Input X'7F' (page 6-860), CCU Interrupt Request Group 2; Input X'76' (page 6-810), Adapter Interrupt Request Group 1; and Input X'77' (page 6-820), Adapter Interrupt Request Group 2.

PROGRAM LEVEL PRIORITIES AND INTERRUPTS (PART 3)



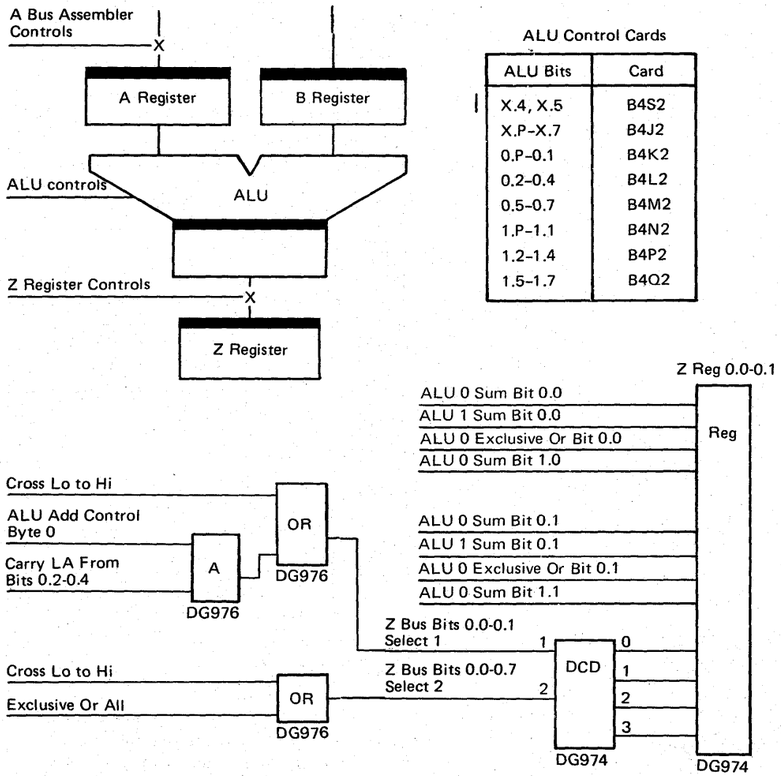
DATA OPERATION CONTROLS

The Arithmetic Logic Unit (ALU) performs all arithmetic and logic functions. It can perform 8 or 16 bit arithmetic (with extended addressing, 18 or 20 bits) in one operation.

The A side of the ALU can be loaded through the A register with the true or the complemented value of SDR, SDR shifted right one bit position, SAR, or hardware generated constants.

The B side of the ALU can be loaded through the B register with the contents of 1 of the 32 general registers or with data from the Y bus.

The chart on this page shows what control lines are active for specific data operations.



ALU Control Cards

ALU Bits	Card
X.4, X.5	B4S2
X.P–X.7	B4J2
0.P–0.1	B4K2
0.2–0.4	B4L2
0.5–0.7	B4M2
1.P–1.1	B4N2
1.2–1.4	B4P2
1.5–1.7	B4Q2

Note: The output of the decode circuit is a binary decode of the two select lines. For example, if 'Z bus bits 0.0-0.7 select 2' is active and 'Z bus bits 0.0-0.1 select 1 is inactive, the binary decode is 2. Therefore, the lines 'ALU 0 exclusive or bit 0.0' and 'ALU 0 exclusive or bit 0.1' are selected to determine the setting of the Z register.

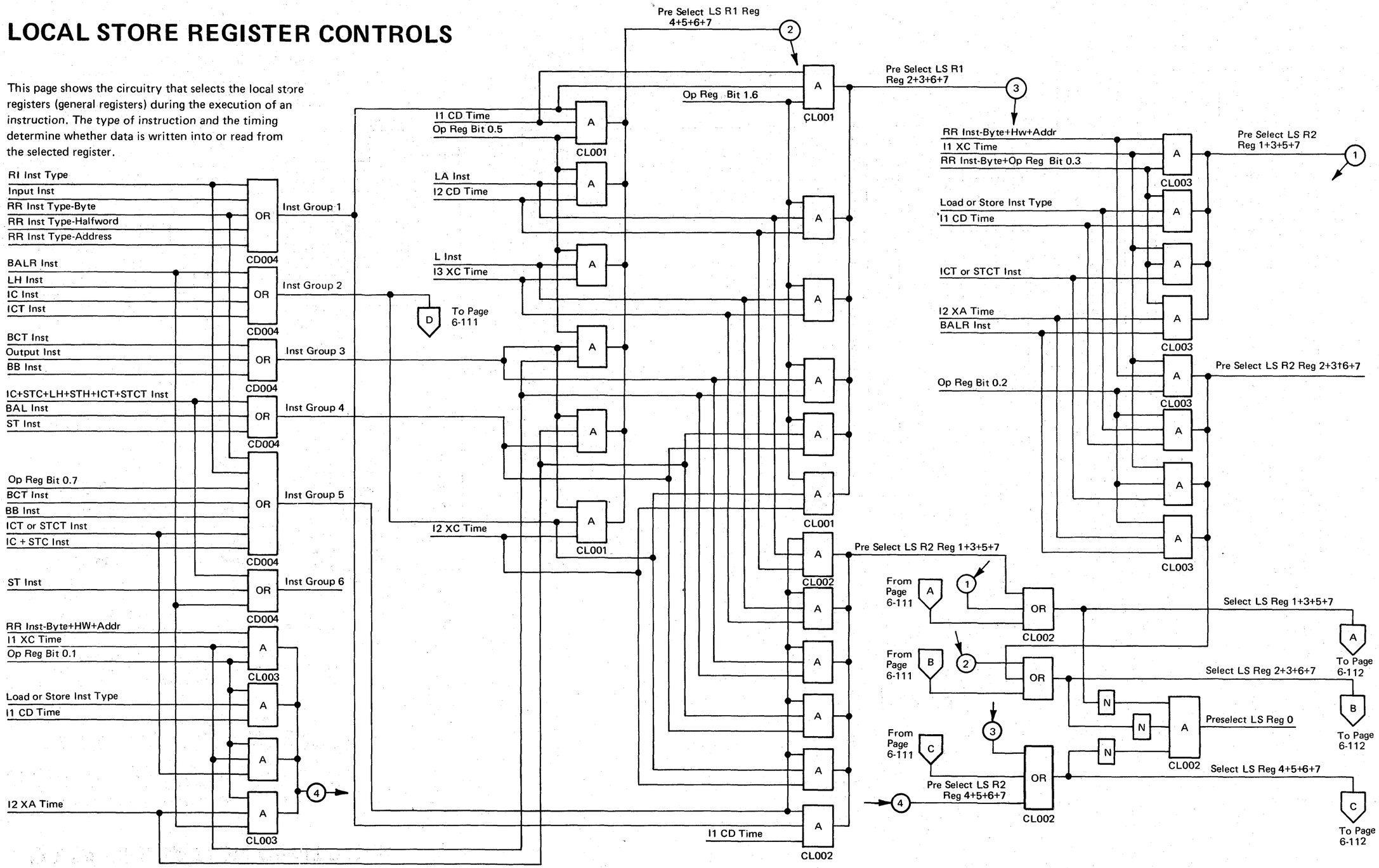
A Bus Assembler Control Lines Cards B3J2 and B4R2 | ALU Control Lines Card B3J2 | Z Register Control Lines Card B3J2

Operation	Complement A Bus (CA004)	Shift Right (CF004)	Shift Right Bit 0.0 (CF004)	Shift Right Bit 1.0 (CF004)	ALU And Control Byte X (CA004)	ALU And Control Byte 0 (CA004)	ALU And Control Byte 1 (CA004)	ALU Or Control Byte X (CA004)	ALU Or Control Byte 0 (CA004)	ALU Or Control Byte 1 (CA004)	ALU Add Control Byte X (CA004)	ALU Add Control Byte 0 (CA004)	ALU Add Control Byte 1 (CA004)	Cross Hi to Lo (CA003)	Cross Lo to Hi (CA003)	Exclusive Or All (CA003)	ALU Add Control Byte X (CA004)	ALU Add Control Byte 0 (CA004)	ALU Add Control Byte 1 (CA004)
A Register Direct (byte 0)	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0
A Register Direct (byte 1)	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0
A Register Direct (bytes 0, 1)	0	0	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0
A Register Direct (bytes X, 0, 1)	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
Add (byte 0)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
Add (byte 1)	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1
Add (bytes 0, 1)	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1
Add (bytes X, 0, 1)	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1
And (byte 0)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
And (byte 1)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
And (bytes 0, 1)	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
And (bytes X, 0, 1)	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
B Register Direct	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Compare (byte 0)	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
Compare (byte 1)	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1
Compare (bytes 0, 1)	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1
Compare (bytes X, 0, 1)	1	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1
Cross Lo to Hi (Byte 1 to Byte 0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Cross Hi to Lo (Byte 0 to Byte 1)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Or (byte 0)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
Or (byte 1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Or (bytes 0, 1)	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
Or (bytes X, 0, 1)	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0
Subtract (byte 0)	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
Subtract (byte 1)	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1
Subtract (bytes 0, 1)	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1
Subtract (bytes X, 0, 1)	1	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1
Xor (byte 0)	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0
Xor (byte 1)	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	1	0	0	0
Xor (bytes 0, 1)	0	0	0	0	0	1	1	0	1	1	0	0	0	0	0	1	0	0	0
Xor (bytes X, 0, 1)	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	1	0	0	0
Shift Right (byte 0)	0	1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0
Shift Right (byte 1)	0	1	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0
Shift Right (bytes 0, 1)	0	1	1	1	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0
Shift Right (bytes X, 0, 1)	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

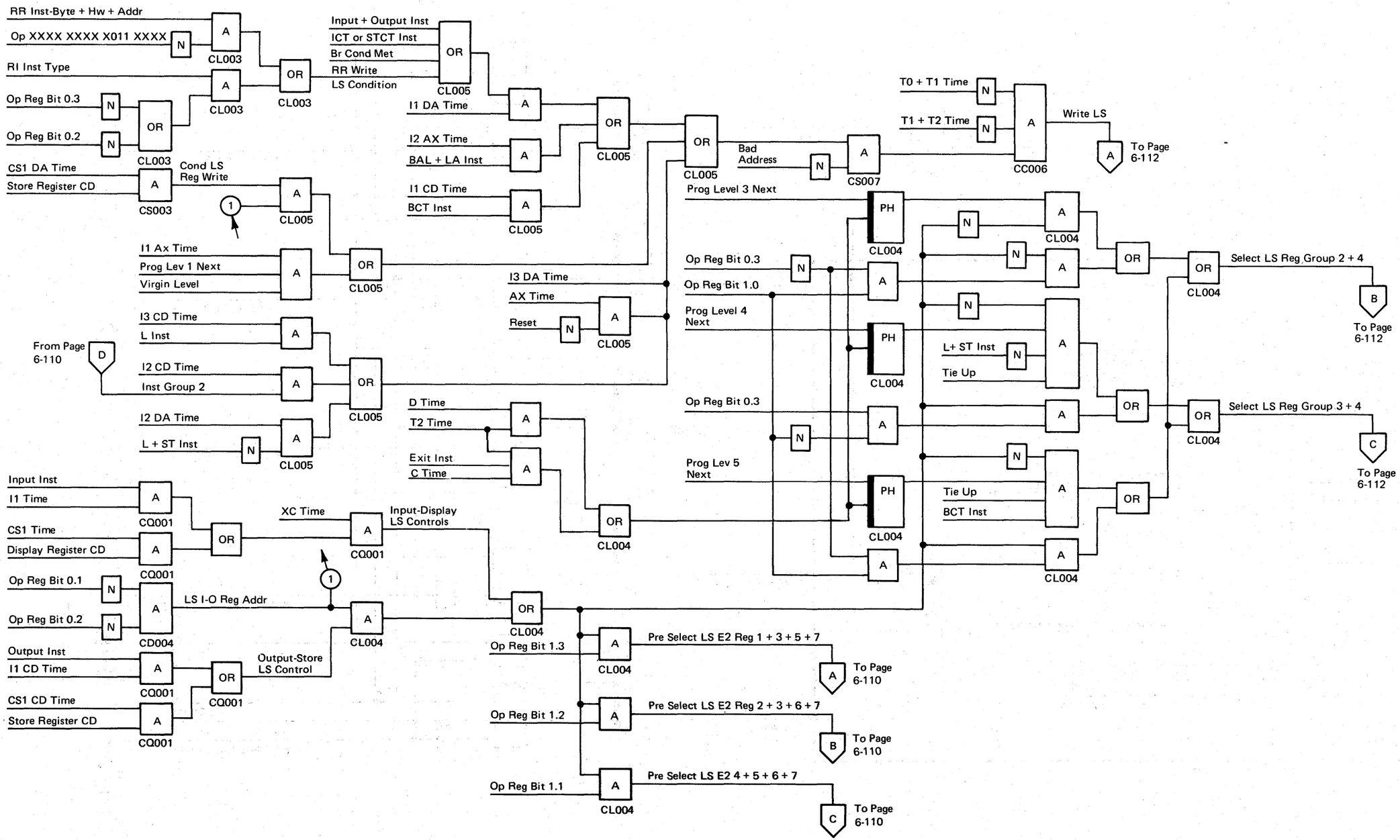
0 = Inactive
1 = Active

LOCAL STORE REGISTER CONTROLS

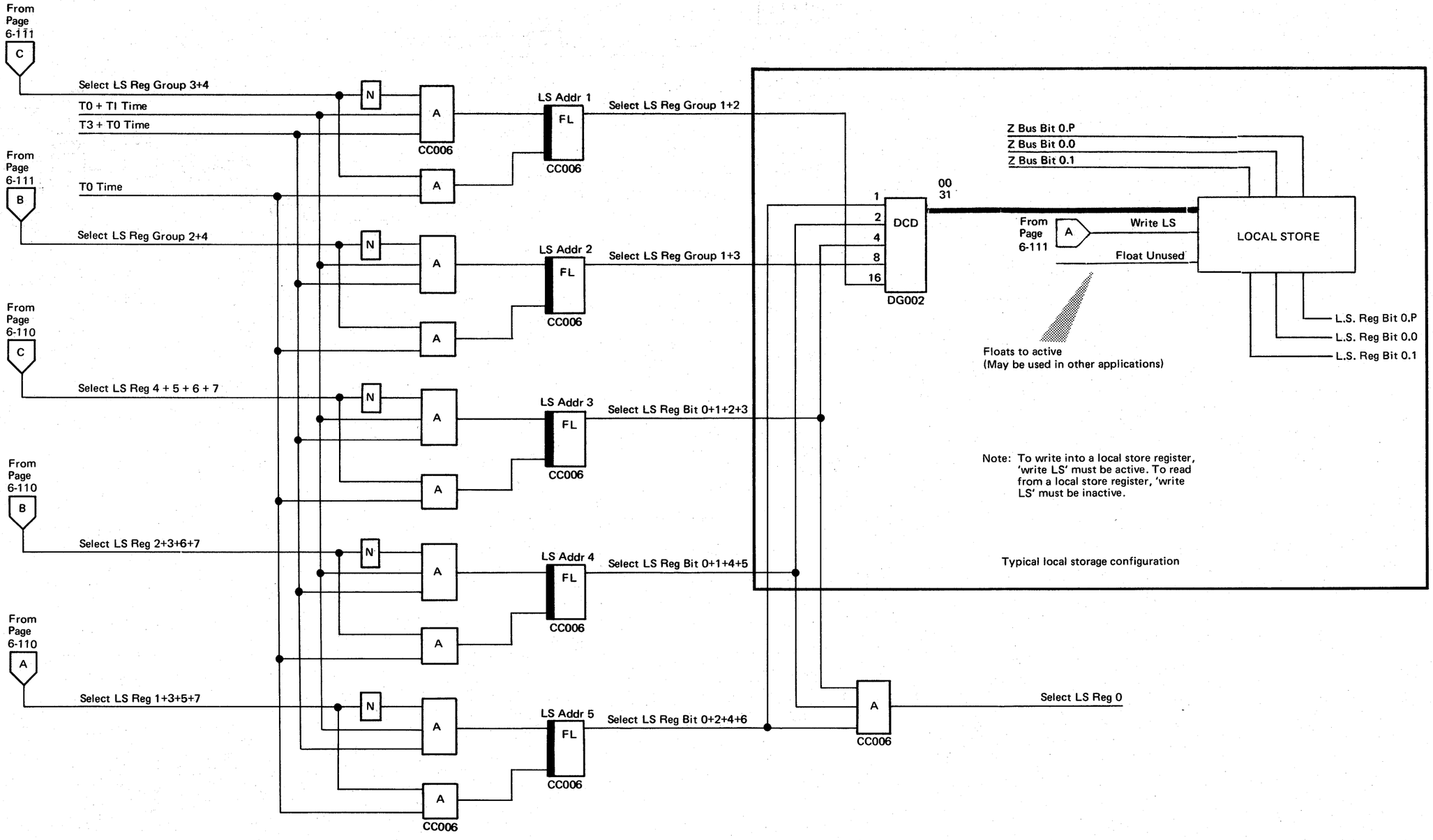
This page shows the circuitry that selects the local store registers (general registers) during the execution of an instruction. The type of instruction and the timing determine whether data is written into or read from the selected register.



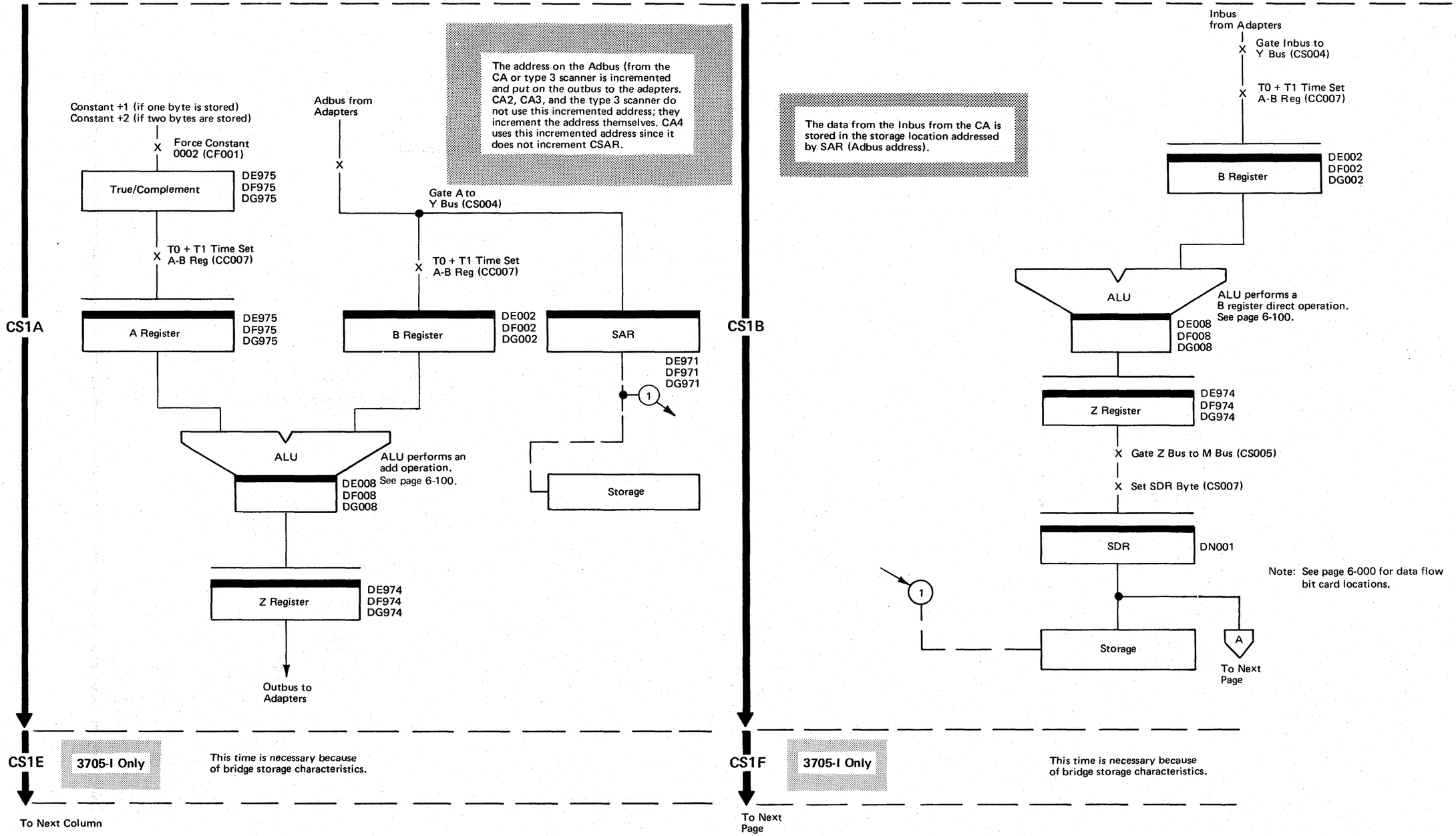
LOCAL STORE REGISTER CONTROLS (PART 2)

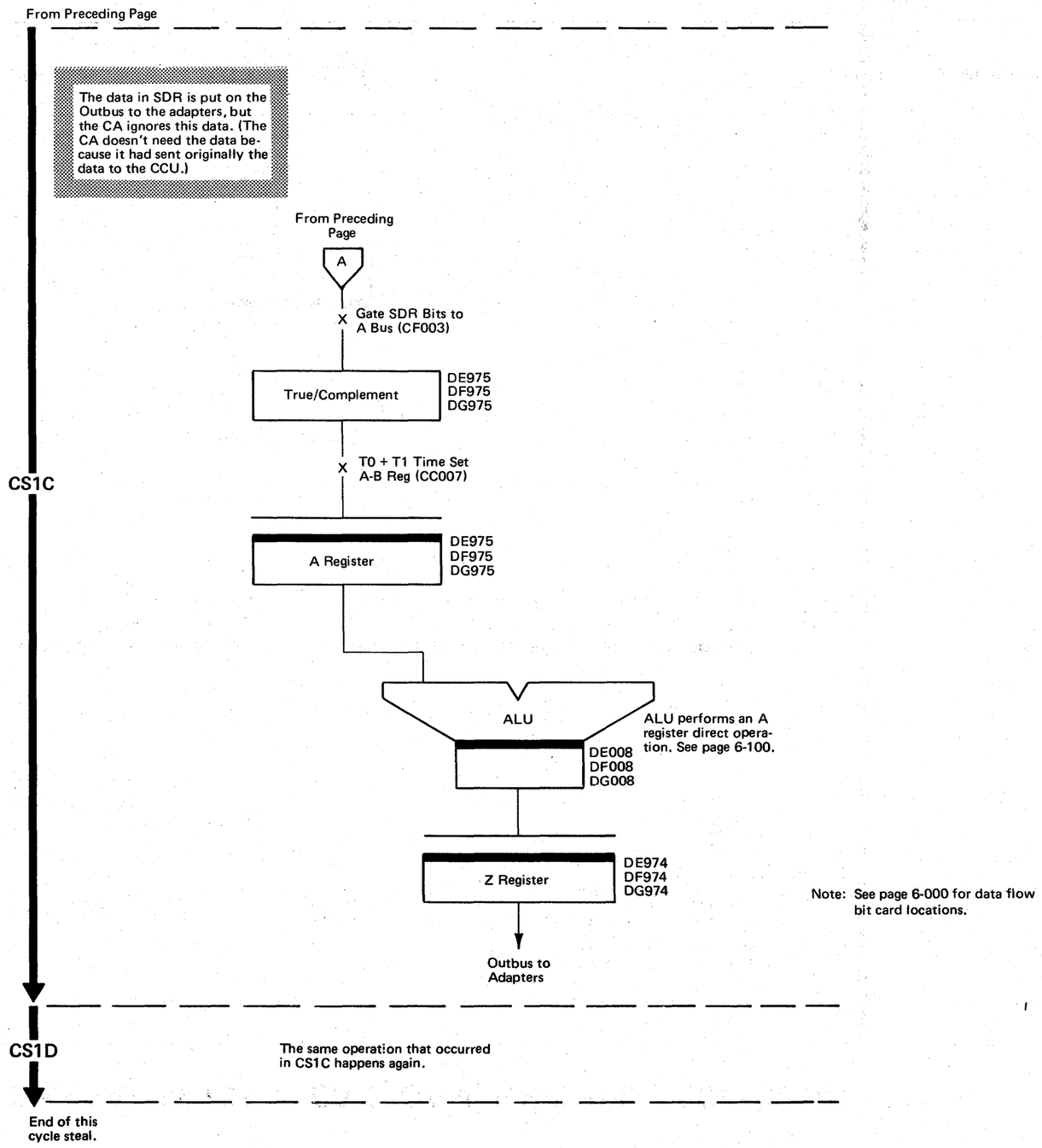


LOCAL STORE REGISTER CONTROLS (PART 3)



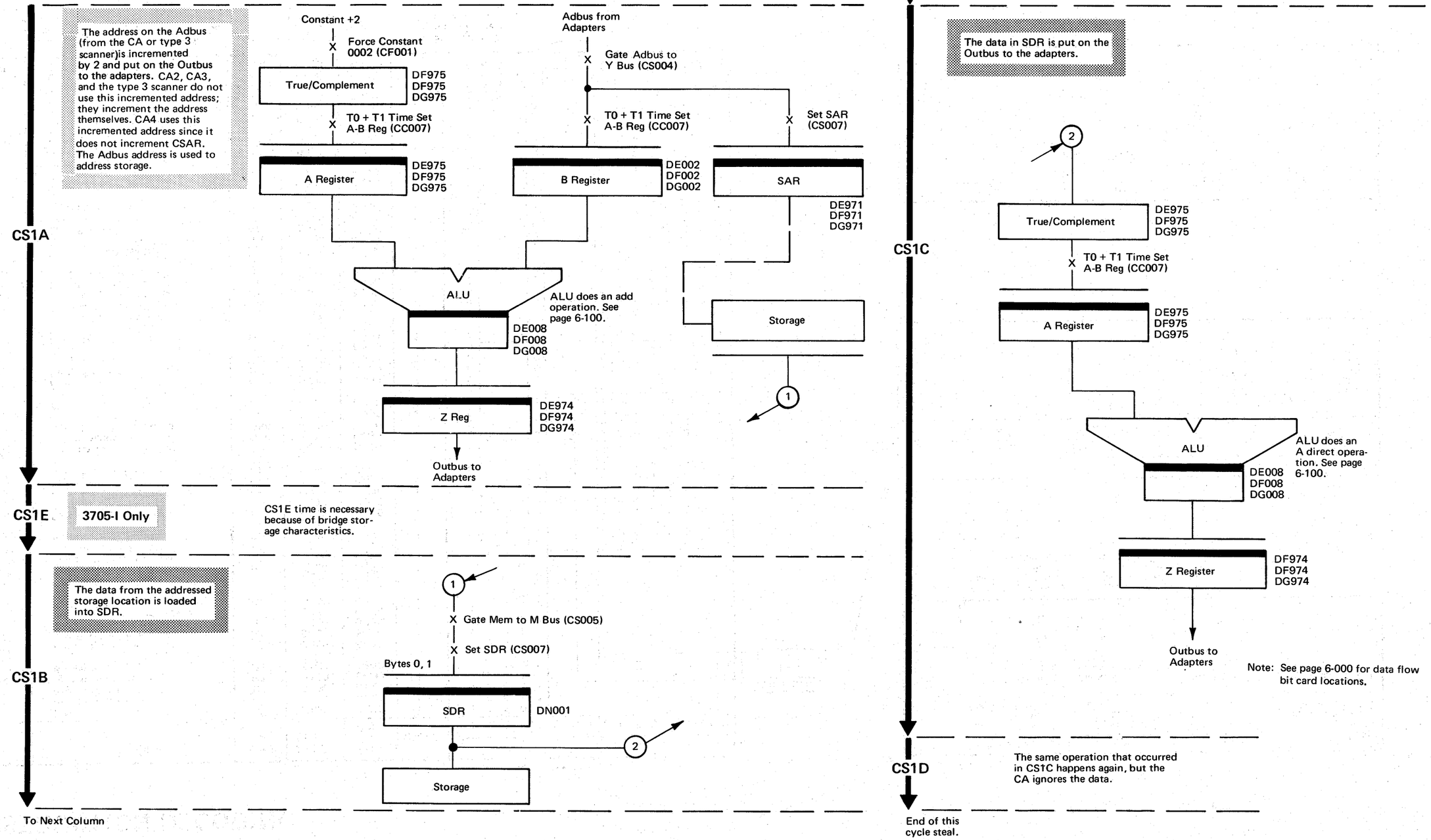
CYCLE STEAL IN (CA 2, CA 3, CA 4, OR TYPE 3 SCANNER)





Note: See page 6-000 for data flow bit card locations.

CYCLE STEAL OUT (CA 2, CA 3, CA 4, OR TYPE 3 SCANNER)



Note: See page 6-000 for data flow bit card locations.

INSTRUCTION DECODING

Abbr.	Instruction	Format Code	FETMM Page	Flow-Chart Page	Cycles	Format
B	Branch	RT	6-630	6-640	1	1 0 1 0 1 T *
BCL	Branch on C Latch	RT	6-630	6-640	1	1 0 0 1 1 T *
BZL	Branch on Z Latch	RT	6-630	6-640	1	1 0 0 0 1 T *
BCT	Branch on Count	RT	6-630	6-680	1	1 0 1 1 1 R N 1 T *
BB****	Branch on Bit	RT	6-630	6-660	1	1 1 M M 1 R N M T *
LRI*	Load Register Immediate	RI	6-160	6-170	1	1 0 0 0 0 R N I
ARI*	Add Register Immediate	RI	6-160	6-170	1	1 0 0 1 0 R N I
SRI*	Subtract Register Immediate	RI	6-160	6-170	1	1 0 1 0 0 R N I
CRI*	Compare Register Immediate	RI	6-160	6-170	1	1 0 1 1 0 R N I
XRI*	Exclusive-Or Register Immediate	RI	6-160	6-170	1	1 1 0 0 0 R N I
ORI*	Or Register Immediate	RI	6-160	6-170	1	1 1 0 1 0 R N I
NRI*	And Register Immediate	RI	6-160	6-170	1	1 1 1 0 0 R N I
TRM*	Test Register Under Mask	RI	6-160	6-170	1	1 1 1 1 0 R N I
LCR*	Load Character Register	RR	6-200	6-220	1	0 0 0 0 0 0 1 0 0 0 R2 N2 R1 N1
ACR*	Add Character Register	RR	6-190	6-220	1	0 0 0 0 0 0 1 1 0 0 0 R2 N2 R1 N1
SCR*	Subtract Character Register	RR	6-210	6-220	1	0 0 0 0 1 0 1 0 0 0 R2 N2 R1 N1
CCR*	Compare Character Register	RR	6-190	6-220	1	0 0 0 1 1 1 0 0 0 0 R2 N2 R1 N1
XCR*	Exclusive Or Character Register	RR	6-200	6-220	1	0 0 1 0 0 1 0 0 0 0 R2 N2 R1 N1
OCR*	Or Character Register	RR	6-210	6-220	1	0 0 1 0 1 1 0 0 0 0 R2 N2 R1 N1
NCR*	And Character Register	RR	6-190	6-220	1	0 0 1 1 0 1 0 0 0 0 R2 N2 R1 N1
LCOR*	Load Character With Offset Reg.	RR	6-200	6-220	1	0 0 1 1 1 1 0 0 0 0 R2 N2 R1 N1
ICT	Insert Character and Count	RSA	6-470	6-480	2	0 0 0 0 1 0 0 0 0 0 R2 N2 B
STCT	Store Character and Count	RSA	6-470	6-520	2	0 0 0 1 1 0 0 0 0 0 R2 N2 B
IC*	Insert Character	RS	6-270	6-290	2	0 1 R N 0 D B
STC	Store Character	RS	6-270	6-330	2	0 1 R N 1 D B
LH*	Load Halfword	RS	6-270	6-290	2	0 0 R 0 D 1 B
STH	Store Halfword	RS	6-270	6-360	2	0 0 R 1 D 1 B
L*	Load	RS	6-270	6-390	3***	0 0 R 0 D 1 0 B
ST	Store	RS	6-270	6-430	3***	0 0 R 1 D 1 0 B
LHR*	Load Halfword Register	RR	6-200	6-220	1	0 0 1 0 0 0 0 0 0 0 R2 R1
AHR*	Add Halfword Register	RR	6-190	6-220	1	0 0 1 0 0 0 0 0 0 0 R2 R1
SHR*	Subtract Halfword Register	RR	6-210	6-220	1	0 0 1 0 1 0 0 0 0 0 R2 R1
CHR*	Compare Halfword Register	RR	6-200	6-220	1	0 0 1 1 0 0 0 0 0 0 R2 R1
XHR*	Exclusive Or Halfword Register	RR	6-200	6-220	1	0 0 1 1 1 0 0 0 0 0 R2 R1
OHR*	Or Halfword Register	RR	6-210	6-220	1	0 0 1 1 0 0 0 0 0 0 R2 R1
NHR*	And Halfword Register	RR	6-190	6-220	1	0 0 1 1 1 0 0 0 0 0 R2 R1
LHOR*	Load Halfword With Offset Reg.	RR	6-200	6-220	1	0 0 1 1 1 1 0 0 0 0 R2 R1
LR*	Load Register	RR	6-210	6-220	1	0 0 1 0 0 0 0 0 0 0 R2 R1
AR*	Add Register	RR	6-190	6-220	1	0 0 1 0 1 1 0 0 0 0 R2 R1
SR*	Subtract Register	RR	6-210	6-220	1	0 0 1 1 0 1 0 0 0 0 R2 R1
CR*	Compare Register	RR	6-200	6-220	1	0 0 1 1 1 1 0 0 0 0 R2 R1
XR*	Exclusive Or Register	RR	6-200	6-220	1	0 0 1 1 0 0 1 0 0 0 R2 R1
OR*	Or Register	RR	6-210	6-220	1	0 0 1 1 1 1 0 0 0 0 R2 R1
NR*	And Register	RR	6-190	6-220	1	0 0 1 1 1 0 1 0 0 0 R2 R1
LOR*	Load With Offset Register	RR	6-210	6-220	1	0 0 1 1 1 1 1 0 0 0 R2 R1
BALR	Branch and Link Register	RR	6-190	6-240	2	0 0 1 0 0 0 0 0 0 0 R2 R1
IN	Input	RE	6-700	6-710	1	0 0 1 1 0 0 0 0 0 0 R2 Ex** R1 Ey**
OUT	Output	RE	6-700	6-730	1	0 0 1 1 1 0 0 0 0 0 R2 Ex** R1 Ey**
BAL	Branch and Link	RA	6-560	6-570	2	1 0 1 1 1 0 0 0 0 R A (16–31)
LA	Load Address	RA	6-560	6-600	2	1 0 1 1 1 0 0 1 0 R A (16–31)
EXIT	Exit	Exit	6-700	6-750	1	1 0 1 1 1 0 0 0 0 1 0 0 0 0 0

*	DISP (HW)
0	1 + T
1	1 – T

* These instructions can change the C and Z condition latches.

**See page 6-151 for a decode of the E Field.

*** These are 2-cycle instructions without extended addressing.

**** See page 6-630 for a decode of the M Field

BYTE SELECTION DECODING

Instr. Bits 1 2 3	R2 N2 Fields: LCR, ACR, SCR, CCR, OCR, XCR, NCR, LCOR	B Field: ICT, STCT, IC, STC, LH, STH, L, ST	R2 Field: LR, AR, SR, CR, OR, XR, NR, LOR, BALR	R2 Field: LHR, AHR, SHR, CHR, OHR, XHR, NHR, LHOR
0 0 0	Reg. 1; Byte 0	See Note 1	Reg. 0; Byte 0, 1	Reg. 0; Byte X, 0, 1
0 0 1	1 1	Reg. 1; Byte X, 0, 1	1	1
0 1 0	3 0	2	2	2
0 1 1	3 1	3	3	3
1 0 0	5 0	4	4	4
1 0 1	5 1	5	5	5
1 1 0	7 0	6	6	6
1 1 1	7 1	7	7	7

Note 1. X'000' specifies the address constant for IC, STC, LH, STH, L, and ST instructions. (See the descriptions of these instructions for the value of the address constant.) X'000' specifies register 0, bytes X, 0, and 1 for ICT and STCT instructions.

Instr. Bits 5 6 7	R, N Fields: LRI, CRI, ORI, XRI, NRI, TRM, BB ICT, STCT, IC, STC	R1, N1 Fields: LCR, CCR, OCR, XCR, NCR, LCOR	R, N Fields: ARI, SRI, BCT	R1, N1 Fields: ACR, SCR
0 0 0	Reg. 1; Byte 0	Reg. 1; Byte 0	Reg. 1; Byte 0	Reg. 1; Byte 0
0 0 1	1 1	1 1	1 0, 1	1 0,1
0 1 0	3 0	3 0	3 0	3 0
0 1 1	3 1	3 1	3 0, 1	3 0,1
1 0 0	5 0	5 0	5 0	5 0
1 0 1	5 1	5 1	5 0, 1	5 0,1
1 1 0	7 0	7 0	7 0	7 0
1 1 1	7 1	7 1	7 0, 1	7 0,1

Instr. Bits 5 6 7	R Field: LH, STH	R1 Field: LHR, AHR, SHR, CHR, OHR, XHR, NHR, LHOR	R1 Field: LR, AR, SR, CR, OR, XR, NR, LOR, BALR	R Field: BAL, LA, IN, OUT, L, ST
0 0 0	See Note 3	Reg. 0; Bytes 0, 1	Reg. 0; Byte X, 0, 1	See Note 2
0 0 1	Reg. 1; Byte 0, 1	1	1	Reg. 1; Byte X, 0, 1
0 1 0	2	2	2	2
0 1 1	3	3	3	3
1 0 0	4	4	4	4
1 0 1	5	5	5	5
1 1 0	6	6	6	6
1 1 1	7	7	7	7

Note 2. X'000' specifies register 0, bytes X, 0, and 1 for L, BAL, LA, IN, and OUT instructions. X'000' specifies a 0 constant (20 bits) for ST.

Note 3. X'000' specifies register 0, bytes 0 and 1 for LH. X'000' specifies a 0 constant (16 bits) for STH.

INPUT REGISTER ADDRESSES

E Field XY	Register/Function		FETMM Page
00	Gen Reg, Group 0	Reg 0	6-770
01		Reg 1	6-770
02		Reg 2	6-770
03		Reg 3	6-770
04		Reg 4	6-770
05		Reg 5	6-770
06		Reg 6	6-770
07		Reg 7	6-770
08	Gen Reg, Group 1	Reg 0	6-770
09		Reg 1	6-770
0A		Reg 2	6-770
0B		Reg 3	6-770
0C		Reg 4	6-770
0D		Reg 5	6-770
0E		Reg 6	6-770
0F		Reg 7	6-770
10	Gen Reg, Group 2	Reg 0	6-770
11		Reg 1	6-770
12		Reg 2	6-770
13		Reg 3	6-770
14		Reg 4	6-770
15		Reg 5	6-770
16		Reg 6	6-770
17		Reg 7	6-770
18	Gen Reg, Group 3	Reg 0	6-770
19		Reg 1	6-770
1A		Reg 2	6-770
1B		Reg 3	6-770
1C		Reg 4	6-770
1D		Reg 5	6-770
1E		Reg 6	6-770
1F		Reg 7	6-770
20-3F	A constant of all zeros is loaded into R, and the CCU sets the input/output check L1 request.		

Note: Inputs and Outputs X'50'-X'5F' are for the type 2 or type 3 CA.

Inputs and Outputs X'60'-X'67' are for the type 1 and 4 CA.

* Inputs and Outputs X'68, 69, 6A, 6B' are used for the remote loader on a REMOTE 3705.

** Inputs and Outputs X'6C'-X'6F' are for the type 4 CA.

E Field XY	Register/Function	FETMM Page
48-4F	A constant of all zeros is loaded into R, and the CCU sets the input/output check L1 request.	
50	INCWAR	9-110
51	OUTCWAR	9-120
52	Control Word Byte Count	9-120
53 T	Sense Register	9-150
54 2	Status Register	9-160
55 C	Control Register	9-180
56 A	Check Register	9-200
57 &	Unused	
58 T	Chnl Bus Out Diag Reg	9-220
59 3	Cycle Steal Address Reg	9-230
5A C	Chnl Adapter Data Buffer	9-240
5B A	Chnl Tag Diagnostic Reg	9-250
5C	CMDR Reg	9-260,G-060
5D	Unused	
5E	Unused	
5F	Unused	
60	Initial Selection Control	8-070,H-050
61	Initial Selection Address & Command	8-070,H-050
62	Data/Status Control	8-090,H-070
63 T	Address and ESC Status	8-100,H-080
64 1	Data Buffer Bytes 1, 2	8-110,H-090
65 C	Data Buffer Bytes 3, 4	8-110,H-090
66 A	NSC Status Byte	8-120,H-100
67 &	Control	8-130,H-110
*68 T	Level 1 Status	
*69 4	Level 3 Status	
*6A C	Parallel Data Register	
*6B A	Control Pgm Load Reg	
**6C	CA4 EB Mode Control Reg	H-130
**6D	CA4 EB Mode Data Buffer	H-150
**6E	CA4-CS Register and CSAR Byte X	H-170
**6F	CA4-CSAR Byte 0/1	H-170
70	Storage Size Installed	6-770
71	Panel Address/Data Digits	6-780
72	Display/Function Select Switch	6-790
73	Insert Key	6-800
74	LAR	6-800
75	A constant of all zeros is loaded into R.	
76 C	Adapter Interrupt Request Group 1	6-810
77 C	Adapter Interrupt Request Group 2	6-820
78 U	A constant of all zeros is loaded into R.	
79	Utility	6-830
7A	Cycle Utilization Counter Register	6-831
7B	BSC CRC Register	6-840
7C	Reserved	
7D	CCU Check Register	6-841
7E	CCU Level 1 Interrupt Requests	6-850
7F	CCU Level 2 Interrupt Requests	6-860

E Field XY	Register/Function Type 1 Scanner	FETMM Page	Register/Function Type 2 Scanner	FETMM Page	Register/Function Type 3 Scanner	FETMM Page
40	Unused		Interface Address	B-120	Interface Address	F–180
41	Interface Address	A-140	Unused		High Speed Select	F–190
42	Cntl A	A-150	Unused		DBAR/Check Register 0	F–190
43	Cntl B/C	A-180	Check Register	B-130	Check Register 1	F–200
44	Status	A-120	ICW Input Reg 0-15	B-140	SCF/PDF Array Byte	F–210
45	Unused		ICW Input Reg 16-31	B-140	LCD/PCF/SDF	F–210
46	Unused		Display Register	B-150	Display Register	F–220
47	Unused		ICW Input Reg 32-45	B-140	ICW Bytes 4 and 5	F–210
48	Unused		Unused		CS Control and Byte Count	F–230
49	Unused		Unused		CSAR	F–230
4A	Unused		Unused		Old BCC	F–230
4B	Unused		Unused		EPCF	F–240
4C	Unused		Unused		PDF Array Bits 0.5-1.7	F–240
4D	Unused		Unused		Not Used	
4E	Unused		Unused		ICW Control	F–240
4F	Unused		Unused		Status	F–240

OUTPUT REGISTER ADDRESSES

E Field XY	Register/Function		FETMM Page
00	Gen Reg, Group 0	Reg 0	6-870
01		Reg 1	6-870
02		Reg 2	6-870
03		Reg 3	6-870
04		Reg 4	6-870
05		Reg 5	6-870
06		Reg 6	6-870
07		Reg 7	6-870
08	Gen Reg, Group 1	Reg 0	6-870
09		Reg 1	6-870
0A		Reg 2	6-870
0B		Reg 3	6-870
0C		Reg 4	6-870
0D		Reg 5	6-870
0E		Reg 6	6-870
0F		Reg 7	6-870
10	Gen Reg, Group 2	Reg 0	6-870
11		Reg 1	6-870
12		Reg 2	6-870
13		Reg 3	6-870
14		Reg 4	6-870
15		Reg 5	6-870
16		Reg 6	6-870
17		Reg 7	6-870
18	Gen Reg, Group 3	Reg 0	6-870
19		Reg 1	6-870
1A		Reg 2	6-870
1B		Reg 3	6-870
1C		Reg 4	6-870
1D		Reg 5	6-870
1E		Reg 6	6-870
1F		Reg 7	6-870
20-3F	The bits of R are ignored, and the CCU sets the input/output check L1.		

E Field XY	Register/Function	FETMM Pages
50	INCWAR	9-110
51	OUTCWAR	9-120
52	The bits of R are ignored.	
53 T	Set Sense Register Bits	9-140
54 2	Set Status Register Bits	9-160
55 C	Set Control Register Bits	9-180
56 A	Rst Control Register Bits	9-180
57 &	Chnl Adapter Mode Reg	9-210
58 T	Chnl Bus Out Diag Reg	9-220
59 3	Type 3 CA Diag Busy	G-050
5A C	Chnl Adapter Data Buffer	9-240
5B A	Chnl Tag Diagnostic Reg	9-250
5C	Unused	
5D	Unused	
5E	Unused	
5F	Unused	
60	Reset Initial Selection	8-070
61	Unused	
62	Data/Status Control	8-080,H-060
63 T	Address and ESC Status	8-100,H-080
64 1	Data Buffer Bytes 1, 2	8-110,H-090
65 C	Data Buffer Bytes 3, 4	8-110,H-090
66 A	NSC Status Byte	8-120,H-100
67 &	Control	8-130,H-120
*68 T	Control	
*69 4	Read/Write	
*6A C	Parallel Data Register	
*6B A	Control Pgm Load Reg	
**6C	CA4 EB Mode Control Reg	H-140
**6D	CA4 EB Mode Data Buffer	H-160
**6E	CA4-CSAR Byte X	H-180
**6F	CA4-CSAR Byte 0/1	H-180
70	Hardstop	6-870
71	Display Reg 1	6-870
72	Display Reg 2	6-870
73	Set Key	6-880
74-76	The bits of R are ignored.	
77 C	Miscellaneous Control	6-900
78 C	Force CCU Checks	6-920
79 U	Utility	6-930
7A	The bits of R are ignored.	6-940
7B	The bits of R are ignored.	
7C	Set PCI L3	6-940
7D	Set PCI L4	6-940
7E	Set Mask Bits	6-940
7F	Reset Mask Bits	6-950

E Field XY	Register/Function Type 1 Scanner	FETMM Page	Register/Function Type 2 Scanner	FETMM Page	Register/Function Type 3 Scanner	FETMM Page
40	Reset Char Service Pending	A-230	Interface Address	B-160	Interface Address	F–250
41	Start Scanner, Reset Bid L2	A-240	Adr Substitution Ctrl	B-160	HS Sel Reg, Sub Ctrl Reg	F–250
42	Control A	A-250	Upper Scan Limit Ctrl	B-170	DBAR/Scan Limit Ctrl	F–260
43	Control B	A-280	Control	B-170	Control	F–270
44	General Control	A-300	ICW 0-15	B-180	SCF/PDF Array Byte	F–280
45	Scanner Control	A-310	ICW 16-23	B-190	LCD/PCF/EPCF	F–290
46	Set Char Service Pending	A-320	ICW 24-33, 44	B-200	SDF	F–300
47	Force Bid L2 Request	A-330	ICW 34-43	B-210	MISC ICW Bits	F–310
48	The bits of R are ignored and the CCU sets the input/output check L1 request.				CS Control and Byte Count	F–320
49					CSAR	F–320
4A					Old BCC	F–320
4B					Reserved	
4C					PDF Array Bits 0.5-1.7	F–330
4D					ICW Cycle Steal PDFs	F–330
4E					CS/PDF Pointers, ICW Control	F–340
4F					Status	F–350

REGISTER IMMEDIATE (RI) INSTRUCTIONS

The CCU takes one I1 cycle to execute each of the eight 'register immediate' instructions. The same sequence occurs during I1A, I1B, and I1C times for each of the instructions; only the sequence during I1D is different.

For all 'register immediate' instructions, the general register designated by the R field in the instruction must be an odd-numbered register.

ADD REGISTER IMMEDIATE (ARI)

0	1	2	3	4	5-6	7	8-15
1	0	0	1	0	R	N	I

The data in the I field is added to byte 0 (N=0) or bytes 0 and 1 (N=1) of the general register designated by the R field. The register specified must be an odd-numbered register. The result is stored in the selected byte(s) of the general register. If N=0, byte 1 of R remains unchanged.

The 'C' latch sets if N=0 and byte 0 of R overflows, or if N=1 and bytes 0 and 1 overflow. The 'Z' latch sets if N=0 and byte 0 of R equals 0, or if N=1 and bytes 0 and 1 of R equal 0.

With Extended Addressing, byte X of the general register is included in the addition if N=1, but byte X does not affect the setting of the C and Z latches.

AND REGISTER IMMEDIATE (NRI)

0	1	2	3	4	5-6	7	8-15
1	1	1	0	0	R	N	I

The data in the I field is ANDed with byte 0 (N=0) or byte 1 (N=1) of the general register designated by the R field. This register must be an odd-numbered register. The results are stored in the selected byte of R. The non-selected byte of the register remains unchanged.

The 'C' latch sets if the selected byte of R does not equal 0. The 'Z' latch sets if the selected byte of R equals 0.

COMPARE REGISTER IMMEDIATE (CRI)

0	1	2	3	4	5-6	7	8-15
1	0	1	1	0	R	N	I

The data in the I field is compared with byte 0 (N=0) or byte 1 (N=1) of the general register designated by the R field. This register must be an odd-numbered register. The contents of the general register are not changed.

The 'C' latch sets if the selected byte of R is less than I. The 'Z' latch sets if the selected byte of R equals I.

EXCLUSIVE-OR REGISTER IMMEDIATE (XRI)

0	1	2	3	4	5-6	7	8-15
1	1	0	0	0	R	N	I

The data in the I field is exclusive-ORed with byte 0 (N=0) or byte 1 (N=1) of the general register designated by the R field. The register must be an odd-numbered register. The results are stored in the selected byte of the general register.

The 'C' latch sets if the selected byte of R does not equal 0. The 'Z' latch sets if the selected byte of R equals 0.

LOAD REGISTER IMMEDIATE (LRI)

0	1	2	3	4	5-6	7	8-15
1	0	0	0	0	R	N	I

The data from the I field is loaded into byte 0 (N=0) or byte 1 (N=1) of the general register designated by the R field. This register must be an odd-numbered register. The non-selected byte of the register remains unchanged.

The 'C' latch sets if the selected byte of R is not equal to 0. The 'Z' latch sets if the selected byte of R equals 0.

OR REGISTER IMMEDIATE (ORI)

0	1	2	3	4	5-6	7	8-15
1	1	0	1	0	R	N	I

The data in the I field is ORed with byte 0 (N=0) or byte 1 (N=1) of the general register designated by R. The register specified by the R field must be an odd-numbered register. A bit position in the resulting byte is set to 1 if one or both of the corresponding bit positions in the general register and the I field are 1; otherwise, the bit is set to 0. The results are stored in the selected byte of R. The non-selected byte of R remains unchanged.

The 'C' latch sets if the selected byte of R does not equal 0. The 'Z' latch sets if the selected byte of R equals 0.

SUBTRACT REGISTER IMMEDIATE (SRI)

0	1	2	3	4	5-6	7	8-15
1	0	1	0	0	R	N	I

The data in the I field is subtracted from byte 0 (N=0) or from bytes 0 and 1 (N=1) of the general register designated by the R field. This register must be an odd-numbered register. The results are stored in the selected byte (s) of R.

Before the subtraction is done, the I field is expanded with high-order zeros to equal the size of the selected byte(s) of the general register.

The subtraction is done by adding the two's complement of the I field to the selected bytes of the general register. If the difference is less than zero, the result is in two's complement form.

The 'C' latch sets if N=0 and byte 0 of R is less than 0, or if N=1 and bytes 0 and 1 of R are less than 0. The 'Z' latch sets if N=0 and byte 0 of R equals 0, or if N=1 and bytes 0 and 1 of R equal 0.

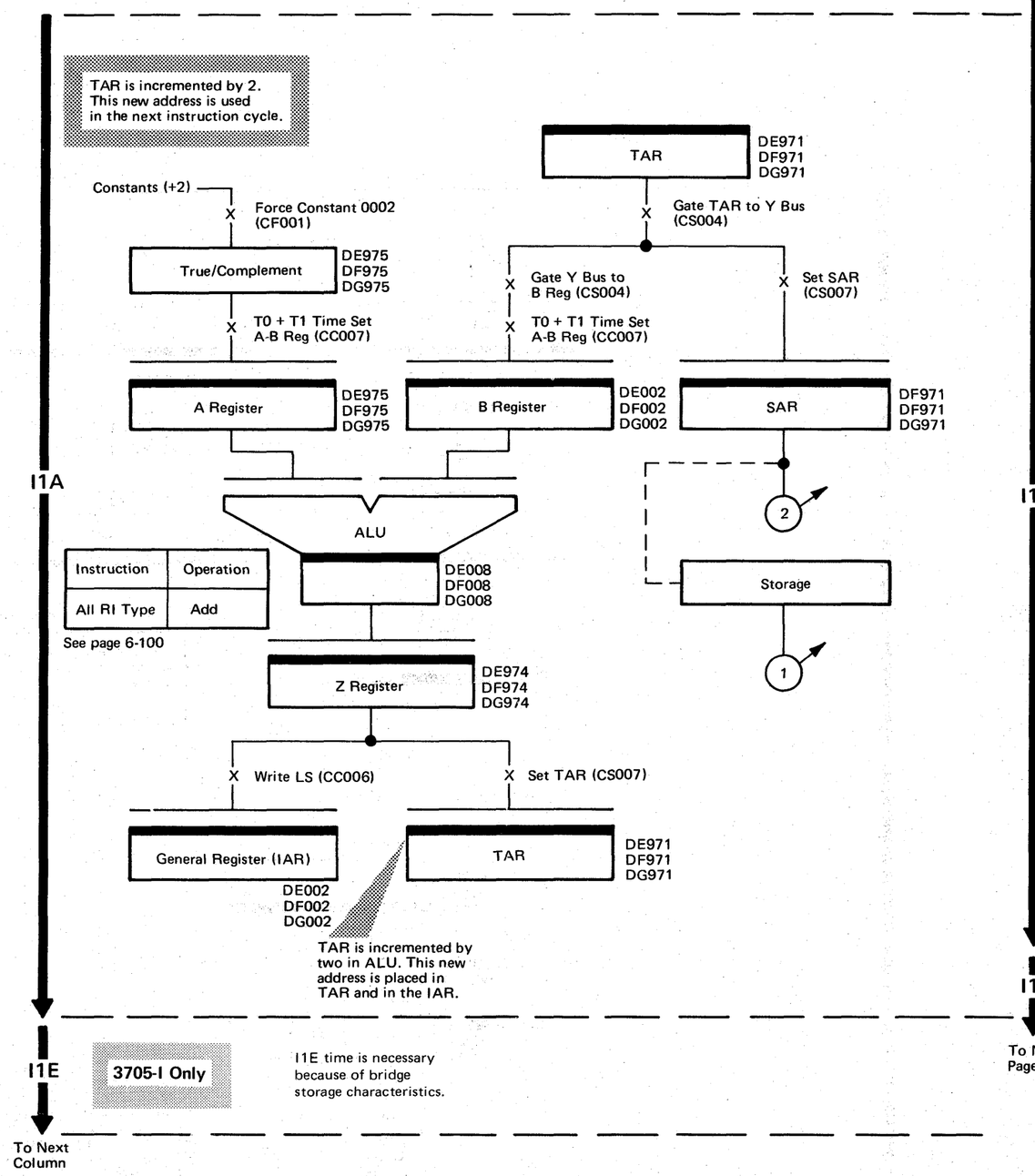
TEST REGISTER UNDER MASK (TRM)

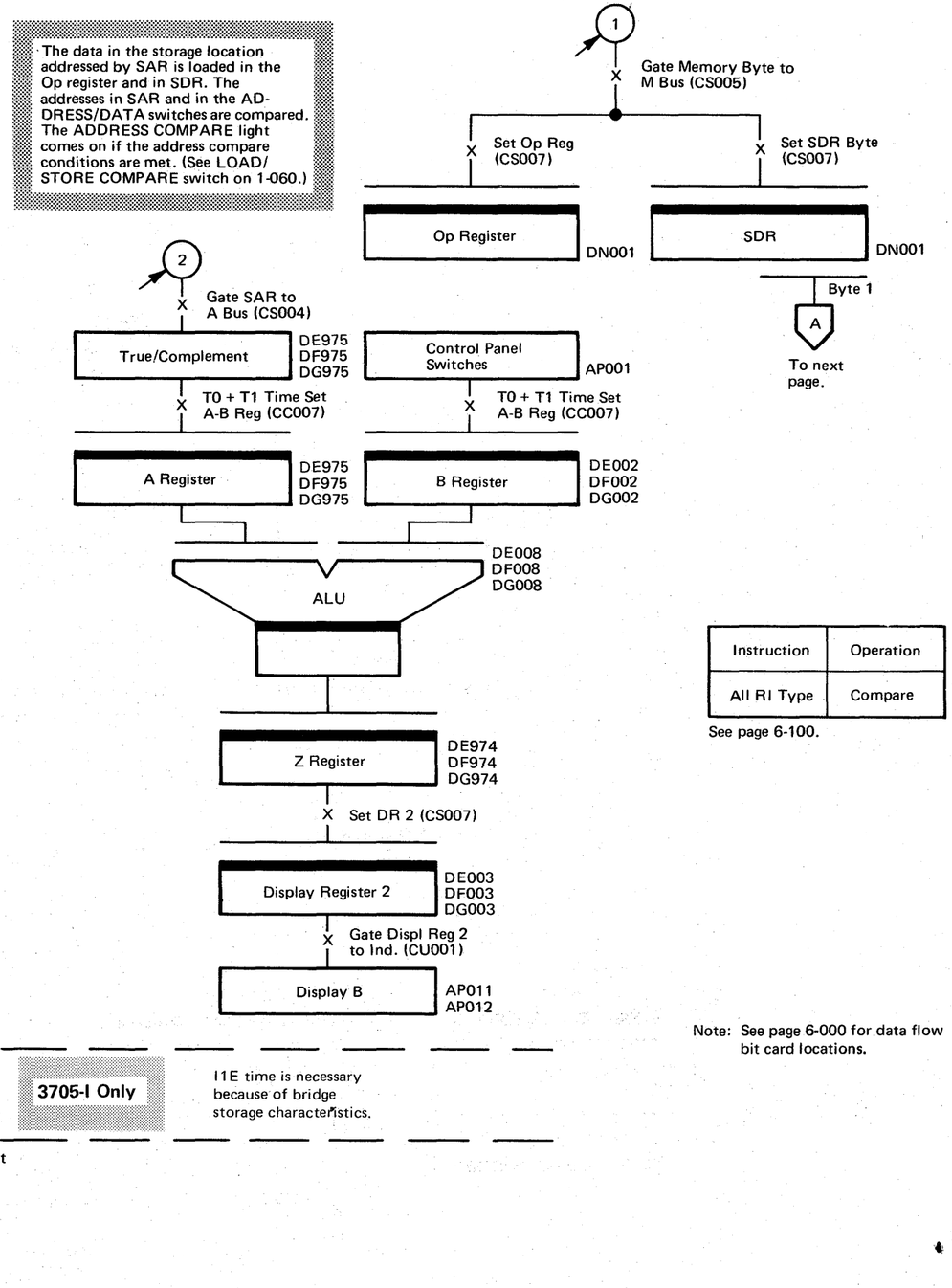
0	1	2	3	4	5-6	7	8-15
1	1	1	1	0	R	N	I

The data in the I field is tested against (ANDed with) byte 0 (N=0) or byte 1 (N=1) of the general register designated by the R field. This register must be an odd-numbered register. The contents of R are not changed.

The 'C' latch sets if the results do not equal 0. The 'Z' latch sets if the results equal 0.

RI INSTRUCTION OPERATION





Note: See page 6-000 for data flow bit card locations.

From Preceding Page

I1C

SDR byte 1 (I field of the instruction) is crossed to byte 0 by ALU and is loaded in byte 0 of SDR. Both bytes 0 and 1 of SDR then contain the I field.

From Preceding Page

A

Byte 1

True/Complement — DE975 DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

Byte 1

A Register — DE975 DF975 DG975

Byte 1

ALU — DE008 DF008 DG008

Byte 0

Instruction	Operation
All RI Type	Cross Lo to Hi

See page 6-100.

SAR — DE971 DF971 DG971

X Set LAR (CS001)

LAR — DE002 DF002 DG002

Z Register — DE974 DF974 DG974

Byte 0

X Gate Z Bus Byte 0 to M Bus (CS005)

X Set SDR Byte (CS007)

SDR — DN001

(1)

To Next Column

I1D

The specified bytes in SDR and the general register are gated to ALU, and the operation specified by the instruction is performed. The result is stored in the specified bytes of the general register.

(1)

X Gate SDR Bits to A Bus (CF003)

True/Complement — DE975 DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DE975 DF975 DG975

General Register (R) — DE002 DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DE002 DF002 DG002

Instruction	Operation
ARI	Add
NRI	And
CRI	Compare
XRI	Xor
LRI	A Reg Direct
ORI	Or
SRI	Subtract
TRM	And

See page 6-100.

ALU — DE008 DF008 DG008

C and Z Latches — CZ001

Z Register — DF974 DF974 DG975

X Write LS (CC006)

General Register (R) — DE002 DF002 DG002

TAR — DE971 DF971 DG971

X Gate TAR to Y Bus (CS004)

X Set SAR (CS007)

SAR — DE971 DF971 DG971

End of Instruction

Note: See page 6-000 for data flow bit card locations.

REGISTER TO REGISTER (RR) INSTRUCTIONS

The CCU takes one I1 cycle to execute any one of the 25 RR instructions except for the 'branch and link register' (BALR) instruction. The BALR instruction requires an I1 and an I2 cycle for execution.

For halfword, and 18 or 20-bit operations, the R1 and R2 fields in the instruction can specify any of the eight general registers in the active group. For byte operations, only an odd-numbered register can be specified, therefore the General Register = (2xR) +1.

ADD CHARACTER REGISTER (ACR)

0	1-2	3	4	5-6	7	8	9	10	11	12	13	14	15
0	R2	N2	0	R1	N1	0	0	0	1	1	0	0	0

Byte 0 (N2=0) or byte 1 (N2=1) of the general register designated by the R2 field is added to byte 0 (N1=0) or bytes 0 and 1 (N1=1) of the general register designated by the R1 field. The result is placed in the selected byte (s) of R1. The registers specified by R1 and R2 must be odd-numbered registers.

With Extended Addressing, byte X of the register specified by R1 is included in the operation. However, byte X does not affect the setting of the C and Z latches.

The 'C' latch sets if N1=0 and byte 0 of R1 overflows, or if N1=1 and bytes 0 and 1 overflow.

The 'Z' latch sets if N1=0 and byte 0 of R1 equals 0, or if N1=1 and bytes 0 and 1 of R1, equal 0.

ADD HALFWORD REGISTER (AHR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	0	0	1	0	0	0	0

Bytes 0 and 1 of the general register designated by R2 are added to bytes 0 and 1 of the general register designated by R1. The result is placed in bytes 0 and 1 of R1.

The 'C' latch sets if bytes 0 and 1 overflow. The 'Z' latch sets if bytes 0 and 1 equal 0.

Note: If general register 0 (IAR) is R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed.

ADD REGISTER (AR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	0	0	1	1	0	0	0

Bytes X, 0, and 1 of the general register designated by R2 are added to bytes X,0, and 1 of the general register designated by R1. The result is placed in R1.

Without Extended Addressing, the operation is the same as for the 'add halfword register' instruction.

The 'C' latch sets if bytes X, 0, and 1 of R1 overflow.

The 'Z' latch sets if bytes X, 0, and 1 of R1 equal 0.

Note: If general register 0 (IAR) is R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed.

AND CHARACTER REGISTER (NCR)

0	1-2	3	4	5-6	7	8	9	10	11	12	13	14	15
0	R2	N2	0	R1	N1	0	1	1	0	1	0	0	0

Byte 0 (N2=0) or byte 1 (N2=1) of the general register designated by R2 is ANDed with byte 0 (N1=0) or byte 1 (N1=1) of the general register designated by R1. The result is placed in the selected byte of R1. The registers specified by R1 and R2 must be odd-numbered registers.

The 'C' latch sets if the selected byte of R1 does not equal 0. The 'Z' latch sets if the selected byte of R1 equals 0.

AND HALFWORD REGISTER (NHR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	1	1	0	0	0	0	0

Bytes 0 and 1 of the general register designated by R2 are ANDed with bytes 0 and 1 of the general register designated by R1. The result is placed in bytes 0 and 1 of R1.

The 'C' latch sets if bytes 0 and 1 of R1 are not equal to 0.

The 'Z' latch sets if bytes 0 and 1 of R1 equal 0.

Note: If general register 0 (IAR) is specified as R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed.

AND REGISTER (NR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	1	1	0	1	0	0	0

Bytes X, 0, and 1 of the general register designated by R2 are ANDed with bytes X, 0, and 1 of the general register designated by R1. The result is placed in R1.

Without Extended Addressing, the operation is the same as for the 'and halfword register' instruction.

The 'C' latch sets if bytes X, 0, and 1 of R1 are not equal to 0.

The 'Z' latch sets if bytes X, 0, and 1 of R1 equal 0.

Note: If general register 0 (IAR) is specified as R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed.

BRANCH AND LINK REGISTER (BALR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	0	1	0	0	0	0	0	0

This two-cycle instruction causes an unconditional branch to the storage address in the general register designated by R2. After the 'branch to' address is obtained from R2, and before it is placed in register 0 (IAR), the contents of register 0 are moved to the register specified by R1 to provide for subroutine linkage.

Since register 0 is the IAR, no linkage is provided if it is specified as R1. For the same reason, no branch occurs if it is specified as R2.

The 'C' and 'Z' latches are not changed.

COMPARE CHARACTER REGISTER (CCR)

0	1-2	3	4	5-6	7	8	9	10	11	12	13	14	15
0	R2	N2	0	R1	N1	0	0	1	1	1	0	0	0

Byte 0 (N2=0) or byte 1 (N2=1) of the general register designated by R2 is compared with byte 0 (N1=0) or byte 1 (N1=1) of the general register designated by R1. The registers specified by R1 and R2 must be odd-numbered registers. The contents of the registers are not changed.

The 'C' latch sets if the selected byte of R1 is less than the selected byte of R2.

The 'Z' latch sets if the selected byte of R1 equals the selected byte of R2.

COMPARE HALFWORD REGISTER (CHR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	0	1	1	0	0	0	0

Bytes 0 and 1 of the general register designated by R2 are compared with bytes 0 and 1 of the general register designated by R1. The contents of the registers are not changed.

The 'C' latch sets if bytes 0 and 1 of R1 are less than bytes 0 and 1 of R2.

The 'Z' latch sets if bytes 0 and 1 of R1 are equal to bytes 0 and 1 of R2.

COMPARE REGISTER (CR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	0	1	1	1	0	0	0

Bytes X, 0, and 1 of R2 are compared with X, 0, and 1 of R1. The contents of the registers are not changed.

Without Extended Addressing, the operation is the same as 'compare halfword register'.

The 'C' latch sets if bytes X, 0, and 1 of R1 are less than bytes X, 0, and 1 of R2.

The 'Z' latch sets if bytes X, 0, and 1 are equal to bytes X, 0, and 1 of R2.

EXCLUSIVE-OR CHARACTER REGISTER (XCR)

0	1-2	3	4	5-6	7	8	9	10	11	12	13	14	15
0	R2	N2	0	R1	N1	0	1	0	0	1	0	0	0

Byte 0 (N2=0) or byte 1 (N2=1) of the general register designated by R2 is exclusive-ORed with byte 0 (N1=0) or byte 1 (N1=1) of the general register designated by R1. The registers specified by R1 and R2 must be odd-numbered registers. The result is placed in the selected byte of R1.

The 'C' latch sets if the selected byte of R1 does not equal 0.

The 'Z' latch sets if the selected byte of R1 equals 0.

EXCLUSIVE-OR HALFWORD REGISTER (XHR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	1	0	0	0	0	0	0

Bytes 0 and 1 of the general register designated by R2 are exclusive-ORed with bytes 0 and 1 of the general register designated by R1. The result is placed in bytes 0 and 1 of R1.

The 'C' latch sets if bytes 0 and 1 of R1 are not equal to 0.

The 'Z' latch sets if bytes 0 and 1 of R1 equal 0.

Note: If general register 0 (IAR) is R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed.

EXCLUSIVE-OR REGISTER (XR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	1	0	0	1	0	0	0

Bytes X, 0, and 1 of the general register designated by R2 are exclusive-ORed with bytes X, 0, and 1 of the general register designated by R1. The result is placed in R1.

Without Extended Addressing, the operation is the same as 'exclusive-or halfword register'.

The 'C' latch sets if bytes X, 0, and 1 of R1 do not equal 0.

The 'Z' latch sets if bytes X, 0, and 1 of R1 equal 0.

Note: If general register 0 (IAR) is R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed.

LOAD CHARACTER REGISTER (LCR)

0	1-2	3	4	5-6	7	8	9	10	11	12	13	14	15
0	R2	N2	0	R1	N1	0	0	0	0	1	0	0	0

Byte 0 (N2=0) or byte 1 (N2=1) of the general register designated by R2 is moved to byte 0 (N1=0) or byte 1 (N1=1) of the general register designated by R1. The registers specified by R1 and R2 must be odd-numbered registers.

The 'C' latch sets if the selected byte of R1 has an even number of data bits set to 1.

The 'Z' latch sets if the selected byte of R1 equals 0.

LOAD CHARACTER WITH OFFSET REGISTER (LCOR)

0	1-2	3	4	5-6	7	8	9	10	11	12	13	14	15
0	R2	N-2	0	R-1	N1	0	1	1	1	1	0	0	0

Byte 0 (N2=0) or byte 1 (N2=1) of the register specified by the R2 field is shifted right one bit position and a 0 is inserted in the high-order bit position. The bit shifted out of position 7 is lost. The resulting byte is placed in the selected byte of R1. The non-selected byte of R1 remains unchanged. The registers specified by R1 and R2 must be odd-numbered registers.

The 'C' latch sets if the bit shifted out of bit position 7 of the selected byte of R2 is 1.

The 'Z' latch sets if the selected byte of R1 equals 0.

LOAD HALFWORD REGISTER (LHR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	0	0	0	0	0	0	0

Bytes 0 and 1 of the general register designated by R2 are loaded into bytes 0 and 1 of the general register designated by R1.

The 'C' latch sets if bytes 0 and 1 of R1 do not equal 0.

The 'Z' latch sets if bytes 0 and 1 of R1 equal 0.

Note: If general register 0 (IAR) is R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed.

LOAD HALFWORD WITH OFFSET REGISTER (LHOR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	1	1	1	0	0	0	0

Bytes 0 and 1 of the general register designated by R2 are shifted right one bit position. A 0 is inserted in the high-order bit position. The resulting halfword is placed in byte 0 and 1 of R1.

The 'C' latch sets if the bit shifted out of bit 1.7 is 1.

The 'Z' latch sets if bytes 0 and 1 of R1 equal 0.

Note: If general register 0 (IAR) is R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed.

LOAD REGISTER (LR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	0	0	0	1	0	0	0

Bytes X, 0, and 1 of the general register designated by R2 are loaded into bytes X, 0, and 1 of R1.

Without Extended Addressing, the operation is the same as 'load halfword register'.

The 'C' latch sets if bytes X, 0, and 1 of R1 do not equal 0.

The 'Z' latch sets if bytes X, 0, and 1 of R1 equal 0.

Note: If general register 0 (IAR) is R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed.

LOAD WITH OFFSET REGISTER (LOR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	1	1	1	1	0	0	0

Bytes X, 0, and 1 of the general register designated by R2 are shifted right one bit position. A 0 is inserted in the high-order bit position. The result is placed in bytes X, 0, and 1 of R1.

Without Extended Addressing, the operation is the same as 'load halfword with offset register.'

The 'C' latch sets if the bit shifted out of bit 1.7 is 1.

The 'Z' latch sets if bytes X, 0, and 1 of R1 equal 0.

Note: If general register 0 (IAR) is R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches do not change.

OR CHARACTER REGISTER (OCR)

0	1-2	3	4	5-6	7	8	9	10	11	12	13	14	15
0	R2	N2	0	R1	N1	0	1	0	1	1	0	0	0

Byte 0 (N2=0) or byte 1 (N2=1) of the general register designated by R2 is ORed with byte 0 (N1=0) or byte 1 (N1=1) of the general register designated by R1. The registers specified by R1 and R2 must be odd-numbered registers. The result is placed in the selected byte of R1. The non-selected byte of R1 remains unchanged.

The 'C' latch sets if the selected byte of R does not equal 0.

The 'Z' latch sets if the selected byte of R1 equals 0.

OR HALFWORD REGISTER (OHR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	1	0	1	0	0	0	0

Bytes 0 and 1 of the general register designated by R2 are ORed with bytes 0 and 1 of the general register designated by R1. The result is placed in bytes 0 and 1 of R1.

The 'C' latch sets if bytes 0 and 1 of R1 do not equal 0.

The 'Z' latch sets if bytes 0 and 1 of R1 equal 0.

Note: If general register 0 (IAR) is R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed.

OR REGISTER (OR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	1	0	1	1	0	0	0

Bytes X, 0, and 1 of the general register designated by R2 are ORed with bytes X, 0, and 1 of the general register designated by R1. The result is placed in bytes X, 0, and 1 of R1.

Without Extended Addressing, the operation is the same as 'or halfword register.'

The 'C' latch sets if bytes X, 0, and 1 of R1 do not equal 0.

The 'Z' latch sets if bytes X, 0, and 1 of R1 equal 0.

Note: If general register 0 (IAR) is R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed.

SUBTRACT CHARACTER REGISTER (SCR)

0	1-2	3	4	5-6	7	8	9	10	11	12	13	14	15
0	R2	N2	0	R1	N1	0	0	1	0	1	0	0	0

Byte 0 (N2=0) or byte 1 (N2=1) of the general register designated by R2 is subtracted from byte 0 (N1=0) or bytes 0 and 1 (N1=1) of the general register designated by R1. Before the subtraction is performed, the selected byte of R2 is expanded with high-order zeros to equal the size of the selected byte(s) of R1. The subtraction is performed by adding the two's complement of the selected byte(s) of R2 to the selected byte(s) of R1. The result is stored in the selected byte(s) of R1. If the difference is less than zero, the result is in two's complement form.

The 'C' latch sets if N=0 and the selected byte(s) of R1 are less than 0.

The 'Z' latch sets if N=1 and the selected bytes(s) of R1 equal 0.

SUBTRACT HALFWORD REGISTER (SHR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	0	1	0	0	0	0	0

Bytes 0 and 1 of the general register designated by R2 are subtracted from bytes 0 and 1 of the general register designated by R1. The subtraction is performed by adding the two's complement of bytes 0 and 1 of R2 to bytes 0 and 1 of R1. The result is placed in bytes 0 and 1 of R1. If the difference is less than zero, the result is in two's complement form.

The 'C' latch sets if bytes 0 and 1 of R1 are less than 0.

The 'Z' latch sets if bytes 0 and 1 of R1 equal 0.

Note: If general register 0 (IAR) is R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed.

SUBTRACT REGISTER (SR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R-2	0	R1	1	0	1	0	1	0	0	0

Bytes X, 0, and 1 of the general register designated by R2 are subtracted from bytes X, 0, and 1 of the general register designated by R1. The subtraction is performed by adding the two's complement of bytes X, 0, and 1 of R2 to bytes X, 0, and 1 of R2. The result is placed in R1. If the difference is less than zero, the result is in two's complement form.

Without Extended Addressing, the operation is the same as 'subtract halfword register'.

The 'C' latch sets if bytes X, 0, and 1 of R1 are less than 0.

The 'Z' latch sets if bytes X, 0, and 1 of R1 equal 0.

Note: If general register 0 (IAR) is R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed.

RR INSTRUCTION OPERATION, EXCEPT BALR

TAR is incremented by 2. This new address is used in the next instruction cycle.

TAR — DE971 DF971 DG971

Constants (+2) → X Force Constant 0002 (CF001) → True/Complement — DE975 DF975 DG975 → X T0 + T1 Time Set A-B Reg (CC007) → A Register — DE975 DF975 DG975

TAR → X Gate TAR to Y Bus (CS004)

X Gate Y Bus to B Reg (CS004) → X T0 + T1 Time Set A-B Reg (CC007) → B Register — DE002 DF002 DG002

X Set SAR (CS007) → SAR — DE971 DF971 DG971

A Register, B Register → ALU — DE008 DF008 DG008 → Z Register — DE974 DF974 DG974

Z Register → X Write LS (CC006) → General Register (IAR) — DE002 DF002 DG002

Z Register → X Set TAR (CS007) → TAR — DE971 DF971 DG971

TAR is incremented by two in ALU. This new address is placed in TAR and in the IAR.

SAR → (2) → Storage → (1)

Instruction	Operation
All RR type, except BALR	Add

See page 6-100

I1A

I1E — 3705-I Only

I1E time is necessary because of bridge storage characteristics.

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The data in the storage location addressed by SAR is loaded in the Op register and in SDR. The addresses in SAR and in the ADDRESS/DATA switches are compared. The ADDRESS COMPARE light comes on if the address compare conditions are met. (See LOAD/STORE COMPARE switch on 1-060.)

(1) → X Gate Memory Byte to M Bus (CS005)

X Set Op Reg (CS007) → Op Register — DN001

X Set SDR Byte (CS007) → SDR — DN001

(2) → X Gate SAR to A Bus (CS004)

True/Complement — DE975 DF975 DG975 → X T0 + T1 Time Set A-B Reg (CC007) → A Register — DE975 DF975 DG975

Control Panel Switches — AP001 → X T0 + T1 Time Set A-B Reg (CC007) → B Register — DE002 DF002 DG002

A Register, B Register → ALU — DE008 DF008 DG008 → Z Register — DE974 DF974 DG974

Z Register → X Set DR 2 (CS007) → Display Register 2 — DE003 DF003 DG003 → X Gate Displ Reg 2 to Ind. (CU001) → Display B — AP011 AP012

Instruction	Operation
All RR type, except BALR	Compare

See page 6-100.

Note: See page 6-000 for data flow bit card locations.

I1B

I1F — 3705-I Only

I1F time is necessary because of bridge storage characteristics.

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From Preceding Page

Applies to all RR instructions except BALR.

The contents of the general register addressed by the R2 field are loaded into SDR. For cross operations, the bytes are crossed by circuitry between ALU and the Z register.

I1C

Instruction	Operation
ACR	Cross
AHR	B Reg Direct
AR	B Reg Direct
NCR	Cross
NHR	B Reg Direct
NR	B Reg Direct
CCR	Cross
CHR	B Reg Direct
CR	B Reg Direct
XCR	Cross
XHR	B Reg Direct
XR	B Reg Direct
LCR	Cross
LCOR	B Reg Direct
LHR	B Reg Direct
LHOR	B Reg Direct
LOR	B Reg Direct
LR	B Reg Direct
OCR	Cross
OHR	B Reg Direct
OR	B Reg Direct
SCR	Cross
SHR	B Reg Direct
SR	B Reg Direct

See page 6-100.

General Register (R2) — DE002, DF002, DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DE002, DF002, DG002

ALU — DE008, DF008, DG008

Z Register — DE974, DF974, DG974

X Gate Z Bus to M Bus (CS005)

X Set SDR Byte (CS007)

SDR

DN001

(1)

SAR — DE971, DF971, DG971

X Set LAR (CS001)

LAR — DE002, DF002, DG002

To Next Column

The specified bytes in SDR and general register R1 are gated to ALU. The ALU performs the operation specified by the instruction in the Op register and stores the results in the specified bytes of general register R1.

I1D

Instruction	Operation
ACR	Add
AHR	Add
AR	Add
NCR	And
NHR	And
NR	And
CCR	Compare
CHR	Compare
CR	Compare
XCR	Xor
XHR	Xor
XR	Xor
LCR	A Reg Direct
LCOR	Shift Right
LHR	A Reg Direct
LHOR	Shift Right
LOR	Shift Right
LR	A Reg Direct
OCR	Or
OHR	Or
OR	Or
SCR	Subtract
SHR	Subtract
SR	Subtract

See page 6-100

(1)

X Gate SDR Bits to A Bus (CF003)

True/Complement — DE975, DF975, DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DE975, DF975, DG975

General Register (R1) — DE002, DF002, DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DE002, DF002, DG002

ALU — DE008, DF008, DG008

C and Z Latches — CZ001

Z Register — DE974, DF974, DG975

X Set TAR (CS007)

X Write LS (CC006)

TAR — DE971, DF971, DG971

General Register (R1) — DE002, DF002, DG002

X Gate TAR to Y Bus (CS004)

X Set SAR (CS007)

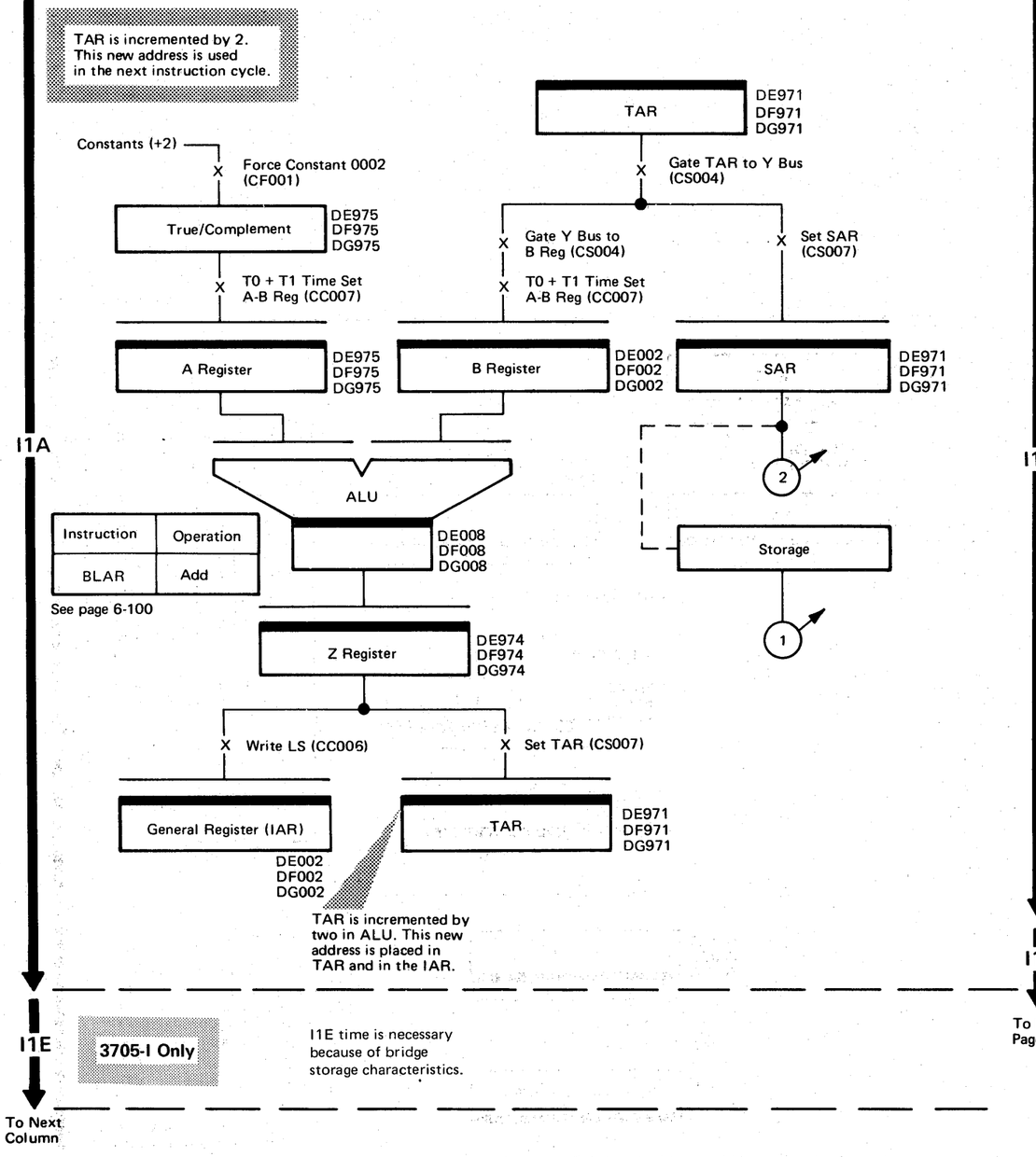
SAR — DE971, DF971, DG971

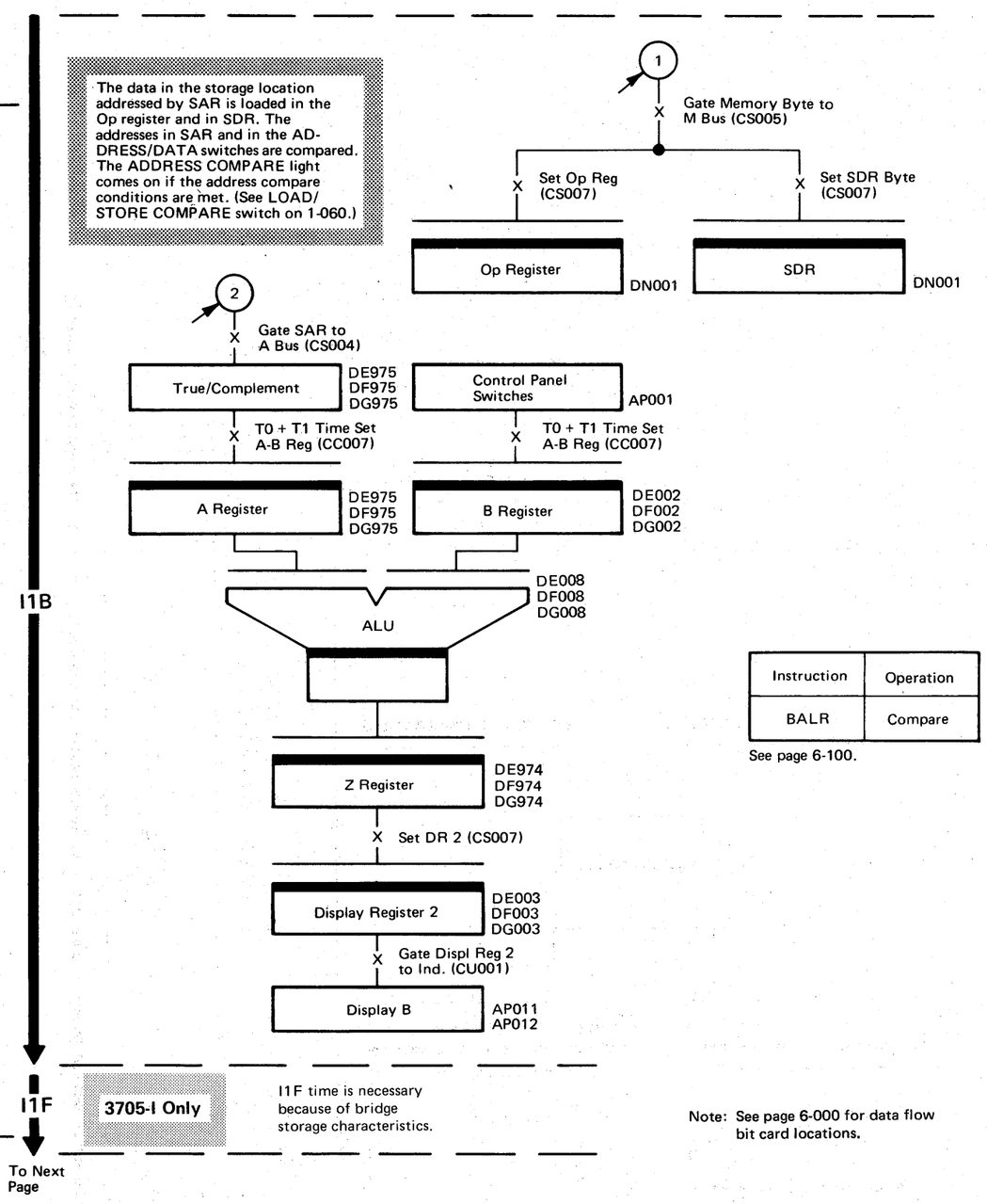
If R1 is general register 0 (IAR), the result is also placed in TAR. A branch to the address formed in register 0 occurs.

End of Instruction

Note: See page 6-000 for data flow bit card locations.

BALR INSTRUCTION OPERATION





Note: See page 6-000 for data flow bit card locations.

From Preceding Page

BALR Only

I1C

The address in SAR is gated to LAR.

SAR — DE971 DF971 DG971

X Set LAR (CS001)

LAR — DE002 DF002 DG002

BALR Only

I1D

The address in TAR is gated to SAR.

TAR — DE971 DF971 DG971

X Gate TAR to Y Bus (CS004)

X Set SAR (CS007)

SAR — DE971 DF971 DG971

BALR Only

I2A

The contents of general register R2 are placed in bytes X, 0, and 1 of SDR.

General Register (R2) — DE002 DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DE002 DF002 DG002

ALU

DE008 DF008 DG008

Instruction	Operation
BALR	B Reg Direct

See page 6-100.

Z Register — DE974 DF974 DG974

X Gate Z Bus to M Bus (CS005)

X Set SDR Byte (CS007)

SDR — DN001

I2E 3705-I Only

I2E time is necessary because of bridge storage characteristics.

To Next Column

BALR Only

I2B

The addresses in SAR and in the ADDRESS/DATA switches are compared, and the ADDRESS COMPARE light comes on if the address compare conditions are met. (See "LOAD/STORE ADDRESS COMPARE Switch" on page 1-060.)

SAR — DE971 DF971 DG971

X Gate SAR to A Bus (CS004)

True/Complement — DE975 DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

Control Panel Switches — AP001

X T0 + T1 Time Set A-B Reg (CC007)

X Gate Y Bus to B Reg (CS004)

A Register — DE975 DF975 DG975

B Register — DE002 DF002 DG002

ALU

DE008 DF008 DG008

Instruction	Operation
BALR	Compare

See page 6-100.

Z Register — DE974 DF974 DG974

X Set DR 2 (CS007)

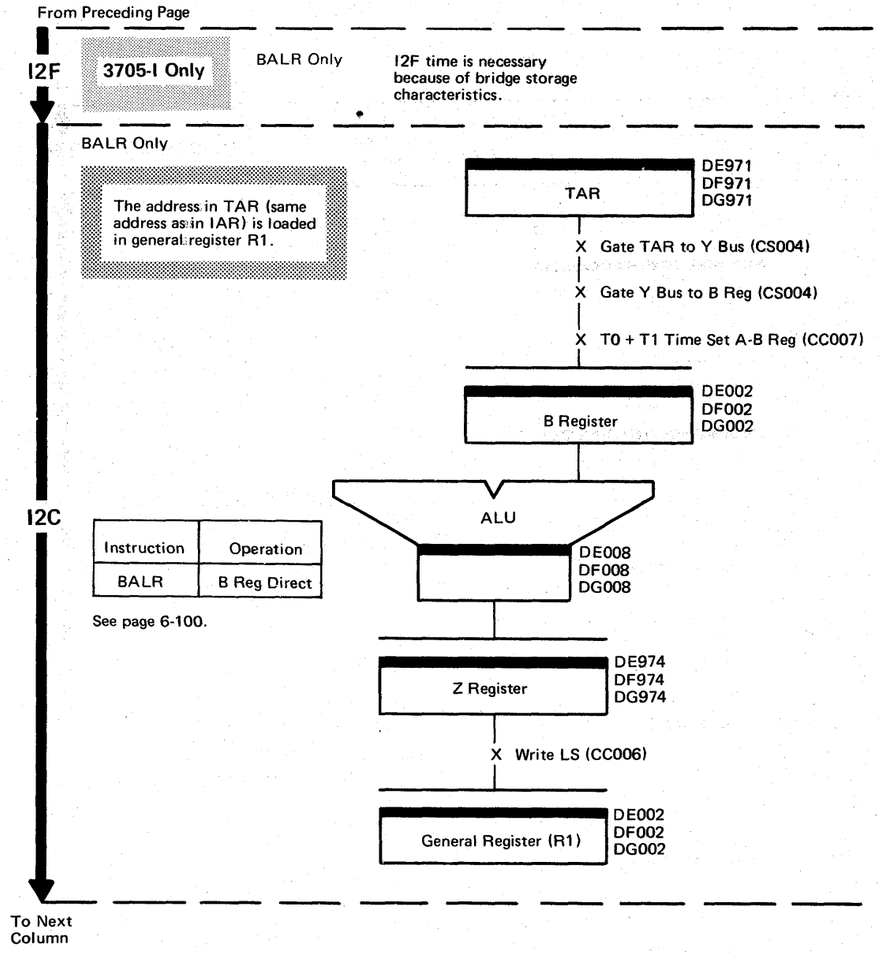
Display Register 2 — DE003 DF003 DG003

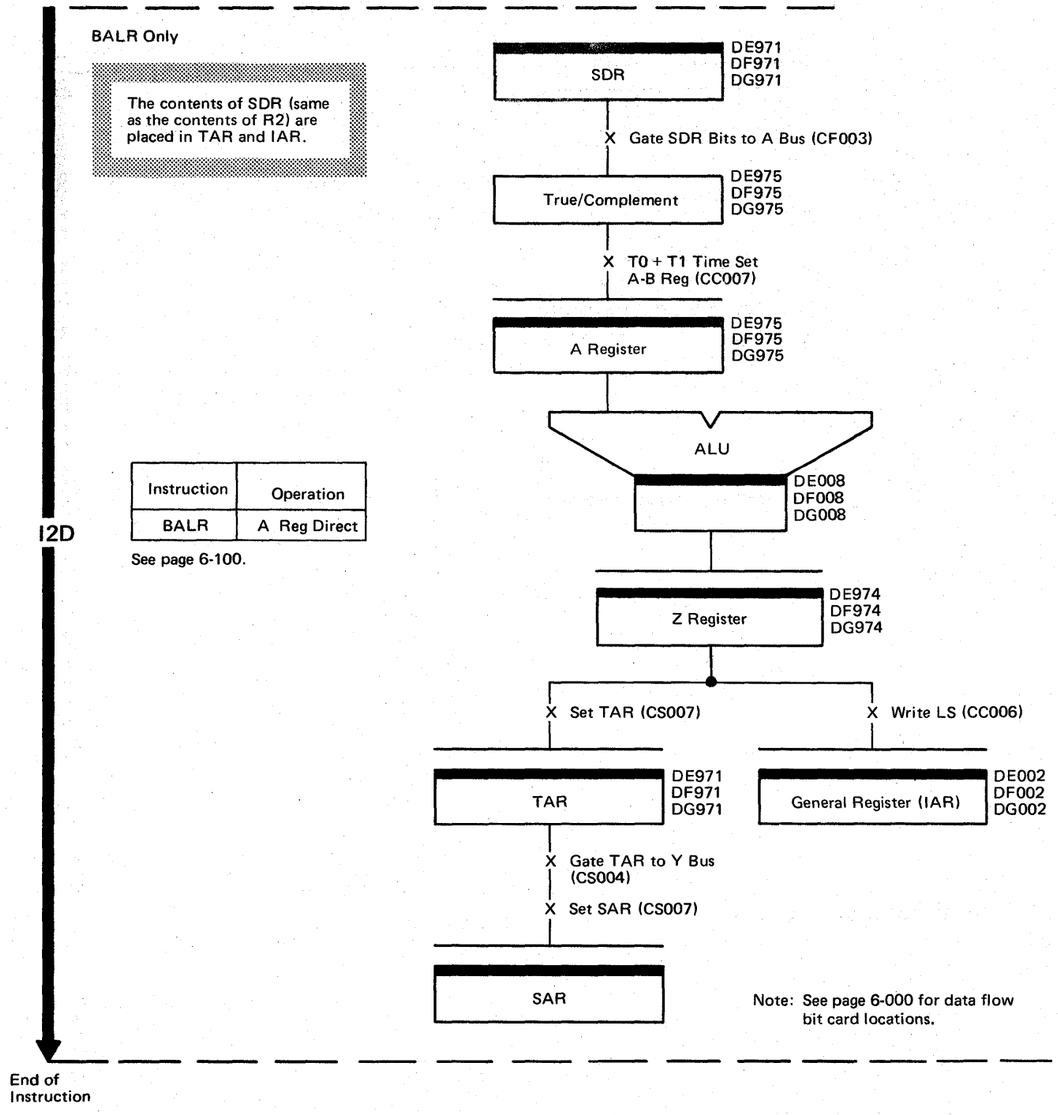
X Gate Displ Reg 2 to Ind. (CU001)

Display B — AP011 AP012

Note: See page 6-000 for data flow bit card locations.

To Next Page


From Preceding Page
I2F
3705-I Only
BALR Only
I2F time is necessary because of bridge storage characteristics.
BALR Only
The address in TAR (same address as in IAR) is loaded in general register R1.
TAR
DE971
DF971
DG971
X Gate TAR to Y Bus (CS004)
X Gate Y Bus to B Reg (CS004)
X T0 + T1 Time Set A-B Reg (CC007)
B Register
DE002
DF002
DG002
I2C
ALU
DE008
DF008
DG008
Instruction
Operation
BALR
B Reg Direct
See page 6-100.
Z Register
DE974
DF974
DG974
X Write LS (CC006)
General Register (R1)
DE002
DF002
DG002
To Next Column

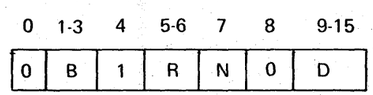

BALR Only
The contents of SDR (same as the contents of R2) are placed in TAR and IAR.
I2D
Instruction
Operation
BALR
A Reg Direct
See page 6-100.
SDR
DE971
DF971
DG971
X Gate SDR Bits to A Bus (CF003)
True/Complement
DE975
DF975
DG975
X T0 + T1 Time Set A-B Reg (CC007)
A Register
DE975
DF975
DG975
ALU
DE008
DF008
DG008
Z Register
DE974
DF974
DG974
X Set TAR (CS007)
X Write LS (CC006)
TAR
DE971
DF971
DG971
General Register (IAR)
DE002
DF002
DG002
X Gate TAR to Y Bus (CS004)
X Set SAR (CS007)
SAR
Note: See page 6-000 for data flow bit card locations.
End of Instruction

REGISTER AND STORAGE (RS) INSTRUCTIONS

The CCU takes an I1 and an I2 machine cycle to execute the 'insert character', 'load halfword', 'store character', or 'store halfword' instruction. The 'load' and 'store instructions each require an I1, I2, and I3 cycle.

For the 'insert character' and 'store character' instructions, the general register designated by the R field in the instruction must be odd-numbered, therefore the General Register = (2xR) +1.

INSERT CHARACTER (IC)



The 16-bit (18 or 20-bit with extended addressing) base address in the general register specified by the B field is added to the displacement specified in the D field. The displacement can be 0 to +127 bytes. The addition forms an effective address that is used to address storage.

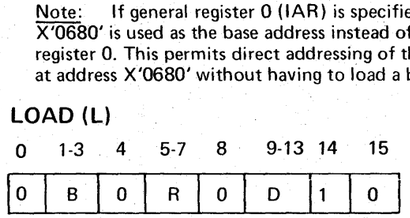
The byte at the effective storage address is loaded into byte 0 (N=0) or byte 1 (N=1) of the general register designated by the R field. The remaining bits of the register are unchanged. R must be an odd register.

The 'C' latch sets if the selected byte of R has an even number of 1 bits.

The 'Z' latch sets if the selected byte of R equals 0.

Note: If general register 0 (IAR) is specified by B, a constant of X'0680' is used as the base address instead of the contents of register 0. This permits direct addressing of the 128 bytes starting at address X'0680' without having to load a base register.

LOAD (L)



The 16-bit (18 or 20-bit with extended addressing) base address in the general register specified by the B field is added to the displacement in the D field. The displacement can be 0 to +31 fullwords. The addition forms an effective address that is used to address storage.

The low-order 16-bits (18 or 20-bits with extended addressing) of the fullword at the effective storage address are loaded into the general register specified by the R field. (The high-order 12, 14, or 16 bits in the storage address are ignored.) The low-order bit of the effective address is ignored since storage is addressed on halfword boundaries.

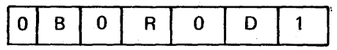
The 'C' latch sets if bytes X, 0, and 1 of R do not equal 0.

The 'Z' latch sets if bytes X, 0, and 1 of R equal 0.

In a 3705 without Extended Addressing, a 'load' instruction is decoded and executed as a 'load halfword' instruction except that X '0780' is used as the base address if IAR is specified by B.

Note: If general register 0 (IAR) is specified by R, an unconditional branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed. If general register 0 is specified by B, X'0780' is used as the base address instead of the contents of register 0. This permits direct addressing of the 32 fullwords starting at address X'0780' without having to load a base register.

LOAD HALFWORD (LH)



The 16-bit (18 or 20-bit with extended addressing) base address in the general register specified by the B field is added to the displacement specified by the D field. The displacement can be 0 to +63 halfwords. This addition forms an effective address that is used to address storage.

The halfword at the effective storage address is loaded into bytes 0 and 1 of the register specified by the R field. The low-order bit of the effective address is ignored since storage is addressed on halfword boundaries.

With Extended Addressing, byte X of the register specified by R is set to zero during the load operation.

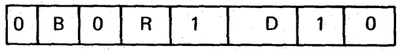
The 'C' latch sets if bytes 0 and 1 of R do not equal 0.

The 'Z' latch sets if bytes 0 and 1 of R equal 0.

The Load Halfword instruction is also used in conjunction with the Input X'7B' instruction to generate the new BSC-CRC character. When this instruction is executed at program level 2, 3, 4, or 5, or level 1 during IPL phase 3, the halfword accessed is loaded into both the specified general register and the BSC-CRC register. For non-CRC operation, the loading of data into the BSC-CRC register serves no purpose.

Note: If general register 0 (IAR) is specified by the R field, an unconditional branch to the address formed in register 0 occurs. The condition codes are not changed. If general register 0 is specified by B, X'0700' is used as the base address instead of the contents of general register 0. This permits direct addressing of the 64 halfwords starting at address X'0700' without having to load a base register.

STORE (ST)



The 16-bit (18 or 20-bit with extended addressing) base address in the general register specified by the B field is added to the displacement specified by the D field. The displacement can be 0 to +31 fullwords. The addition forms the effective address used to address storage.

Bytes X, 0, and 1 of the general register specified by the R field are stored in the low-order 16 bits (18 or 20 bits with extended addressing) of the fullword located at the effective address. The high-order 14 bits (12 or 10 bits with extended addressing) are not affected. The low-order bit of the effective address is ignored since storage is addressed on halfword boundaries.

Without Extended Addressing, bytes 0 and 1 of the register are stored into the low-order 16 bits of the fullword in storage, and the high-order 16 bits remain unchanged.

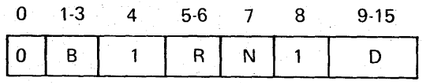
The 'C' and 'Z' latches are not changed.

In a 3705 without Extended Addressing, a 'store' instruction is decoded and executed as a 'store halfword' instruction except that X '0780' is used as the base address if IAR is specified by B.

Note: If general register 0 (IAR) is specified by B, X'0780' is used as the base address instead of the contents of register 0. This permits direct addressing of the 32 fullwords starting at address X'0780' without having to load a base register.

Special Case: A 'store' instruction must be located at storage location X'0010'. The R field and B field of this instruction both equal 0. This is the first instruction executed when a program level 1 interrupt occurs. During I1A time of the store instruction, the gate 'Write LS' is blocked in order to perserve the IAR of program level 2. During I3D time of the instruction, the storage location X'0012' is forced onto the Indata Bus to address the next storage instruction.

STORE CHARACTER (STC)



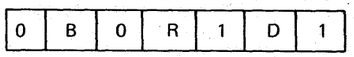
The 16-bit (18 or 20-bit with extended addressing) base address in the general register specified by the B field is added to the displacement specified by the D field. The displacement can be 0 to +127 bytes. The addition forms an effective address that is used to address storage.

Byte 0 (N=0) or byte 1 (N=1) of the general register specified by the R field is stored at the effective storage address. R must be an odd register.

The 'C' and 'Z' latches are not changed.

Note: If general register 0 (IAR) is specified by B, X'0680' is used as the base address instead of the contents of register 0. This permits direct addressing of the 128 bytes starting at address X'0680' without having to load a base register.

STORE HALFWORD (STH)



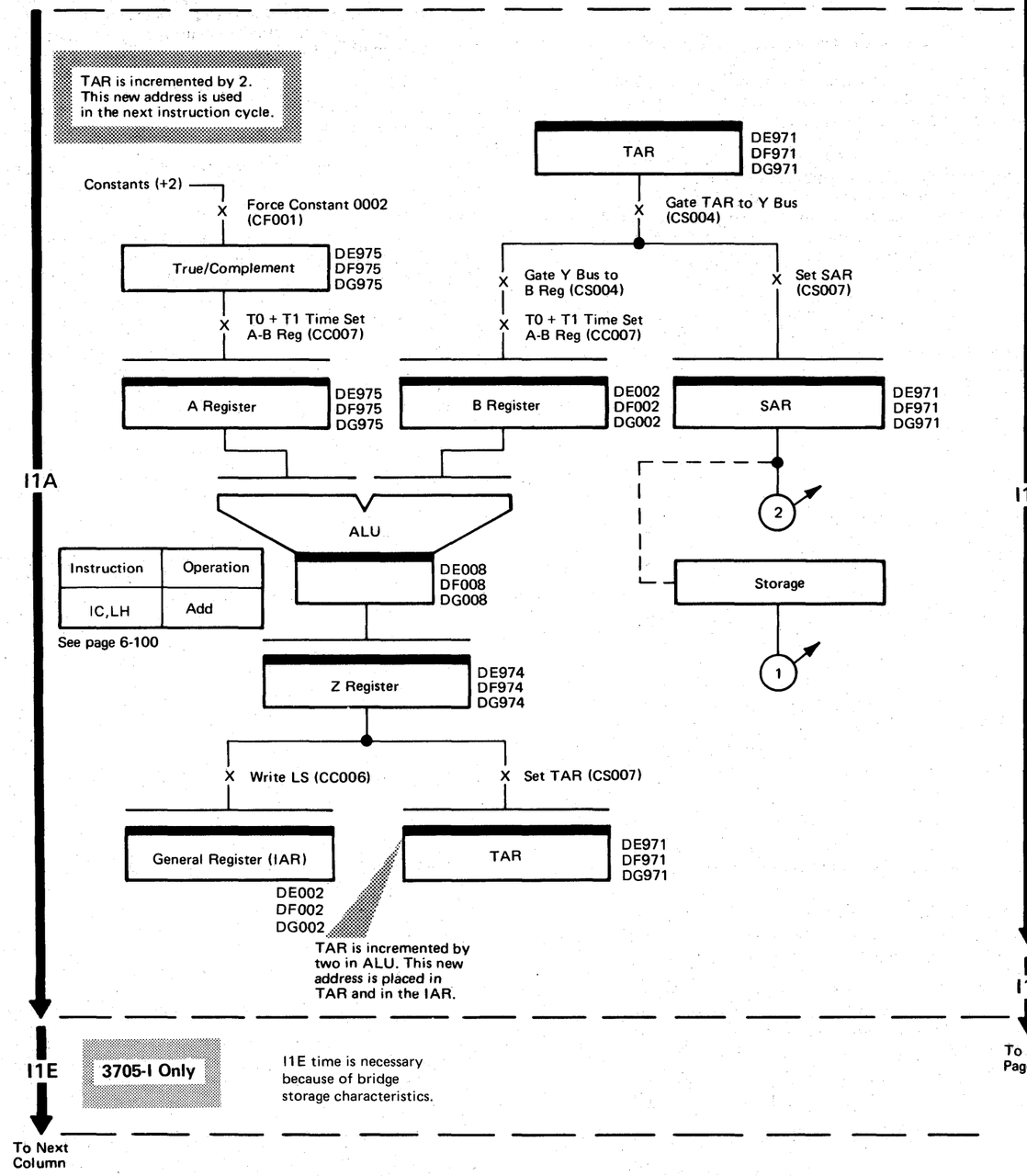
The 16-bit (18 or 20-bit with extended addressing) base address in the general register designated by the B field is added to the displacement specified by the D field. The displacement can be 0 to +63 halfwords. The addition forms an effective address that is used to address storage.

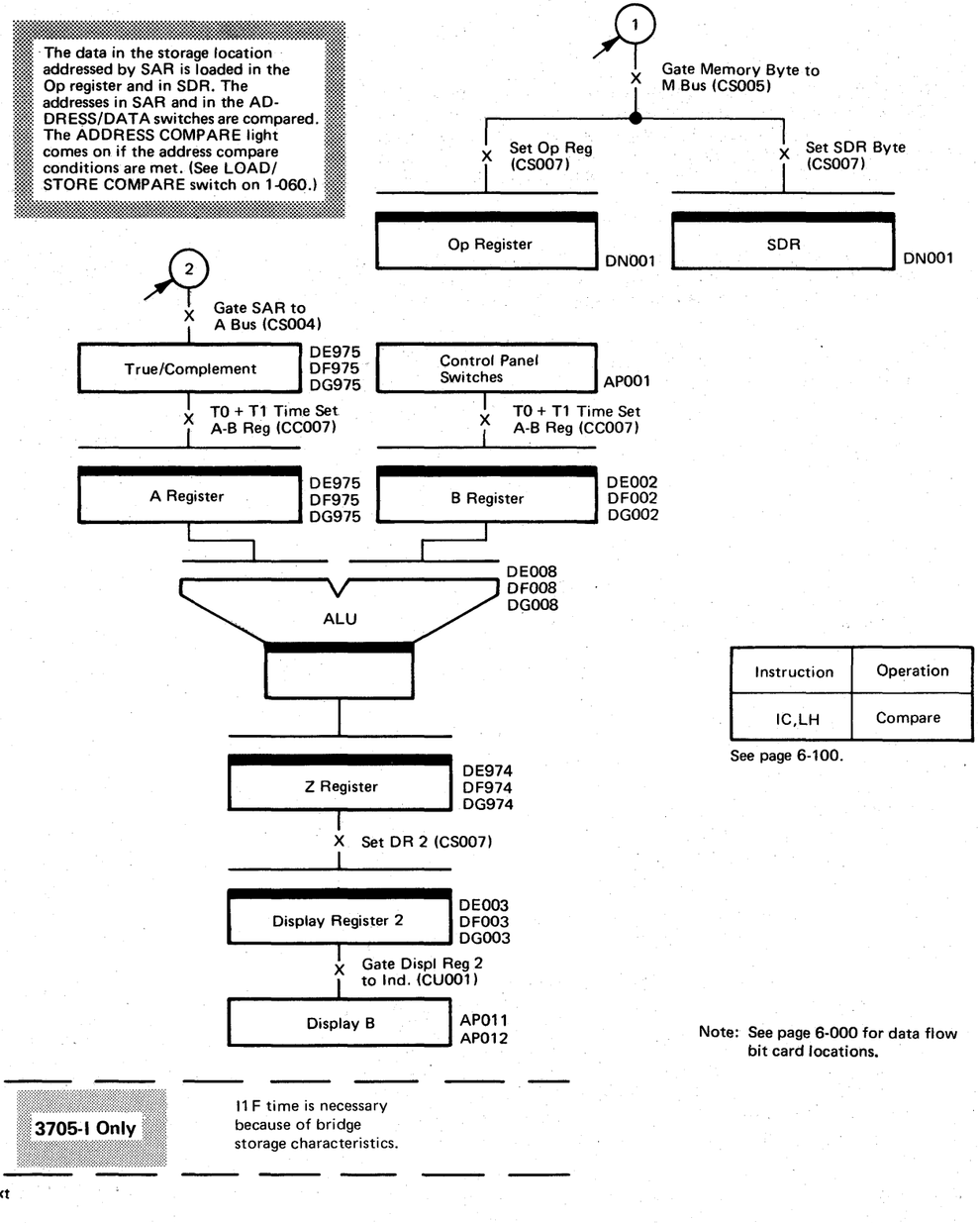
Byte 0 and 1 of the general register designated by the R field are stored at the effective address. The low-order bit of the effective address is ignored since storage is addressed on halfword boundaries.

The 'C' and 'Z' latches are not changed.

Note: If general register 0 (IAR) is specified by B, X'0700' is used as the base address instead of the contents of register 0. This permits direct addressing of the 64 halfwords starting at address X'0700' without having to load a base register. If the R field is zero, X'0000' is stored at the storage address instead of the contents of register 0.

IC AND LH INSTRUCTION OPERATION





Note: See page 6-000 for data flow bit card locations.

From Preceding Page

IC and LH Only

I1C

The address in SAR is gated to LAR.

SAR — DE971 DF971 DG971

X Set LAR (CS001)

LAR — DE002 DF002 DG002

IC and LH Only

SDR — DN001

X Gate SDR Bits to A Bus (CF003)

The D field (now in SDR) is added to general register B by the ALU. The result is gated to TAR and is used as the next storage address. If general register 0 (IAR) is B, a constant is used as the base address. (See the description of the specific instruction.)

True/Complement — DE975 DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DE975 DF975 DG975

General Register (B) — DE002 DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DE002 DF002 DG002

ALU

DE008 DF008 DG008

I1D

Instruction	Operation
IC	Add
LH	Add

See page 6-100.

Z Register — DE974 DF974 DG974

X Set TAR (CS007)

TAR — DE971 DF971 DG971

X Gate TAR to Y Bus (CS004)

X Set SAR (CS007)

SAR — DE971 DF971 DG971

1

To Next Column

IC and LH Only

I2A

For an IC instruction, the byte of general register R that is not specified by N is loaded into the SDR. This byte is duplicated in the other byte of SDR.

For an LH instruction, the contents of general register R are loaded into SDR. (See the description of the specific instruction.)

1

Storage

A

To next page.

General Register (R) — DE002 DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DE002 DF002 DG002

ALU

DE008 DF008 DG008

Instruction	Operation
IC	Cross
LH	B Reg Direct

See page 6-100.

Z Register — DE974 DF974 DG974

X Gate Z Bus to M Bus (CS005)

X Set SDR Byte (CS007)

SDR — DN001

I2E

3705-I Only

I2E time is necessary because of bridge storage characteristics.

To Next Page

Note: See page 6-000 for data flow bit card locations.

CCU

From Preceding Page

IC and LH Only

The data in the storage location addressed by SAR is loaded into SDR. The addresses in SAR and in the ADDRESS/DATA switches are compared, and the ADDRESS COMPARE light comes on if the address compare conditions are met. (See LOAD/STORE ADDRESS COMPARE switch on 1-060.)

From preceding page

A

X Gate Mem Byte to M Bus (CS005)

X Set SDR Byte (CS007)

SDR — DN001

1

I2B

SAR — DE971 DF971 DG971

X Gate SAR to A Bus (CS004)

True/Complement — DE975 DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DE975 DF975 DG975

Control Panel Switches — AP001

X T0 + T1 Time Set A-B Reg (CC007)

X Gate Y Bus to B Reg (CS004)

B Register — DE002 DF002 DG002

ALU

DE008 DF008 DG008

Instruction	Operation
IC	Compare
LH	Compare

See page 6-100.

Z Register — DE974 DF974 DG974

X Set DR 2 (CS007)

Display Register 2 — DE003 DF003 DG003

X Gate Displ Reg 2 to Ind (CU001)

Display B — AP011 AP012

Note: If SAR bit 1.7 is on, set SDR byte 1 (Condition Set SDR Byte 1, CS002). If SAR bit 1.7 is off, set SDR byte 0 (Condition Set SDR Byte 0, CS002).

To Next Column

I2F

3705-I Only

I2F time is necessary because of bridge storage characteristics.

IC and LH Only

The data in SDR is loaded in the selected byte(s) of general register R.

For an IC instruction, ALU does a cross operation if the byte from storage (in SDR) is not the same byte (0 or 1) as the selected byte of general register R.

1

X Gate SDR Bits to A Bus (CF003)

True/Complement — DE975 DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DE975 DF975 DG975

ALU

DE008 DF008 DG008

I2C

Instruction	Operation
IC	A Reg Direct or Cross A Reg Direct
LH	

See page 6-100.

C and Z Latches — CZ001

Z Register — DE974 DF974 DG974

X Write LS (CC006)

General Register (R) — DE002 DF002 DG002

To Next Page

Note: See page 6-000 for data flow bit card locations.

From Preceding Page

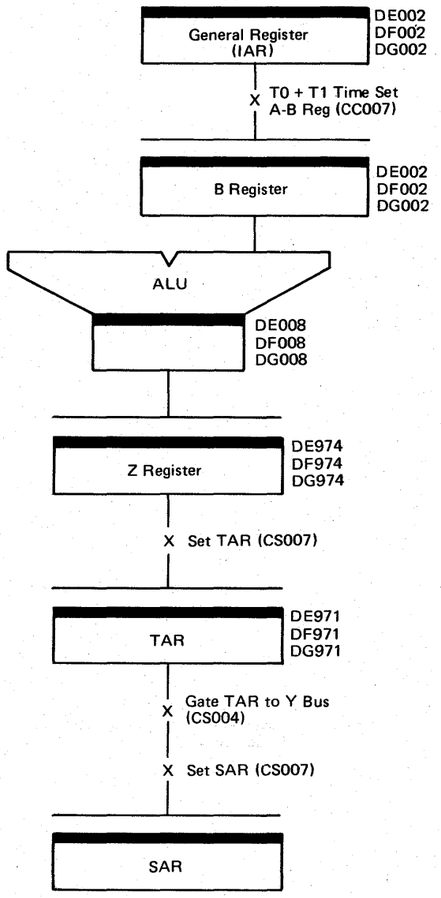
IC and LH Only

The address of the next instruction is loaded into TAR from IAR.

Instruction	Operation
IC	B Reg Direct
LH	B Reg Direct

See page 6-100.

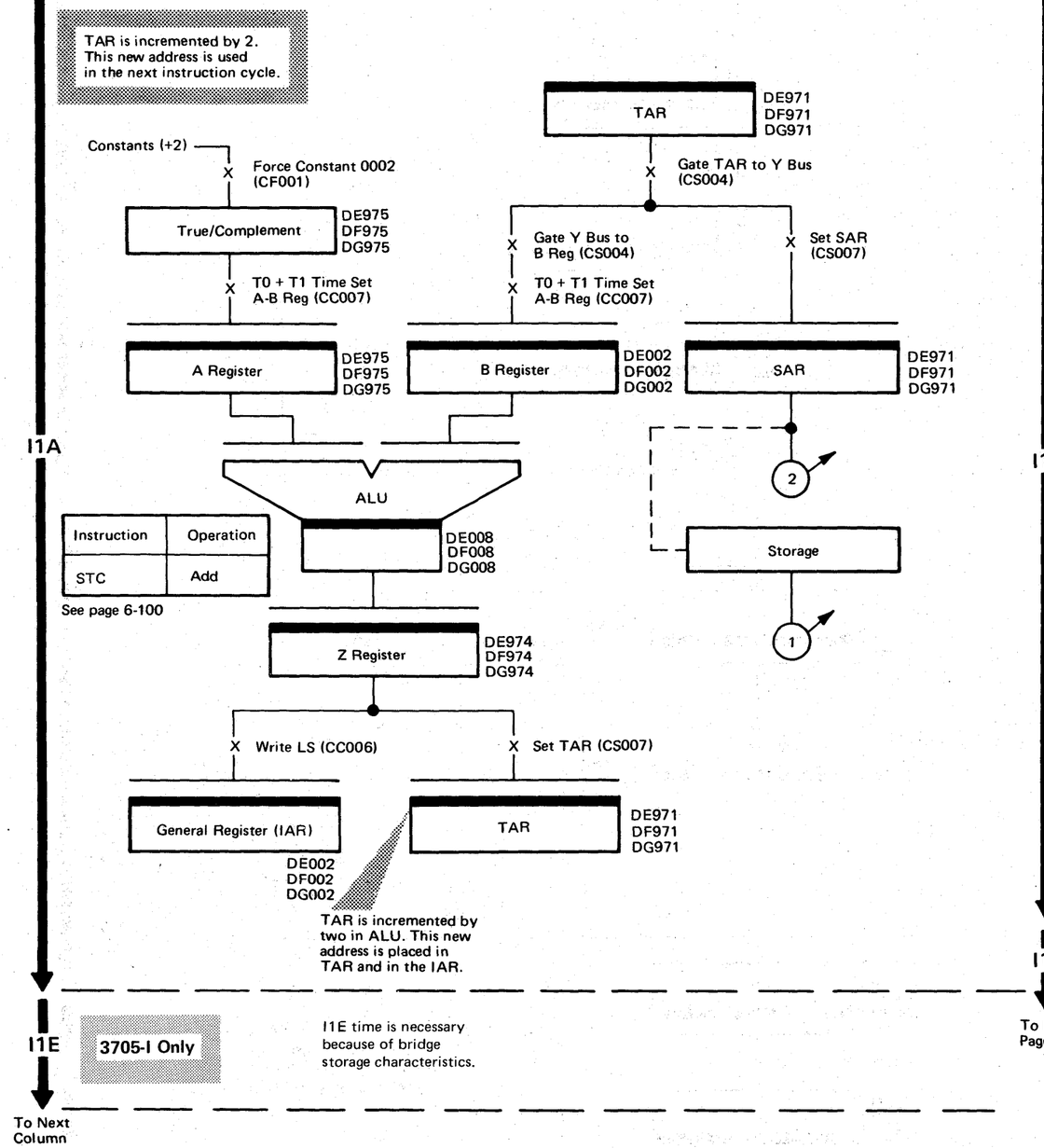
I2D

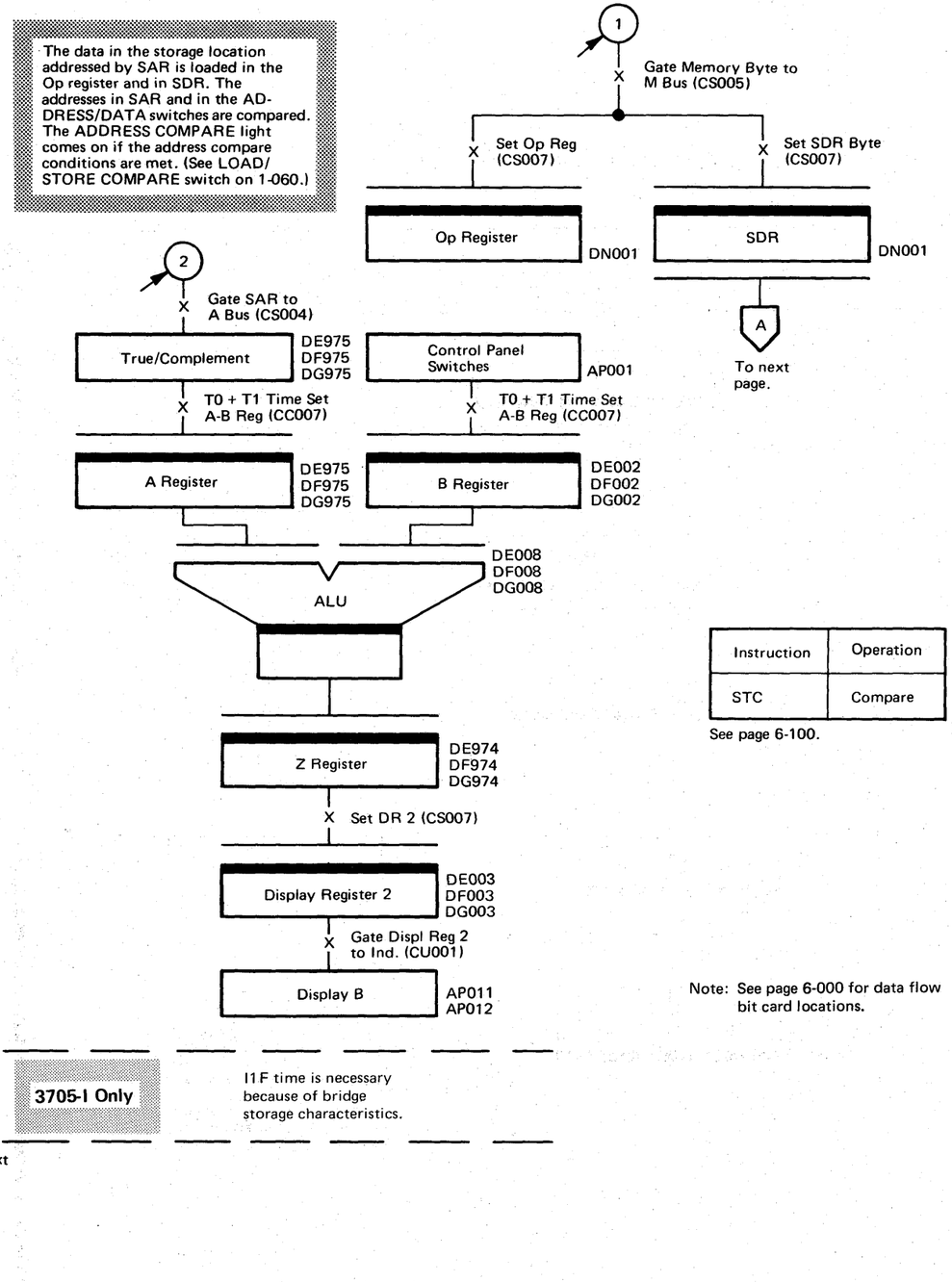


End of Instruction

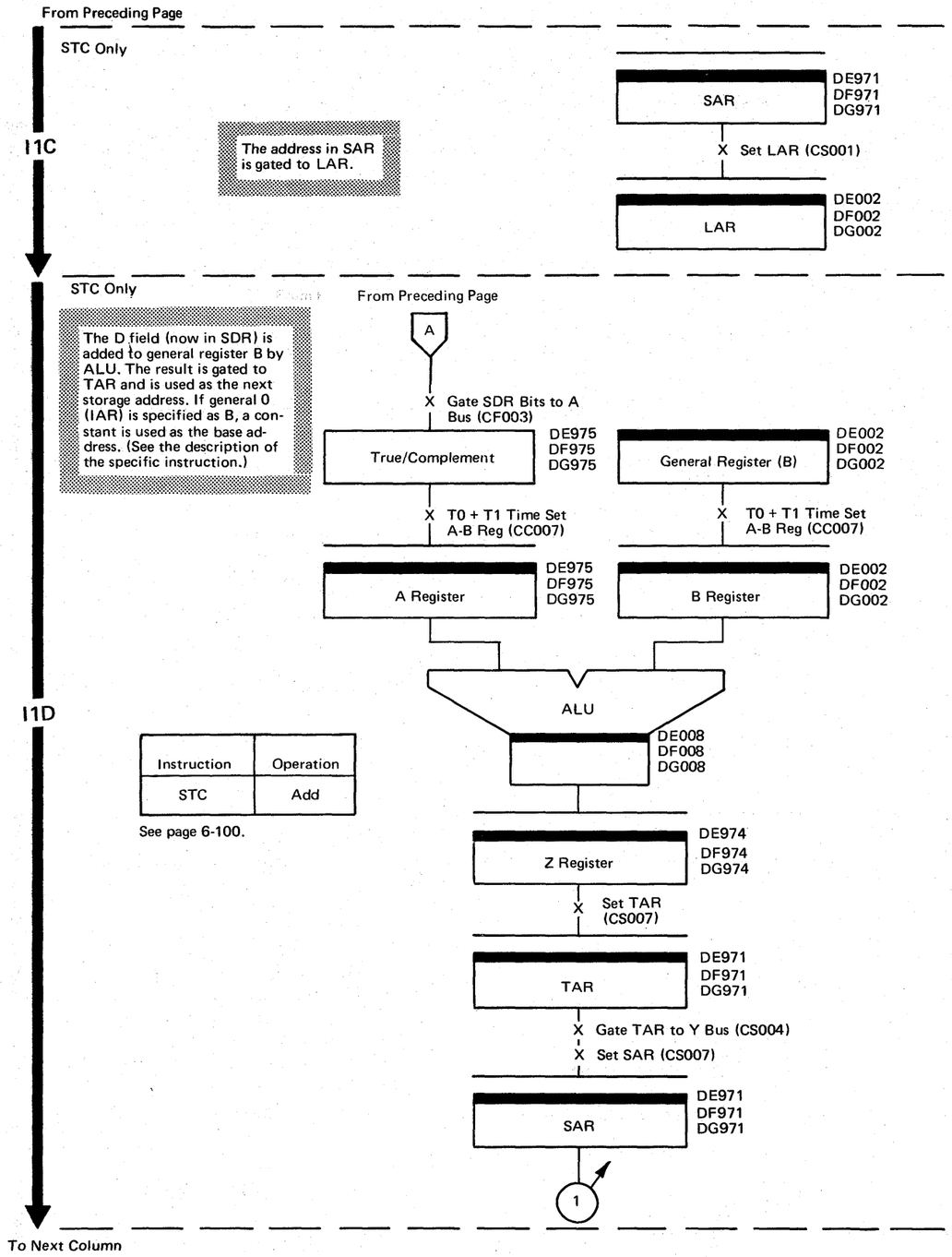
Note: See page 6-000 for data flow bit card locations.

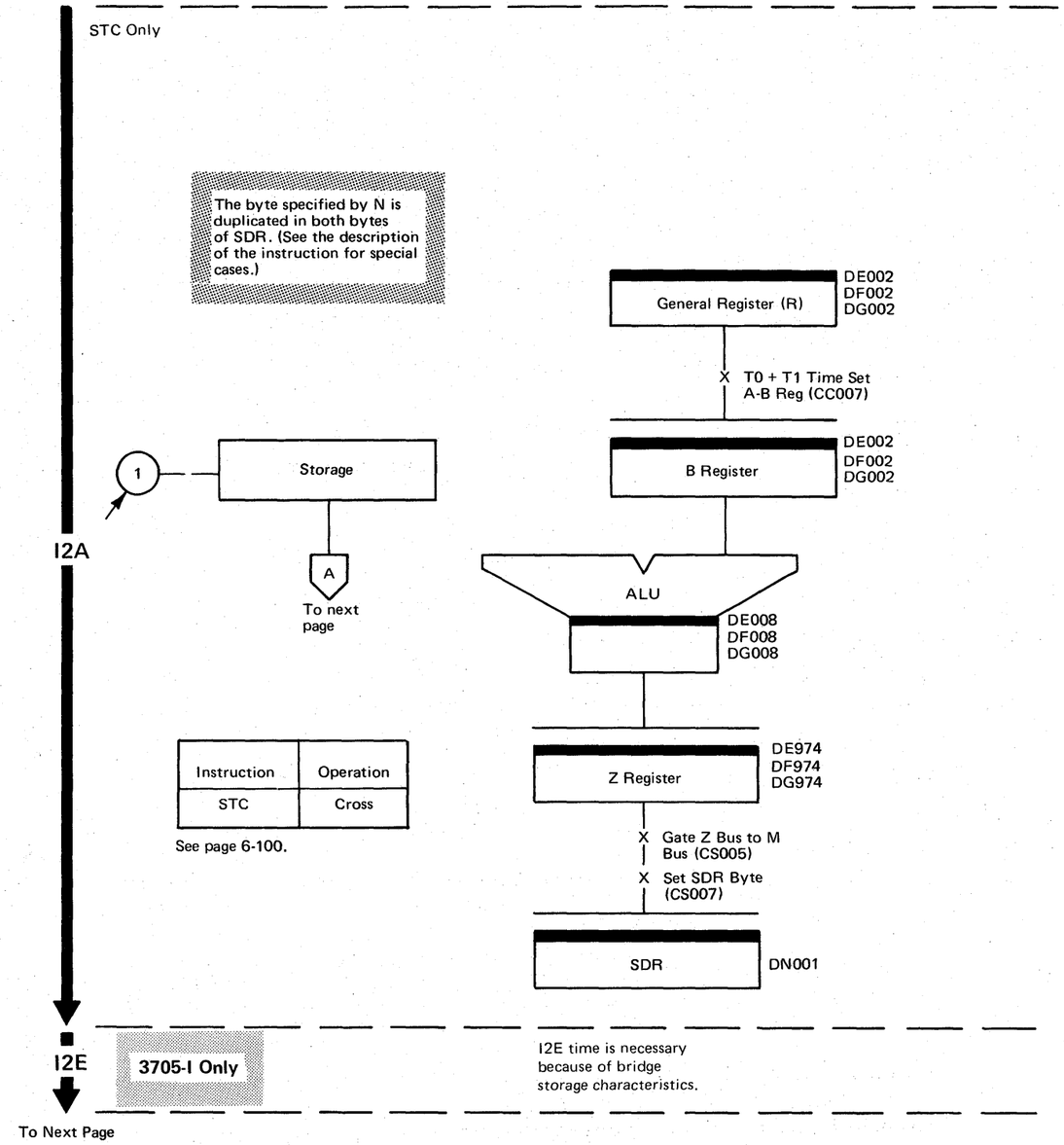
STC INSTRUCTION OPERATION





Note: See page 6-000 for data flow bit card locations.





Note: See page 6-000 for data flow bit card locations.

From Preceding Page

STC Only

The byte of the storage location that is not specified by the B field is placed in the same byte of SDR. Bytes 0 and 1 of SDR are then stored at the storage address. The addresses in SAR and in the ADDRESS/DATA switches are compared, and the ADDRESS COMPARE light comes on if the address compare conditions are met. (See LOAD/STORE ADDRESS COMPARE switch on page 1-060.)

I2B

From Preceding Page

A

X Gate Mem Byte to M Bus (CS005)

X Set SDR Byte (CS007)

SDR — DN001

Storage — 1

1

X Gate SAR to A Bus (CS004)

SAR — DE971, DF971, DG971

True/Complement — DE975, DF975, DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DE975, DF975, DG975

Control Panel Switches — AP001

X T0 + T1 Time Set A-B Reg (CC007)

X Gate Y Bus to B Reg (CS004)

B Register — DE002, DF002, DG002

ALU — DE008, DF008, DG008

Instruction	Operation
STC	B Reg Direct

See page 6-100.

Z Register — DE974, DF974, DG974

X Set DR2 (CS007)

Display Register 2 — DE003, DF003, DG003

X Gate Displ Reg 2 to Ind (CU001)

Display B — AP011, AP012

To Next Column

I2F

3705-I Only

I2F time is necessary because of bridge storage characteristics.

I2C

No Action

STC Only

The address of the next instruction is loaded into TAR from IAR.

I2D

Instruction	Operation
STH	B Reg Direct

See page 6-100.

General Register (IAR) — DE002, DF002, DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DE002, DF002, DG002

ALU — DE008, DF008, DG008

Z Register — DE974, DF974, DG974

TAR — DE971, DF971, DG971

X Gate TAR to Y Bus (CS004)

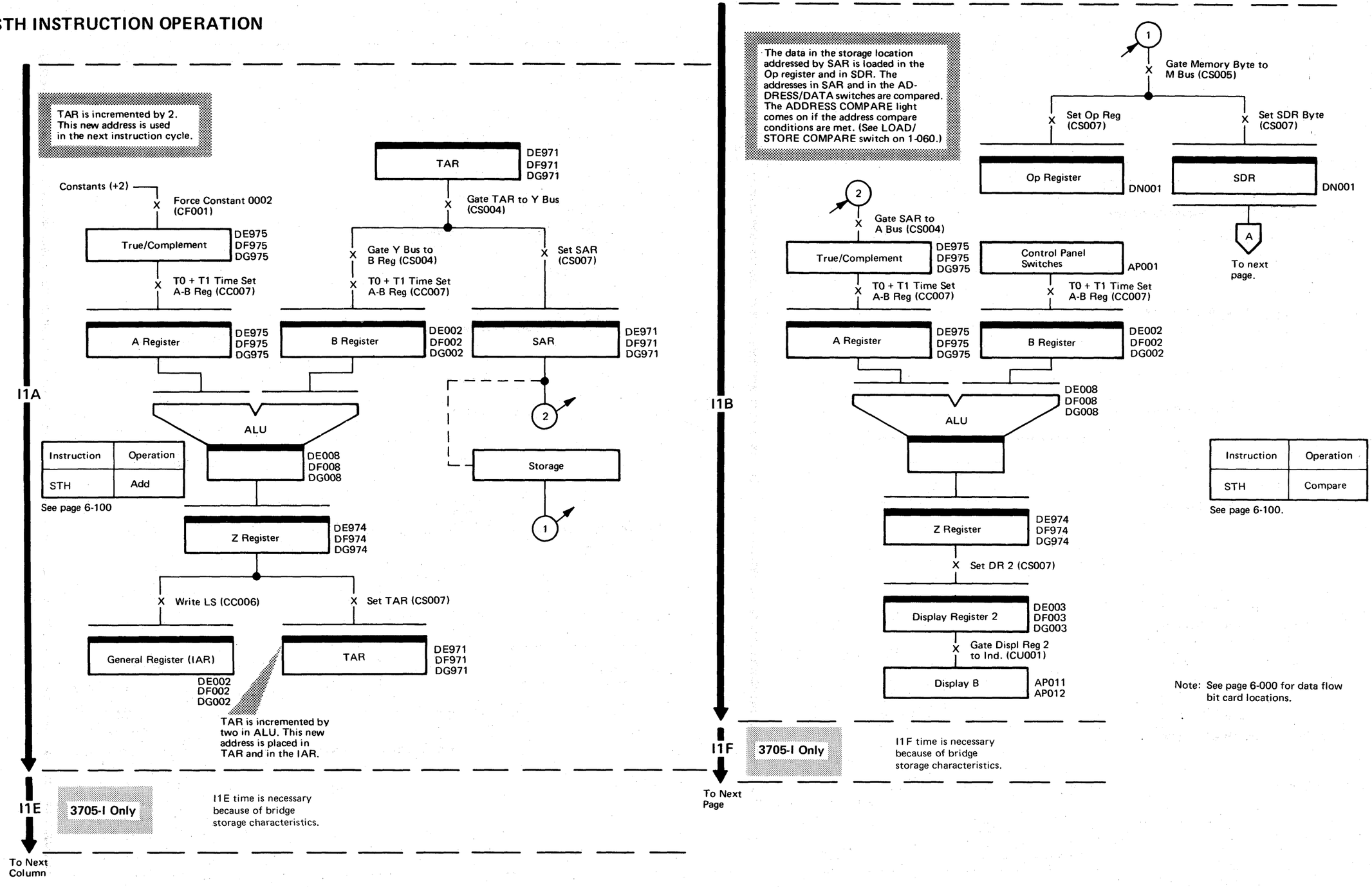
X Set SAR (CS007)

SAR — DE971, DF971, DG971

End of Instruction

Note: See page 6-000 for data flow bit card locations.

STH INSTRUCTION OPERATION



From Preceding Page

STH Only

I1C

No Action

STH Only

The D field (now in SDR) is added to general register B by ALU. The result is gated to TAR and is used as the next storage address. If general register 0 (IAR) is B, a constant is used as the base address. (See the description of the instruction.)

From Preceding Page

A

X Gate SDR Bits to A Bus (CF003)

True/Complement — DE975 DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DE975 DF975 DG975

General Register (B) — DE002 DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DE002 DF002 DG002

ALU

DE008 DF008 DG008

Z Register — DE974 DF974 DG974

X Set TAR (CS007)

TAR — DE971 DF971 DG971

X Gate TAR to Y Bus (CS004)

SAR — DE971 DF971 DG971

1

Instruction	Operation
STH	Add

See page 6-100.

I1D

To Next Column

STH Only

I2A

The data in byte 0 and 1 of the R field is gated to the SDR.

1

Storage

A

To next page

General Register (R) — DE002 DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DE002 DF002 DG002

ALU

DE008 DF008 DG008

Z Register — DE974 DF974 DG974

X Gate Z Bus to M Bus (CC005)

Set SDR Byte (CS007)

SDR — DN001

Instruction	Operation
STH	B Reg Direct

See page 6-100.

Note: See page 6-000 for data flow bit card locations.

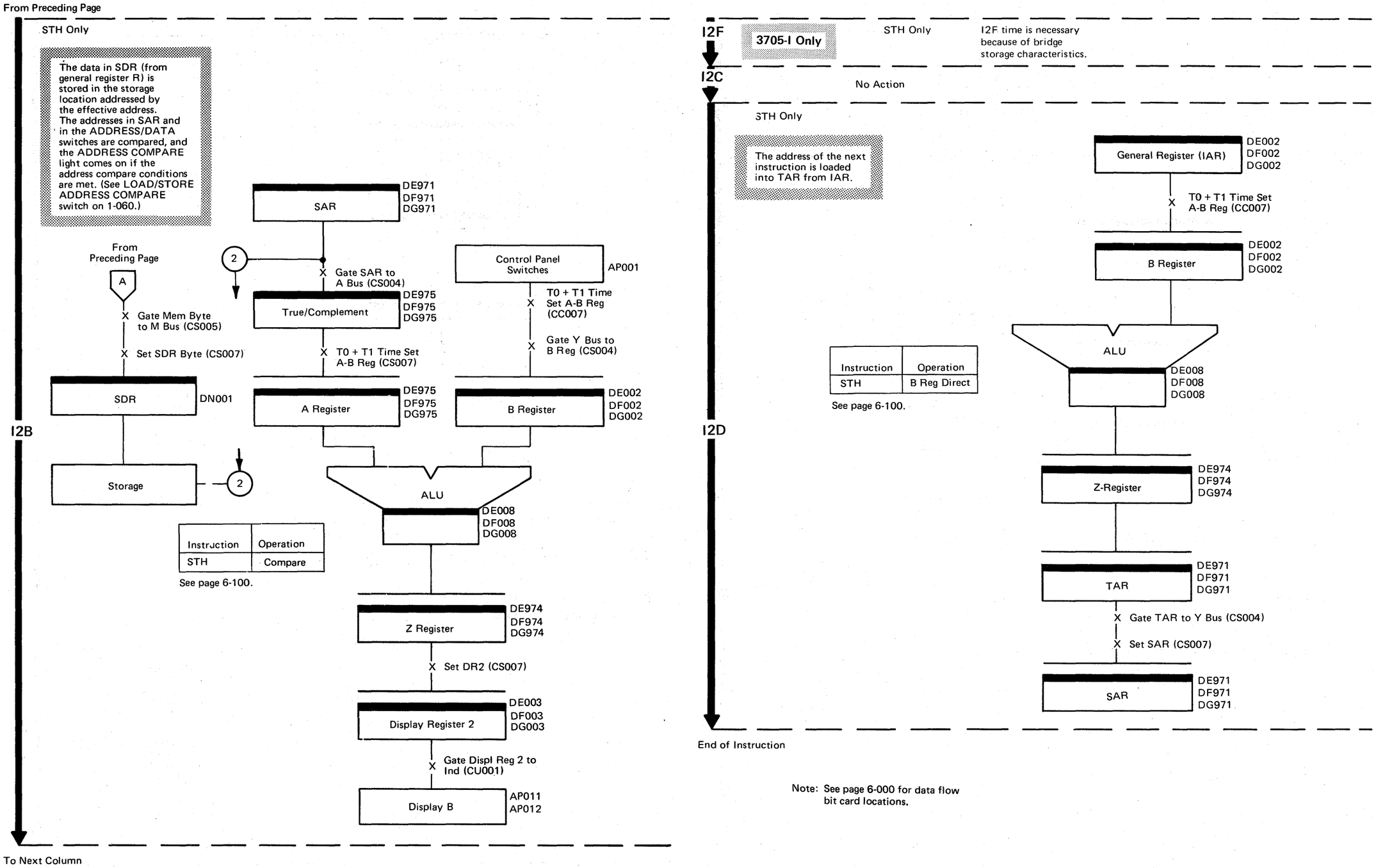
I2E

3705-I Only

I2E time is necessary because of bridge storage characteristics.

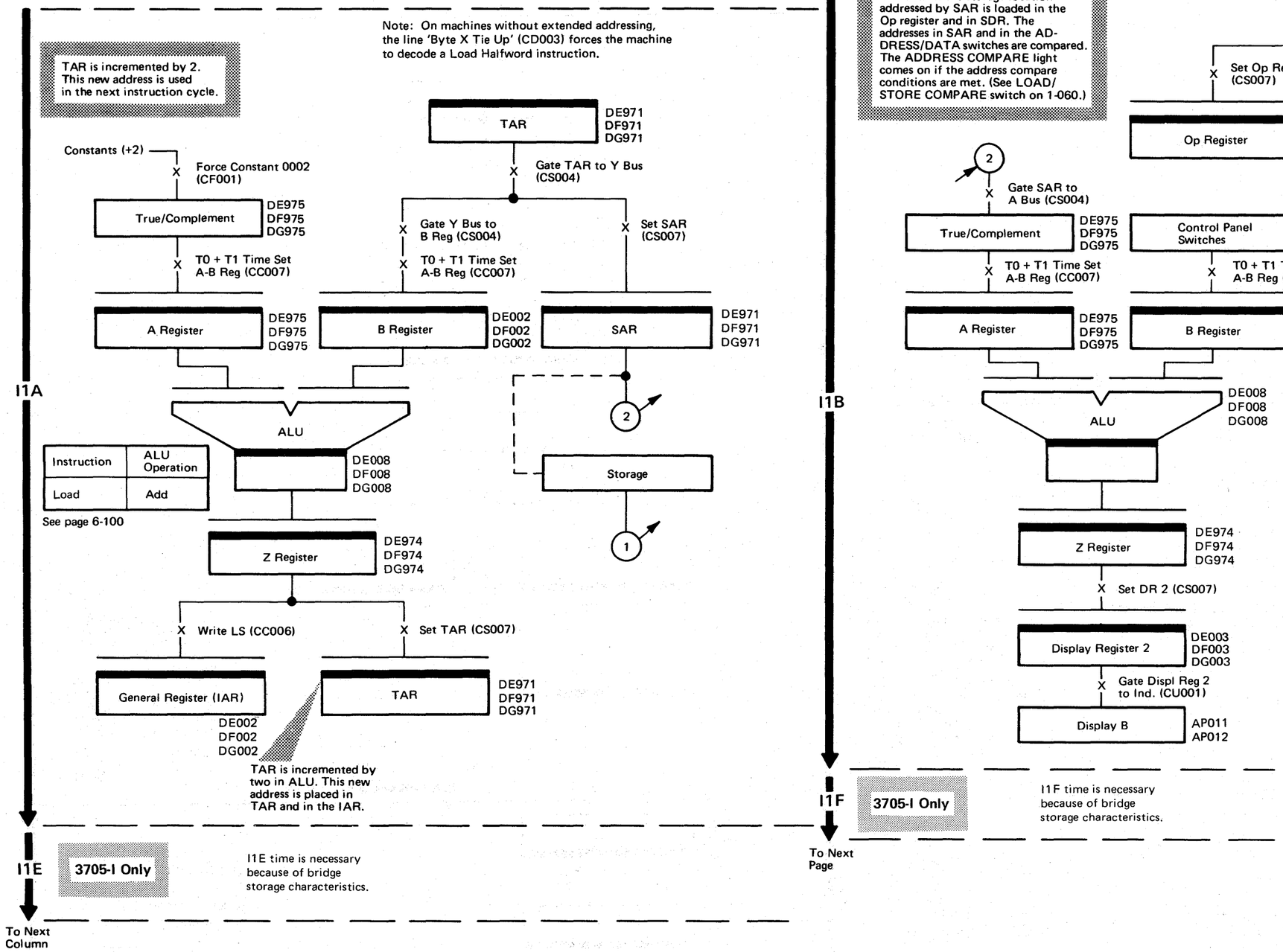
To Next Page

CCU

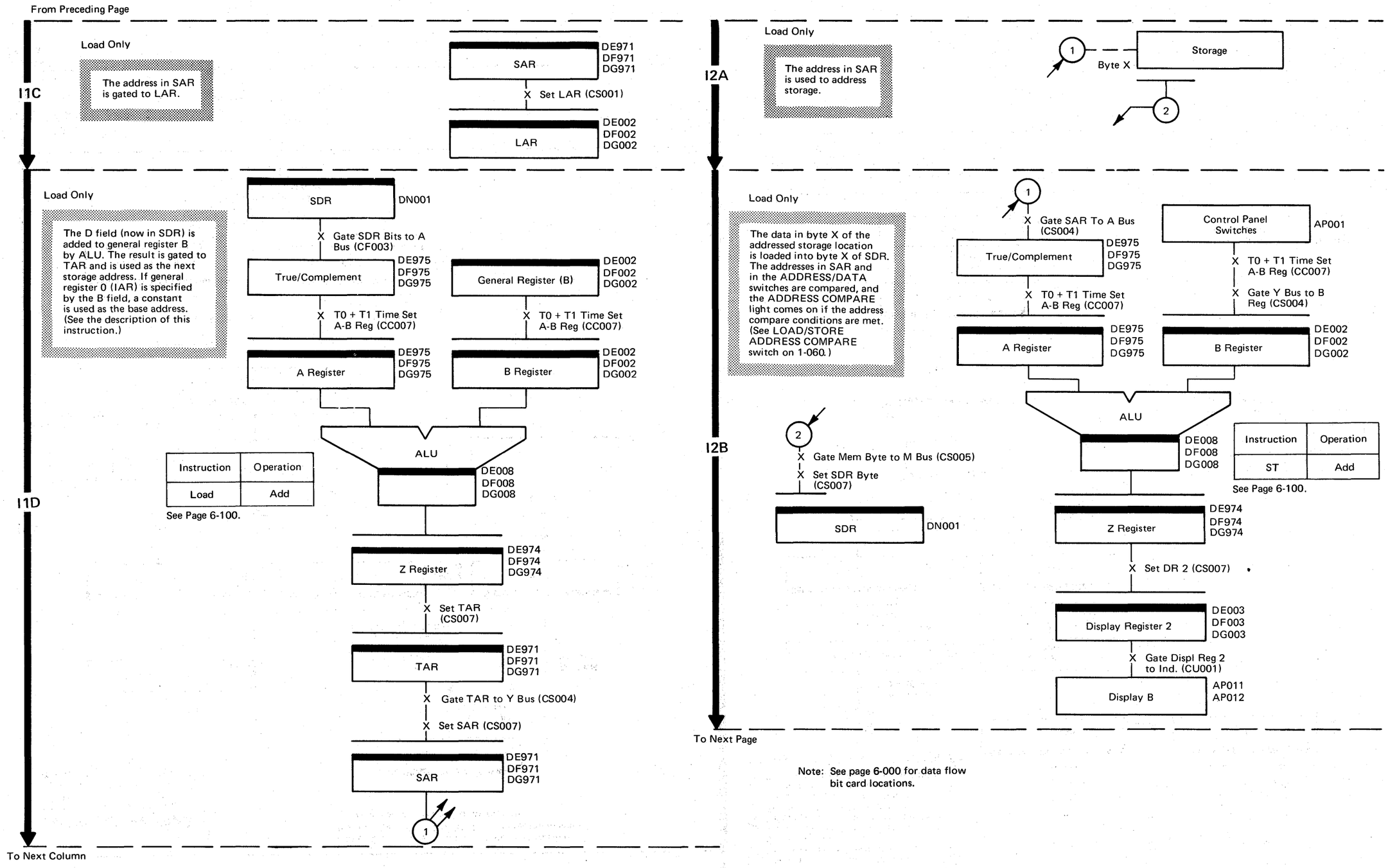


Note: See page 6-000 for data flow bit card locations.

LOAD INSTRUCTION OPERATION



Note: See page 6-000 for data flow bit card locations.



Note: See page 6-000 for data flow bit card locations.

From Preceding Page

I2F

3705-I Only

Load Only

I2F time is necessary because of bridge storage characteristics.

I2C

Load Only

No Action

Load Only

The address in TAR is incremented by 2.

Constant (+2)

X Force Constant 0002 (CF001)

True/Complement — DE975 DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DE975 DF975 DG975

TAR — DE971 DF971 DG971

X Gate TAR to Y Bus (CS004)

X Gate Y Bus to B Reg (CS004)

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DE002 DF002 DG002

ALU

DE008 DF008 DG008

Z Register — DE974 DF974 DG974

X Set TAR (CS007)

TAR — DE971 DF971 DG971

X Gate TAR to Y Bus (CS004)

X Set SAR (CS007)

SAR — DE971 DF971 DG971

(1)

I2D

Instruction	Operation
Load	Add

See page 6-100.

To Next Column

Load Only

I3A

The address in SAR is used to address storage.

(1) Storage

Bytes 0 and 1 (2)

I3E

3705-I Only

Load Only

I3E time is necessary because of bridge storage characteristics.

Load Only

The data in bytes 0 and 1 of the addressed storage location is loaded into bytes 0 and 1 of SDR. The addresses in SAR and in the ADDRESS/DATA switches are compared, and the ADDRESS COMPARE light comes on if the address compare conditions are met. (See LOAD/STORE ADDRESS COMPARE switch on 1-060.)

(1)

X Gate SAR To A Bus (CS004)

True/Complement — DE975 DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DE975 DF975 DG975

Control Panel Switches — AP001

X T0 + T1 Time Set A-B Reg (CC007)

X Gate Y Bus to B Reg (CS004)

B Register — DE002 DF002 DG002

ALU

DE008 DF008 DG008

Instruction	Operation
Load	Compare

See page 6-100.

(2)

X Gate Mem Byte to M Bus (CS005)

X Set SDR Byte (CS007)

SDR — DN001

Z Register — DE974 DF974 DG974

X Set DR 2 (CS007)

Display Register 2 — DE003 DF003

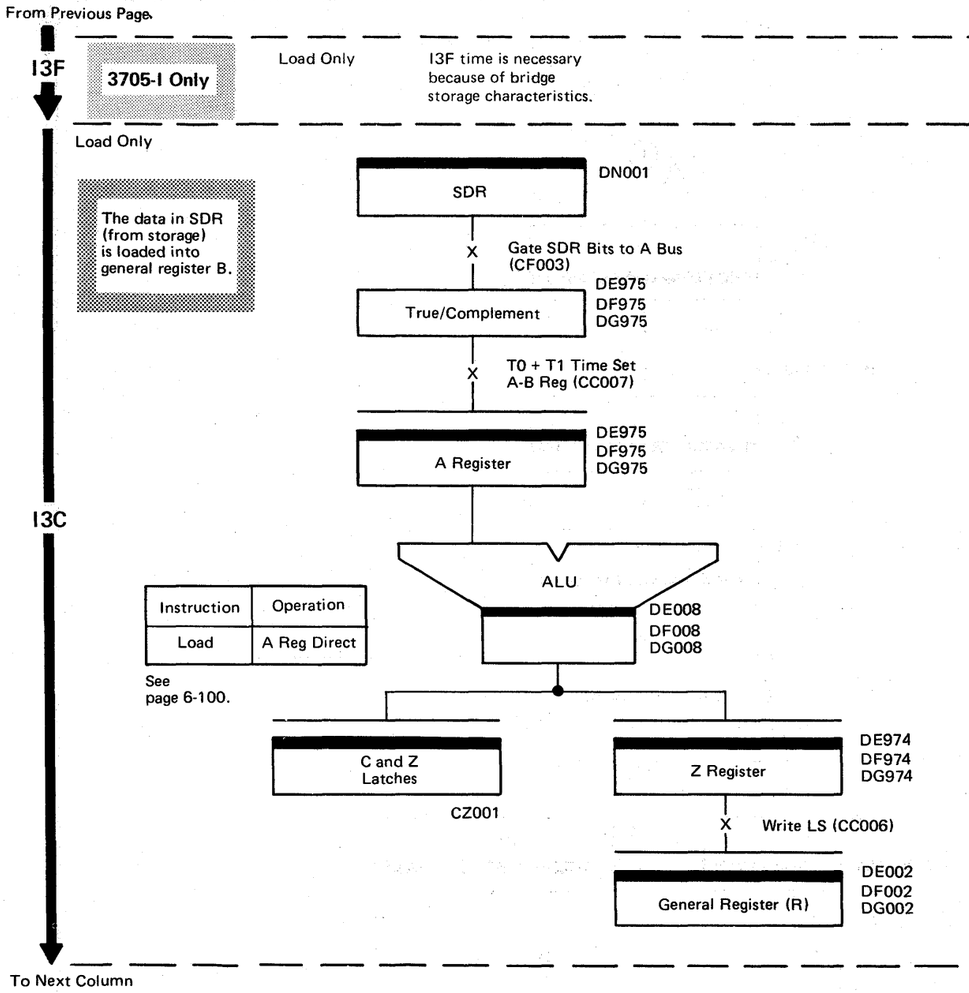
X Gate Displ Reg 2 to Ind. (CU001)

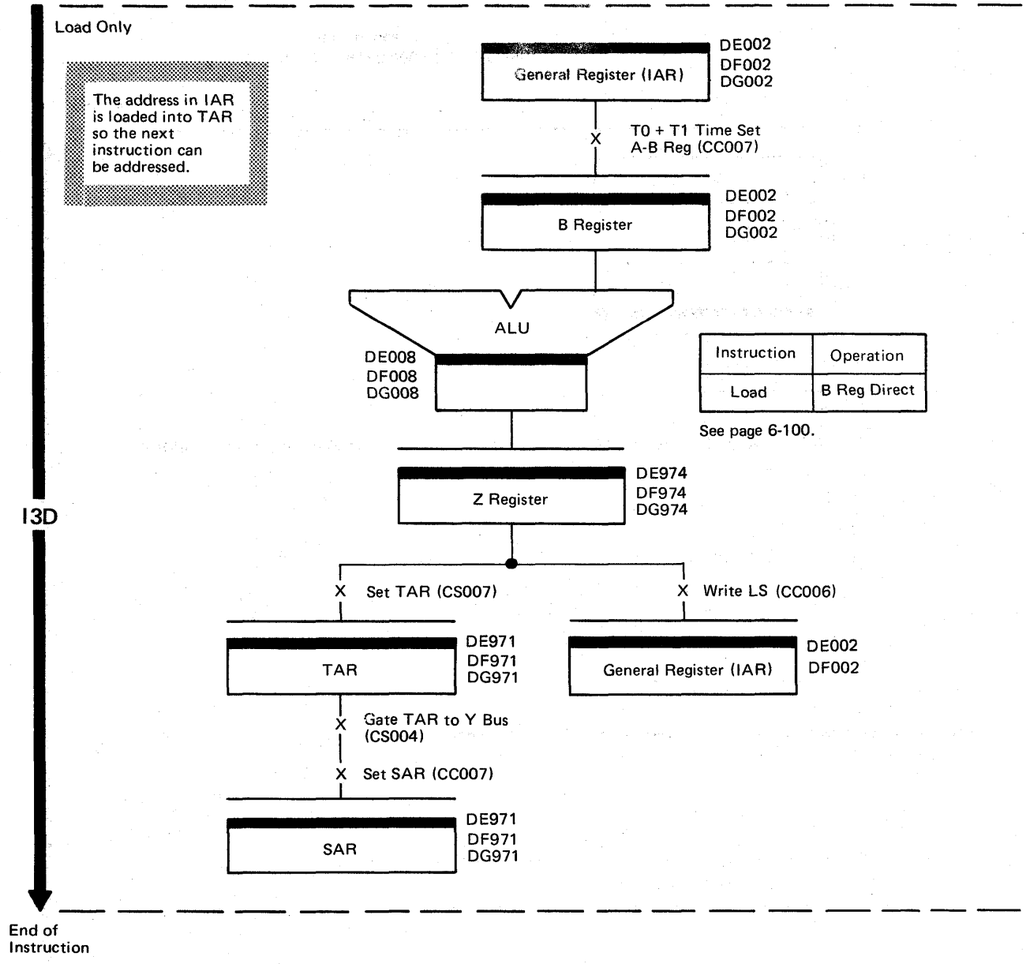
Display B — AP011 AP012

I3B

To Next Page

Note: See page 6-000 for data flow bit card locations.





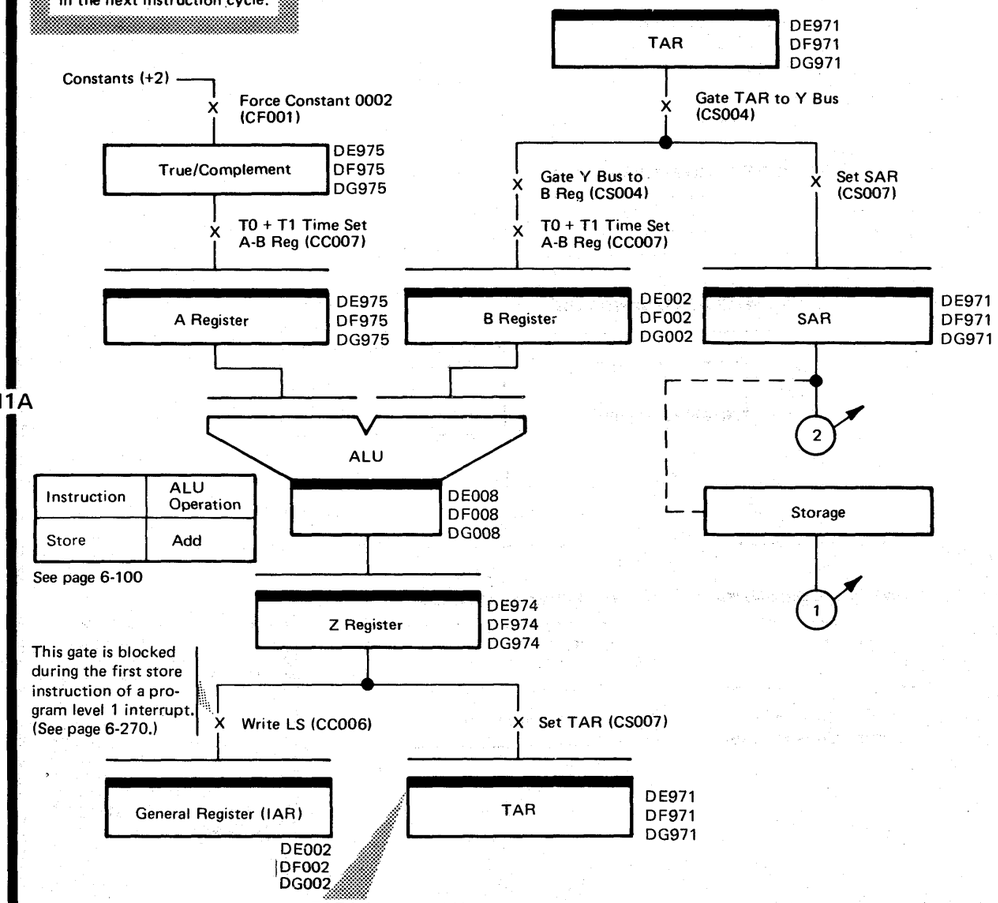
Note: See page 6-000 for data flow bit card locations.

STORE INSTRUCTION OPERATION

Note: On machines without extended addressing, the line 'Byte X Tie Up' (CD003) forces the machine to decode a Store Halfword instruction.

TAR is incremented by 2. This new address is used in the next instruction cycle.

The address exception checks made during each instruction cycle are not shown. See ALD pages CM002 and CM003.



Instruction	ALU Operation
Store	Add

See page 6-100

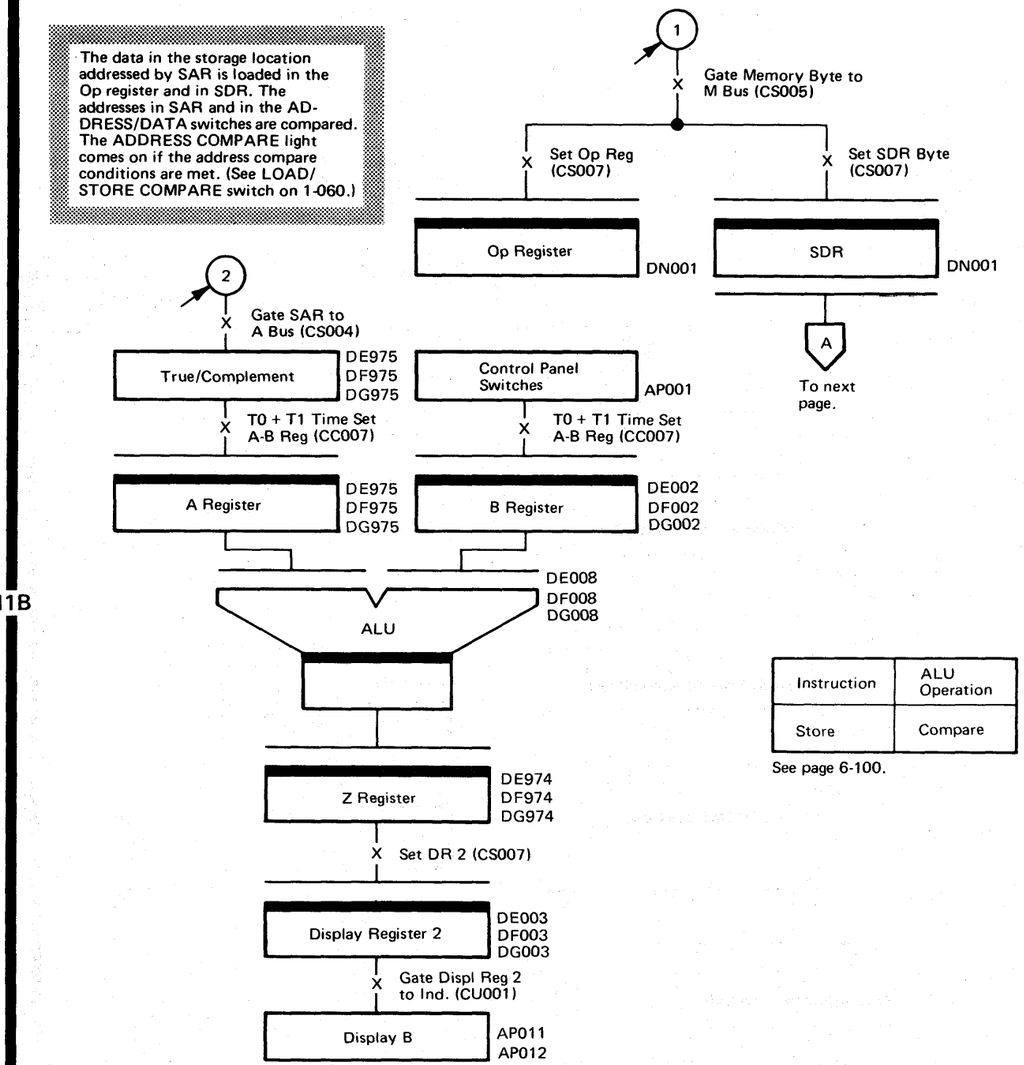
I1A

I1E **3705-I Only**

I1E time is necessary because of bridge storage characteristics.

To Next Column

The data in the storage location addressed by SAR is loaded in the Op register and in SDR. The addresses in SAR and in the ADDRESS/DATA switches are compared. The ADDRESS COMPARE light comes on if the address compare conditions are met. (See LOAD/STORE COMPARE switch on 1-060.)



To next page.

Instruction	ALU Operation
Store	Compare

See page 6-100.

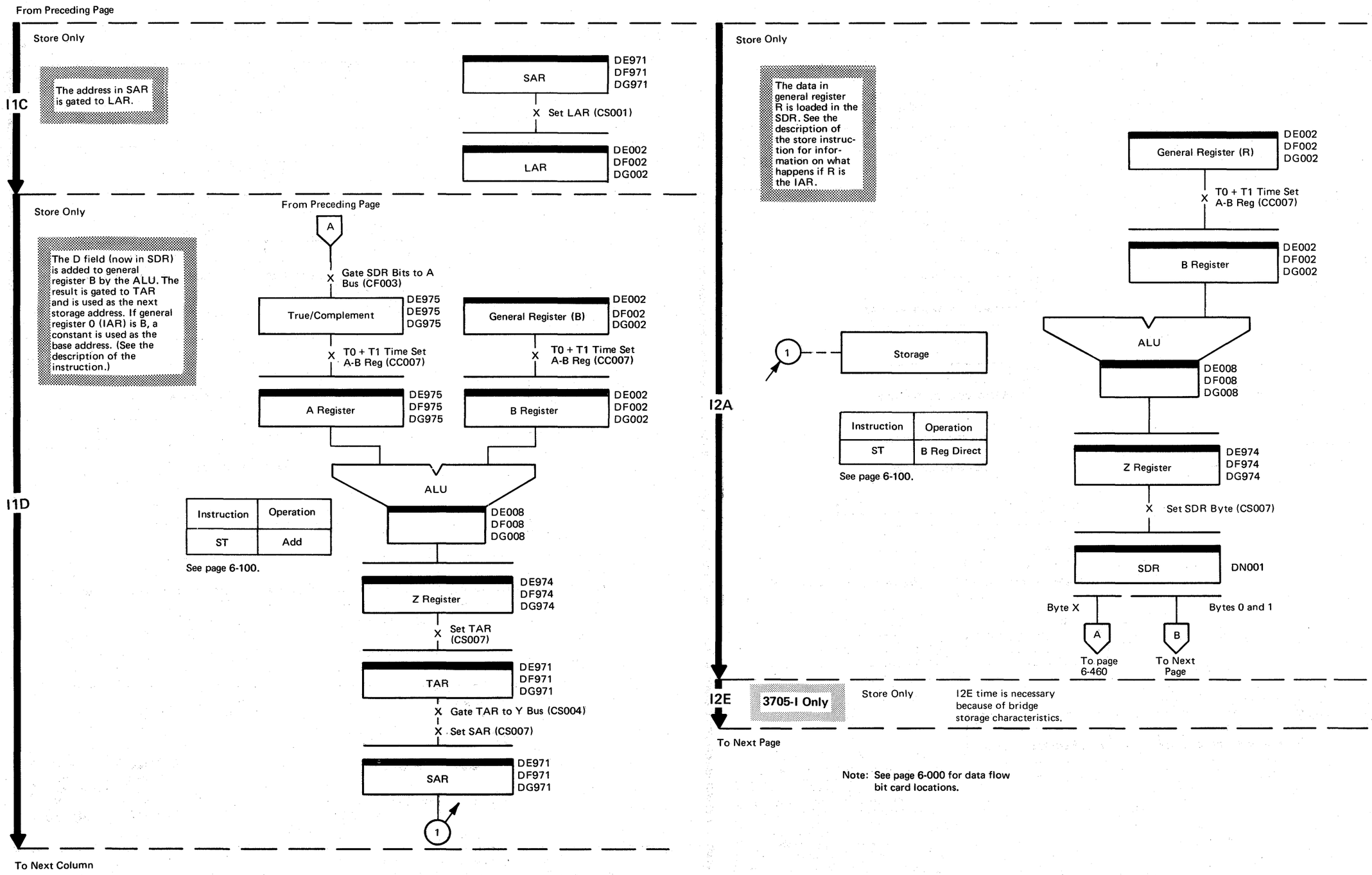
I1B

I1F **3705-I Only**

I1F time is necessary because of bridge storage characteristics.

To Next Page

Note: See page 6-000 for data flow bit card locations.



Note: See page 6-000 for data flow bit card locations.

From Preceding Page

Store Only

Bytes 0 and 1 of the SDR are placed in storage. The addresses in the SAR and in the ADDRESS/DATA switches are compared, and the ADDRESS COMPARE light comes on if the address compare conditions are met. (See LOAD/STORE ADDRESS COMPARE switch on 1-060.)

From Preceding Page

B

Bytes 0 and 1

Storage

SAR — DF971 DG971

X Gate SAR To A Bus (CS004)

True/Complement — DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

Control Panel Switches — AP001

X T0 + T1 Time Set A-B Reg (CC007)

X Gate Y Bus to B Reg (CS004)

A Register — DF975 DG975

B Register — DF002 DG002

ALU

DF008 DG008

Z Register — DF974 DG974

X Set DR 2 (CS007)

Display Register 2 — DF003 DG003

X Gate Displ Reg 2 to Ind. (CU001)

Display B — AP012

Instruction	Operation
ST	Compare

See page 6-100.

I2B

I2F

3705-I Only

Store Only

I2F time is necessary because of bridge storage characteristics.

I2C

Store Only

No Action

To Next Column

I2D

Store Only

The address in TAR is decremented by 2.

Constant (-2)

X Force Constant 0002 (CF001)

True/Complement — DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

TAR — DF971 DG971

X Gate TAR to Y Bus (CS004)

X Gate Y Bus to B Reg (CS004)

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DF975 DG975

B Register — DF002 DG002

ALU

DF008 DG008

Instruction	Operation
ST	Subtract

See page 6-100.

Z Register — DF974 DG974

X Set TAR (CS007)

TAR — DF971 DG971

X Gate TAR to Y Bus (CS004)

SAR — DF971 DG971

C

To Next Page

I3A

The address in the SAR is used to address storage.

Storage

To Next Page

Note: See page 6-000 for data flow bit card locations.

From Preceding Page

I3E — 3705-I Only — Store Only

I3E time is necessary because of bridge storage characteristics.

I3C — Store Only — No Action

Store Only

Byte X of SDR is stored in the storage location addressed by the SAR. The addresses in the SAR and in the ADDRESS/DATA switches are compared, and the ADDRESS COMPARE light comes on if the address compare conditions are met. (See LOAD/STORE ADDRESS COMPARE switch on 1-060.)

From Preceding Page

C

X Gate SAR To A Bus (CS004)

Control Panel Switches — AP001

True/Complement — DE975 DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

X Gate Y Bus to B Reg (CS004)

From Page 6-440

A

I3B

Byte X

Storage

A Register — DE975 DF975 DG975

B Register — DE002 DF002 DG002

ALU — DE008 DF008 DG008

Instruction	Operation
ST	Compare

See page 6-100.

Z Register — DE974 DF974 DG974

X Set DR 2 (CS007)

Display Register 2 — DE003 DF003 DG003

X Gate Displ Reg 2 to Ind. (CU001)

Display B — AP011 AP012

I3F — 3705-I Only — Store Only

I3F time is necessary because of bridge storage characteristics.

To Next Column

I3D

The data in register 0 (IAR) is loaded into the TAR and back into the IAR.

Instruction	Operation
ST	B Reg Direct

See page 6-100.

General Register (IAR) — DE002 DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DE002 DF002 DG002

ALU — DE008 DF008 DG008

Z Register — DE974 DF974 DG974

X Set TAR (CS007)

X Write LS (CC006)

TAR — DE971 DF971 DG971

General Register (IAR) — DE002 DF002 DG002

Force interrupt address X'0012' during program level 1 interrupt (CS004) see page 6-270.

X Gate TAR to Y Bus (CS004)

X Set SAR (CS007)

SAR — DE971 DF971 DG971

End of Instruction

Note: See page 6-000 for data flow bit card locations.

REGISTER AND STORAGE WITH ADDITION (RSA) INSTRUCTIONS

The CCU takes an I1 and an I2 cycle to execute either the 'insert character and count' or 'store character and count' instructions.

For the 'ICT' and 'STCT" instructions, the general register designated by the R field in the instruction must be an odd-numbered register; therefore, the general register = (2xR) +1.

INSERT CHARACTER AND COUNT (ICT)

0	1-3	4	5-6	7	8	9	10	11	12	13	14	15
0	B	0	R	N	0	0	0	1	0	0	0	0

The B field specifies a general register in the active group. The register contains an address (effective address) that is used to address storage. The content of the register specified by B is incremented by 1 after the effective address has been obtained. The byte at the effective address is placed in byte 0 (N=0) or byte 1 (N=1) of the general register designated by the R field. The register specified by R must be an odd-numbered register. Register 0 should not normally be specified in the B field because it contains the instruction address.

The 'C' and 'Z' latches are not changed.

Note: If the registers specified by B and R are the same, the contents of byte 1 of the register is incremented before the 8-bit character is inserted. If N=1, the inserted character then overlays byte 1 of the same register, and the previous incrementing has no significance. If N=0, the character is inserted into byte 0 of the register, and byte 1 contains the original value plus 1.

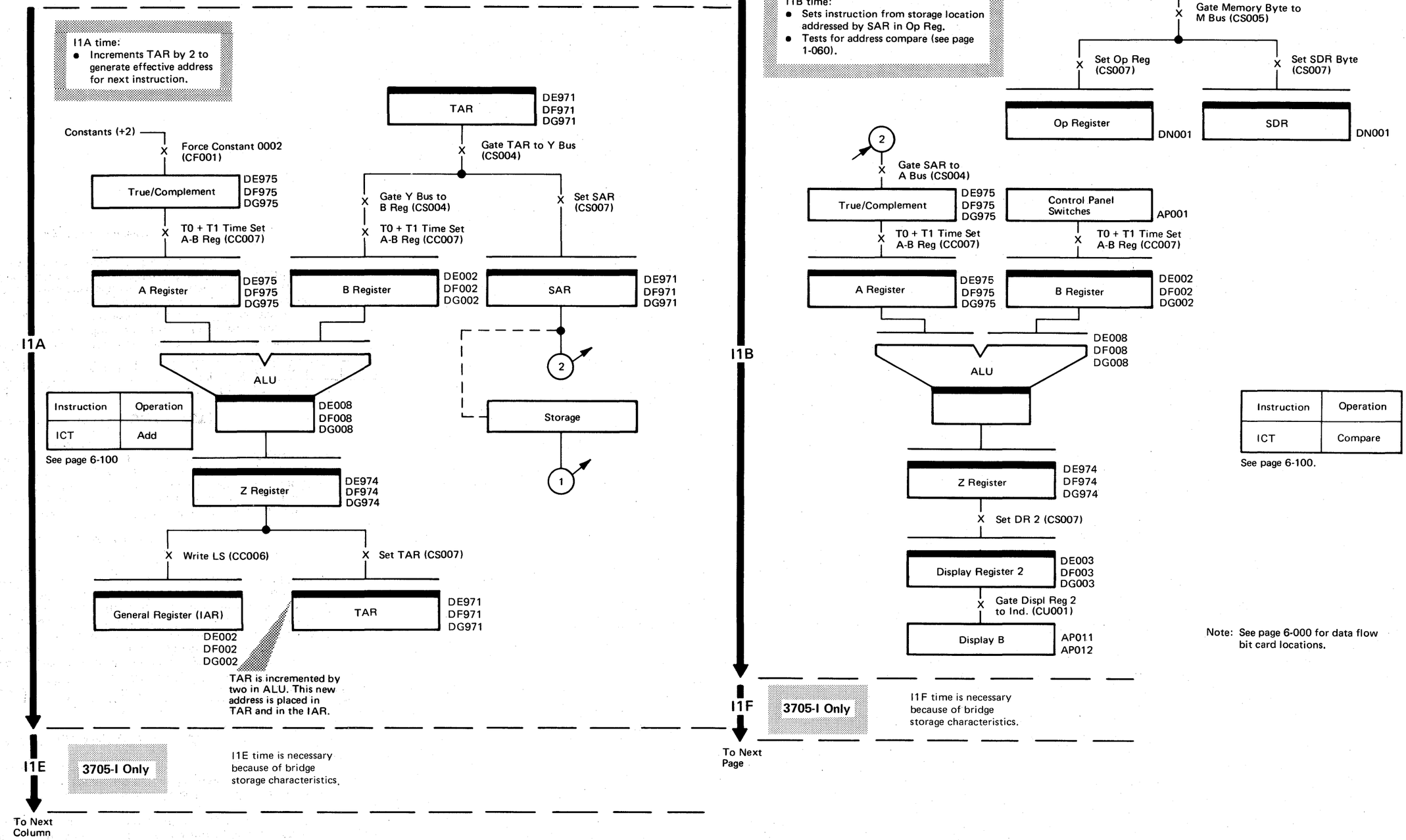
STORE CHARACTER AND COUNT (STCT)

0	1-3	4	5-6	7	8	9	10	11	12	13	14	15
0	B	0	R	N	0	0	1	1	0	0	0	0

The B field specifies a general register in the active group. This register contains an address (effective address) that is used to select a storage location. The content of the register specified by B is incremented by 1. Byte 0 (N=0) or byte 1 (N=1) of the general register specified by R is then stored at the effective address. The register specified by R must be an odd-numbered register. Register 0 should not be specified by the B field because it contains the instruction address.

The 'C' and 'Z' latches are not changed.

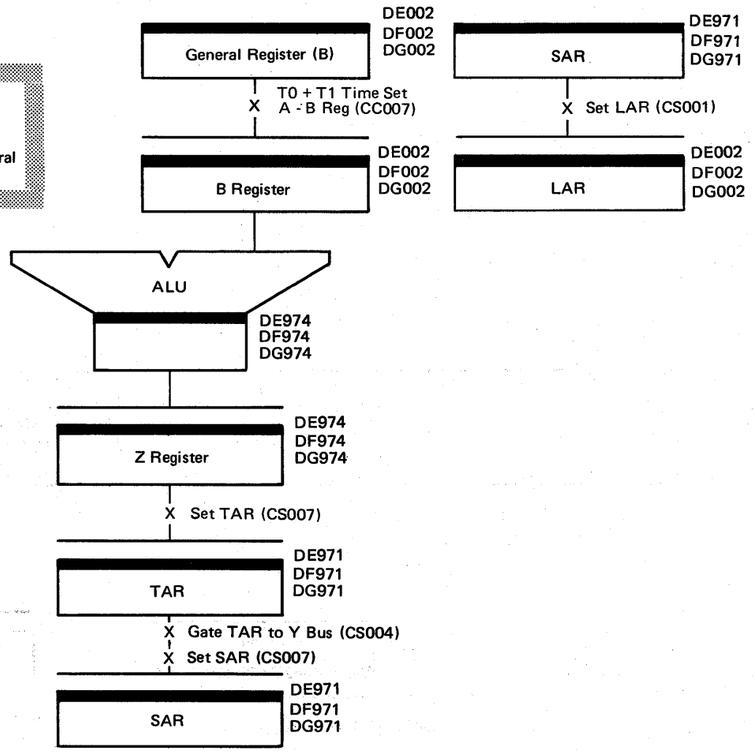
ICT INSTRUCTION OPERATION



From Preceding Page

ICT Only

I1C time:
- Preserves the instruction address in LAR.
- Places the address from General Register (B) into SAR.



Instruction	Operation
ICT	B Reg Direct

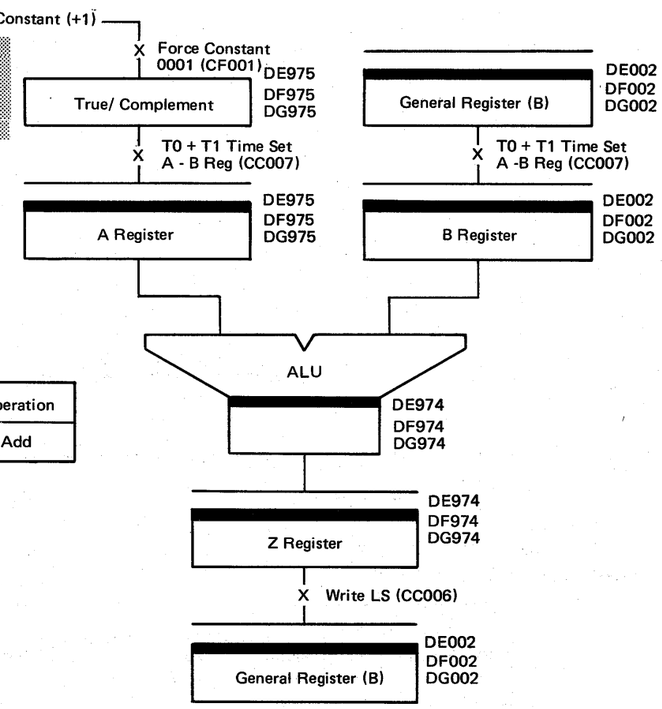
See page 6-100.

I1C

To Next Column

ICT Only

I1D time:
- Increments the contents of General Register B by 1.



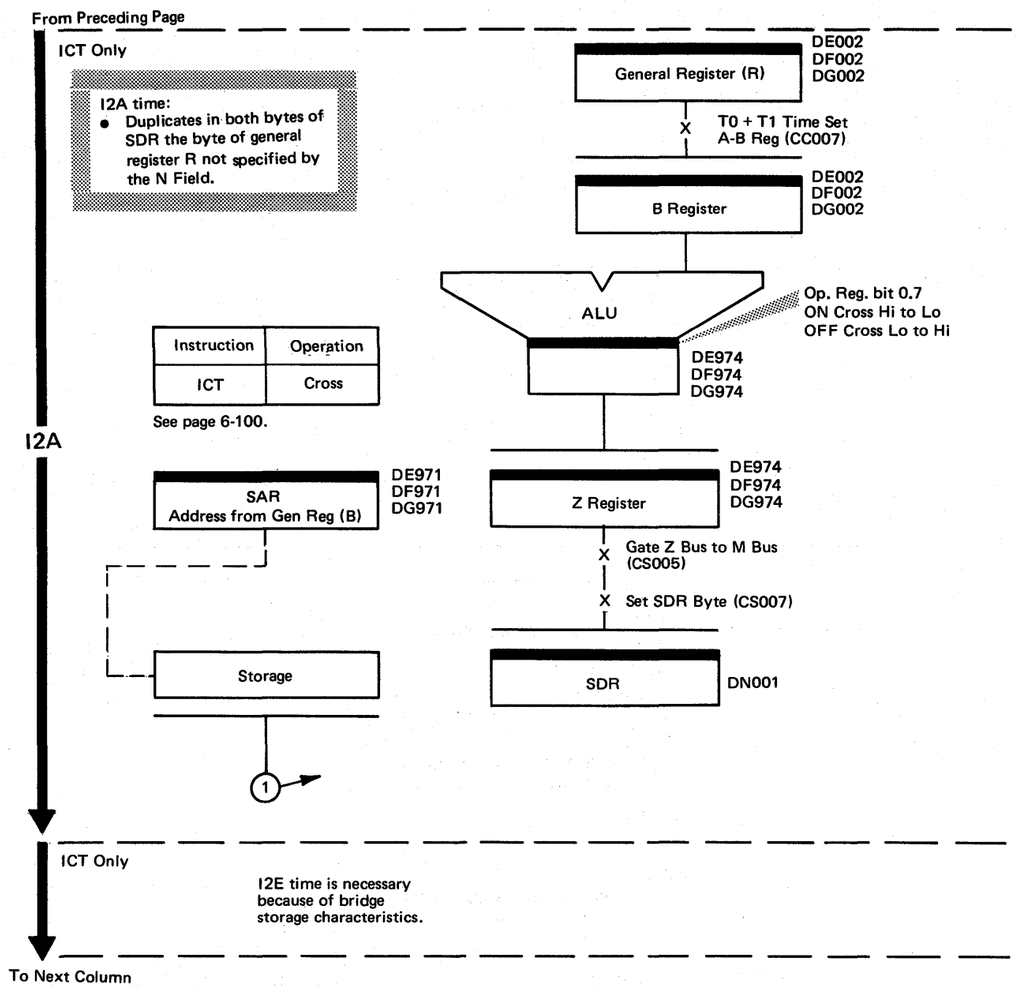
Instruction	Operation
ICT	Add

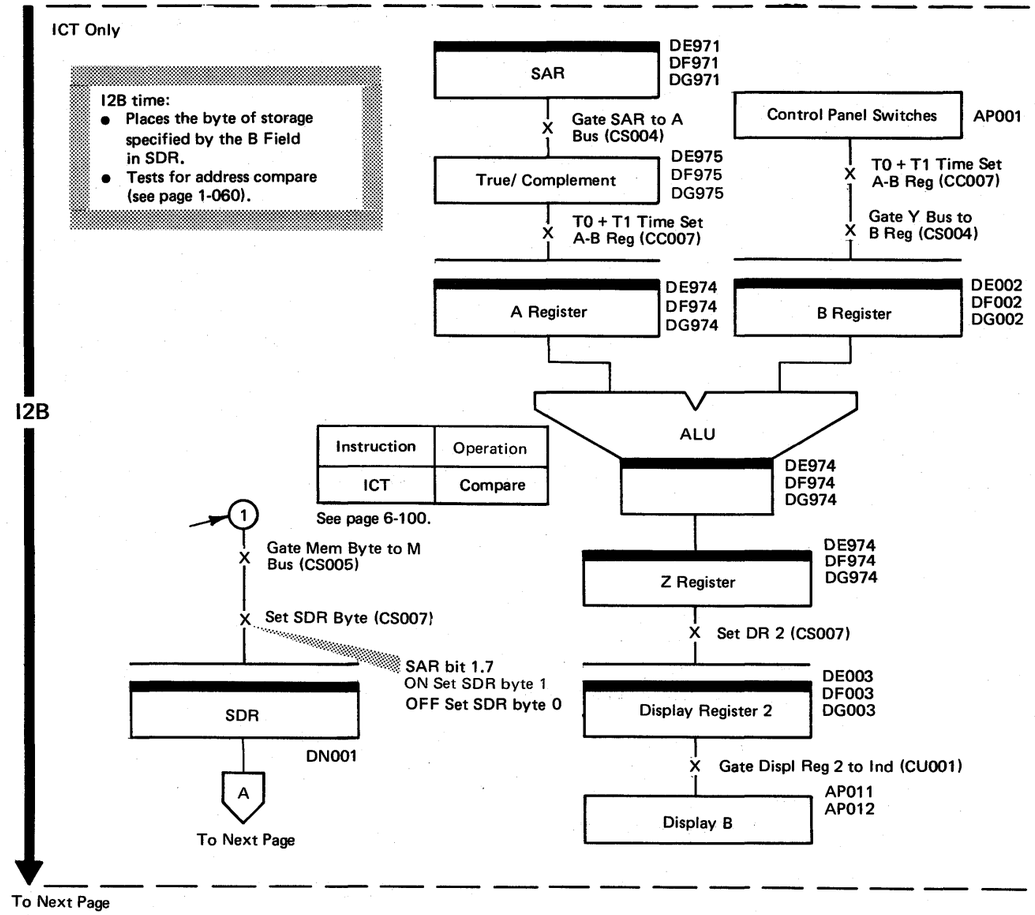
See page 6-100.

I1D

To Next Page

Note: See page 6-000 for data flow bit card locations.





Note: See page 6-000 for data flow bit card locations.

From Preceding Page

I2F

3705-I Only

ICT Only

I2F time is necessary because of bridge storage characteristics.

ICT Only

I2C time:
- Transfer the bytes A Reg Direct when the N field specifies the same byte as the B field.
- Crosses the bytes when the N field and the B field specify different bytes.

I2C

From Preceding Page

A

X Gate SDR Bits to A Bus (CF003)

True/ Complement — DE975 DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DE975 DF975 DG975

ALU — DE974 DF974 DG974

Z Register — DE974 DF974 DG974

X Write LS (CC006)

General Register (R) — DE002 DF002 DG002

Instruction	Operation
ICT	*Cross or A Reg Direct

See page 6-100.

*Note: Cross Hi to Lo and Lo to Hi

To Next Column

ICT Only

I2D time:
- Loads the address of the next instruction in TAR and SAR.

I2D

Instruction	Operation
ICT	B Reg Direct

See page 6-100.

General Register (IAR) — DE002 DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DE002 DF002 DG002

ALU — DE974 DF974 DG974

Z Register — DE974 DF974 DG974

X Set TAR (CS007)

TAR — DE971 DF971 DG971

X Gate TAR to Y Bus (CS004)

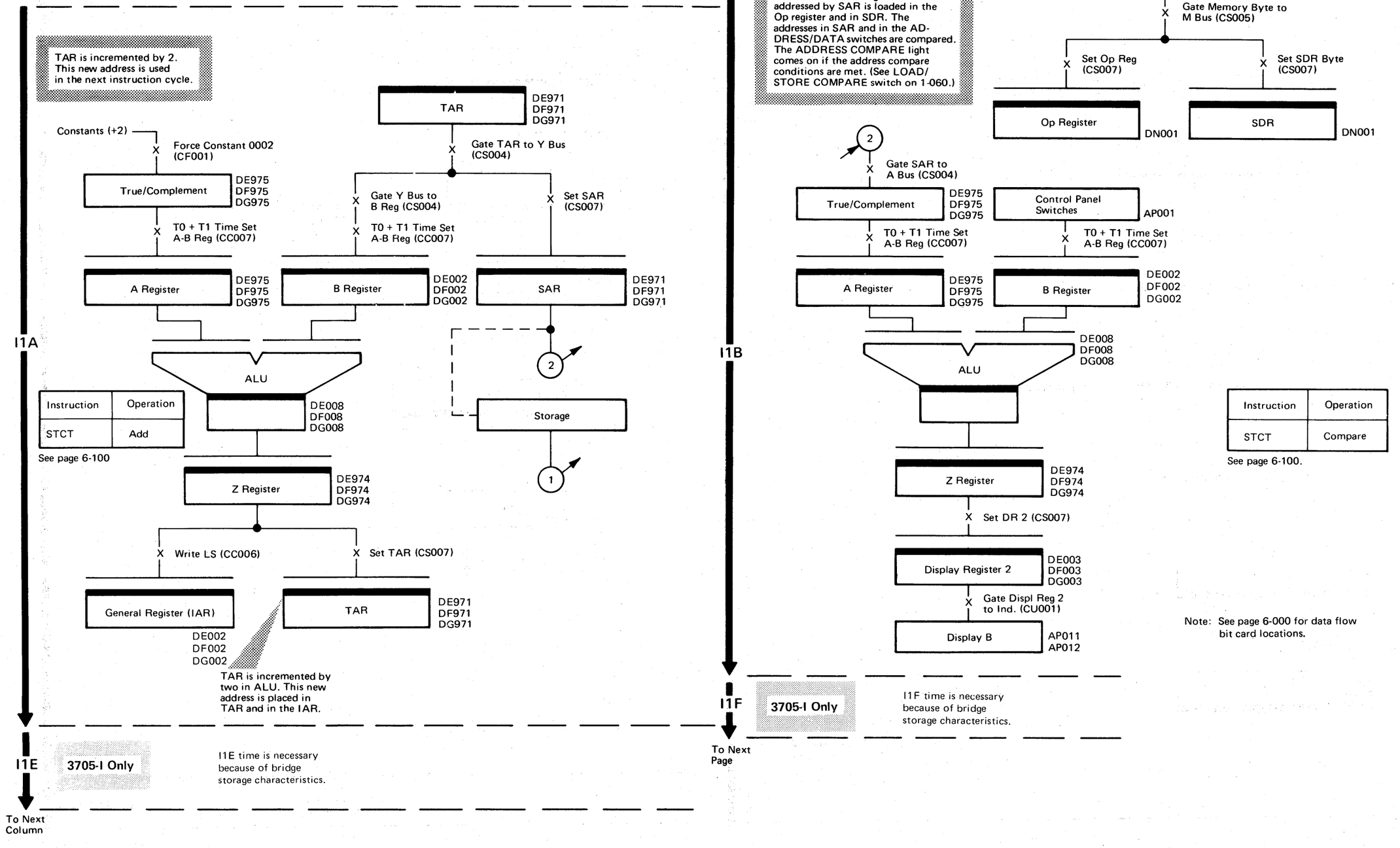
X Set SAR (CS007)

SAR — DE971 DF971 DG971

End of Instruction

Note: See page 6-000 for data flow bit card locations.

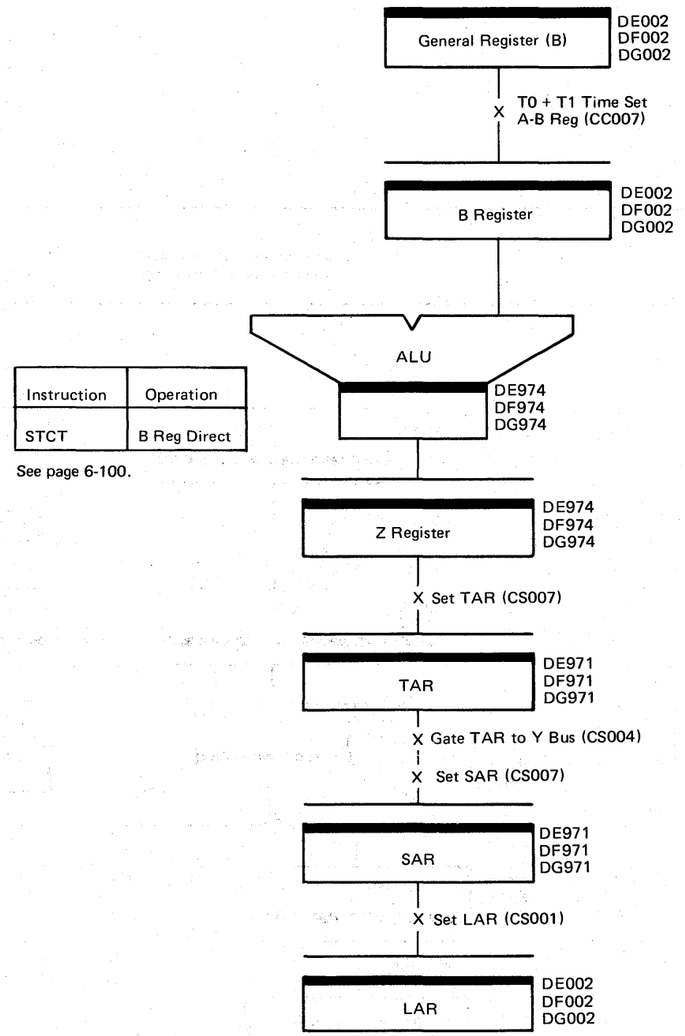
STCT INSTRUCTION OPERATION



From Preceding Page

STCT Only

The address in general register B is placed in SAR so it can be used to address storage.

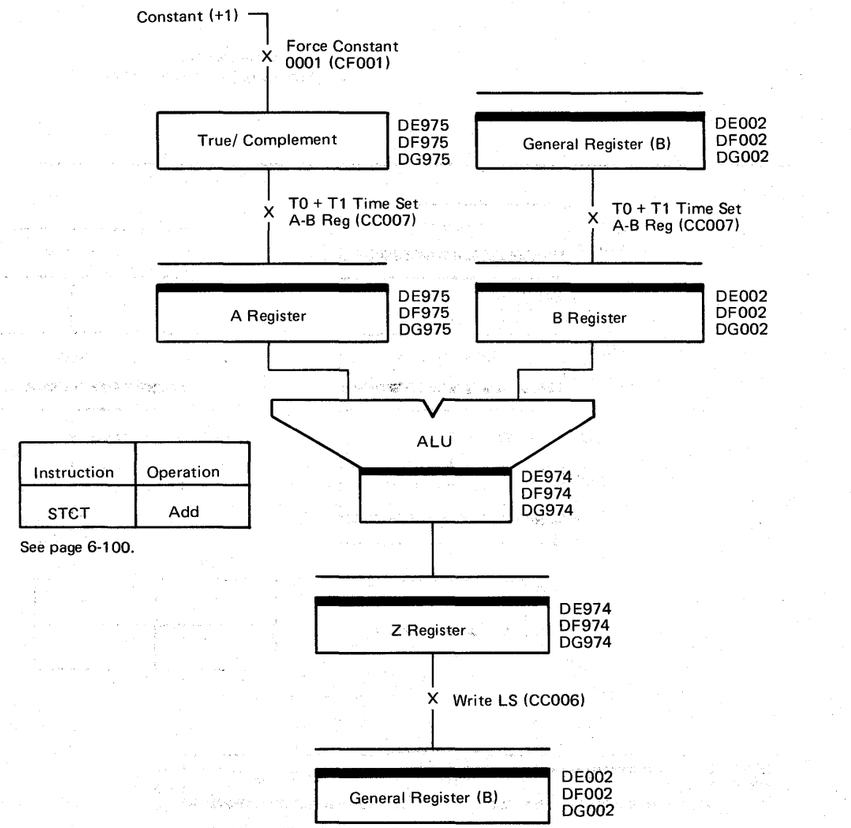


I1C

To Next Column

STCT Only

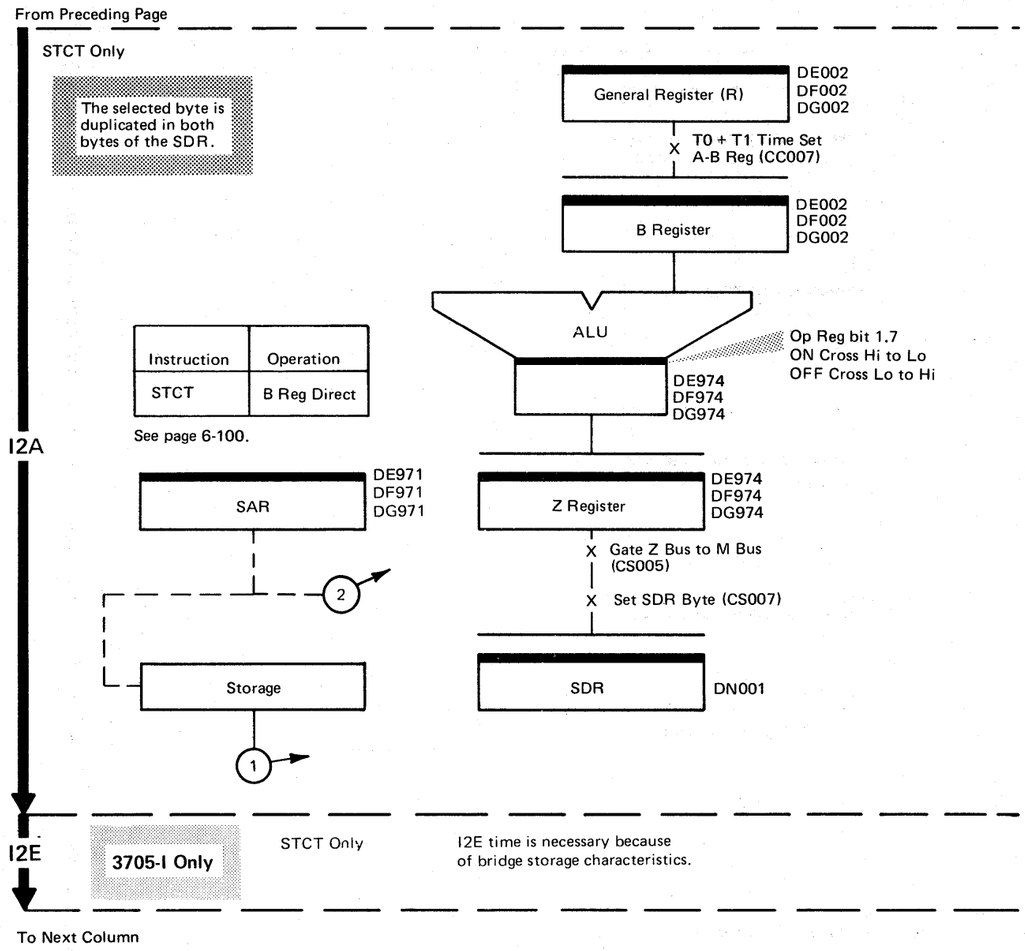
The content of general register B is incremented by 1.

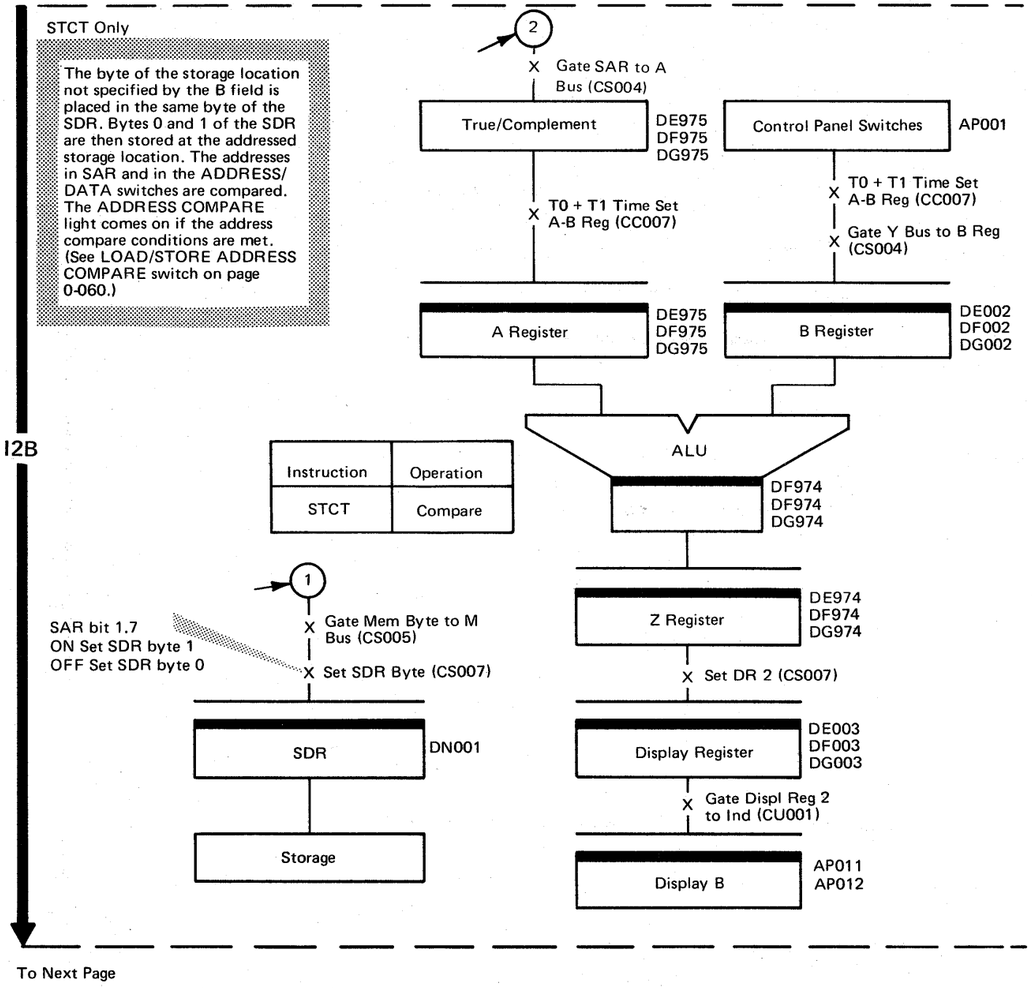


I1D

To Next Page

Note: See page 6-000 for data flow bit card locations.





Note: See page 6-000 for data flow bit card locations.

From Preceding Page

I2F

3705-I Only

STCT Only

I2F time is necessary because of bridge storage characteristics.

I2C

STCT Only

No Action

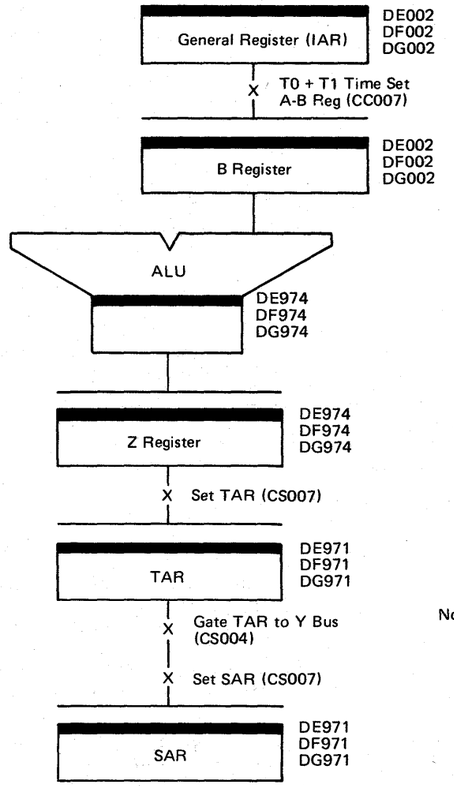
STCT only

The address of the next instruction is loaded into TAR and SAR.

I2D

Instruction	Operation
STCT	B Reg Direct

See page 6-100.



Note: See page 6-000 for data flow bit card locations.

End of Instruction

REGISTER AND IMMEDIATE ADDRESS (RA) INSTRUCTIONS

The CCU takes an I1 and an I2 cycle to execute either the 'branch and link' or the 'load address' instruction.

The 'branch and link' and 'load address' instructions are the only 32-bit instructions for the 3705.

BRANCH AND LINK (BAL)

0	1	2	3	4	5-7	8	9	10	11	12–31
1	0	1	1	1	R	0	0	0	0	A

This instruction causes an unconditional branch to the storage address specified by the A field. The contents of general register 0 (IAR) are moved to the general register specified by the R field to provide for subroutine linkage. The address in the A field is then placed in register 0. Since register 0 is the IAR, no linkage is provided if it is specified by R. Bits 12, 13, 14 and 15 of the A field are used only with Extended Addressing.

The 'C' and 'Z' latches are not changed.

LOAD ADDRESS (LA)

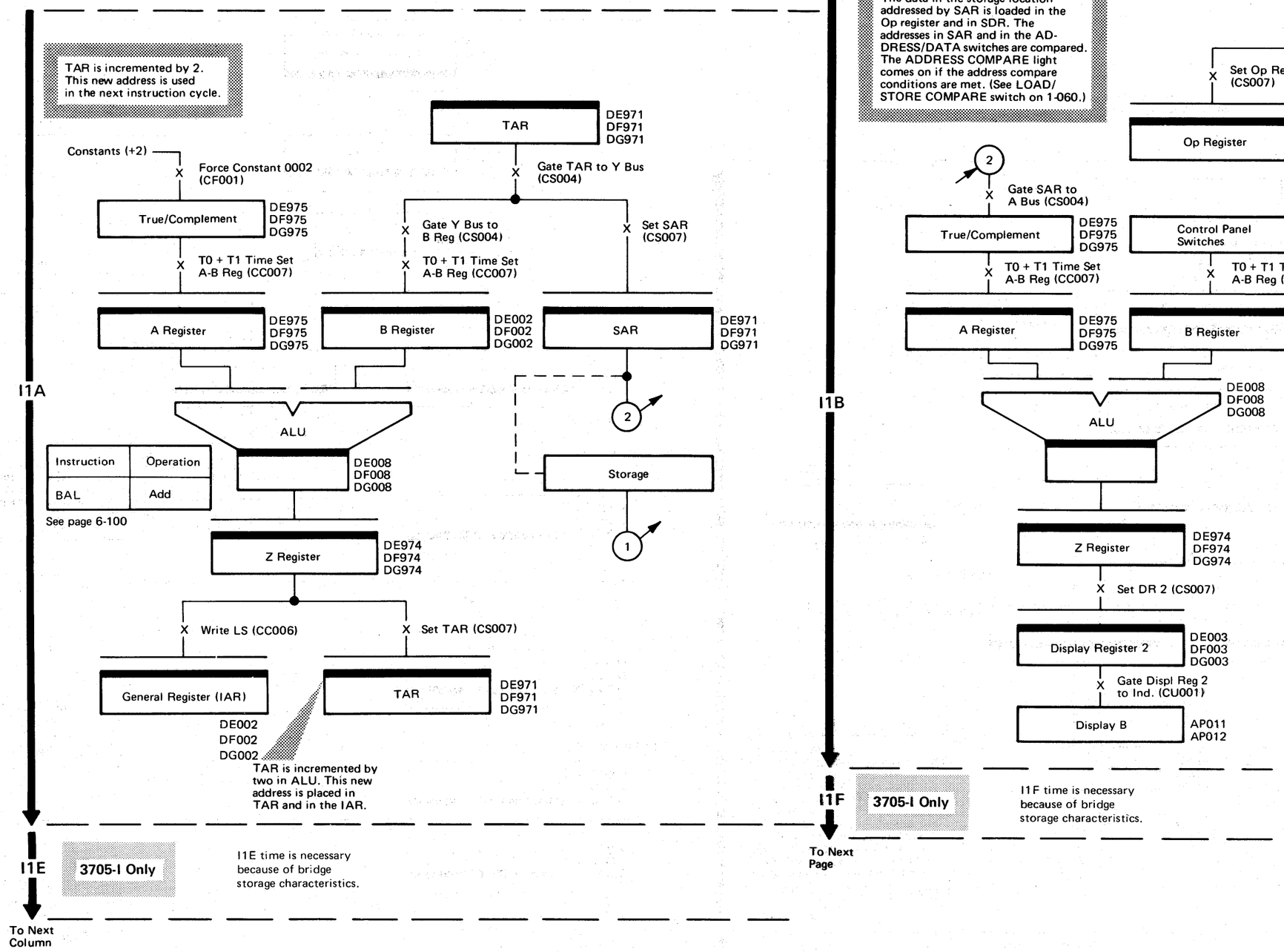
0	1	2	3	4	5-7	8	9	10	11	12–31
1	0	1	1	1	R	0	0	1	0	A

This instruction places the contents of the A field in the general register specified by the R field. With Extended Addressing, bits 12, 13, 14 and 15 of the A field are loaded into byte X of R. Without Extended Addressing, these bits are ignored.

The 'C' and 'Z' latches are not changed.

Note: If general register 0 (IAR) is addressed, an unconditional branch occurs to the instruction located at the storage address specified by the A field.

BAL INSTRUCTION OPERATION



From Preceding Page

I1C

BAL Only

The address in SAR is placed in LAR.

SAR — DE971 DF971 DG971

X Set LAR (CS001)

LAR — DE002 DF002 DG002

I1D

BAL Only

The address in TAR is placed in SAR.

TAR — DE971 DF971 DG971

X Gate TAR to Y Bus (CS004)

X Set SAR (CS007)

SAR — DE971 DF971 DG971

(1)

I2A

BAL Only

The address in TAR is incremented by 2 and placed in general register R, and serves as the backward link. A storage fetch operation fetches the second halfword of the BAL instruction.

Constant (+2)

X Force Constant 0002 (CF001)

True/Complement — DE975 DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DE975 DF975 DG975

TAR — DE971 DF971 DG971

X Gate TAR to Y Bus (CS004)

X Gate Y Bus to B Reg (CS004)

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DE002 DF002 DG002

Instruction	Operation
BAL	Add

See page 6-100.

ALU — DE974 DF974 DG974

(1) Storage (2)

Z Register — DE974 DF974 DG974

X Write LS (CC006)

General Register (R) — DE002 DF002 DG002

To Next Column

I2E

3705-I Only

BAL Only

I2E time is necessary because of bridge storage characteristics.

BAL Only

The address in the addressed storage location is loaded into bytes 0 and 1 of the SDR. The addresses in the SAR and in the ADDRESS/DATA switches are compared. The ADDRESS COMPARE light comes on if the address compare conditions are met. (See LOAD/STORE ADDRESS COMPARE switch on page 1-060.)

(1)

X Gate SAR to A Bus (CS004)

True/Complement — DE975 DF975 DG975

X T0 + T1 Time Set A - B Reg (CC007)

Control Panel Switches — AP001

X T0 + T1 Time Set A-B Reg (CC007)

X Gate Y Bus to B Reg (CS004)

A Register — DE975 DF975 DG975

B Register — DE002 DF002 DG002

I2B

(2)

X Gate Mem Byte to M Bus (CS005)

X Set SDR Byte (CS007)

SDR — DN001

A

To Next Page

ALU — DE974 DF974 DG974

Z Register — DE974 DF974 DG974

X Set DR 2 (CS007)

Instruction	Operation
BAL	Compare

See page 6-100.

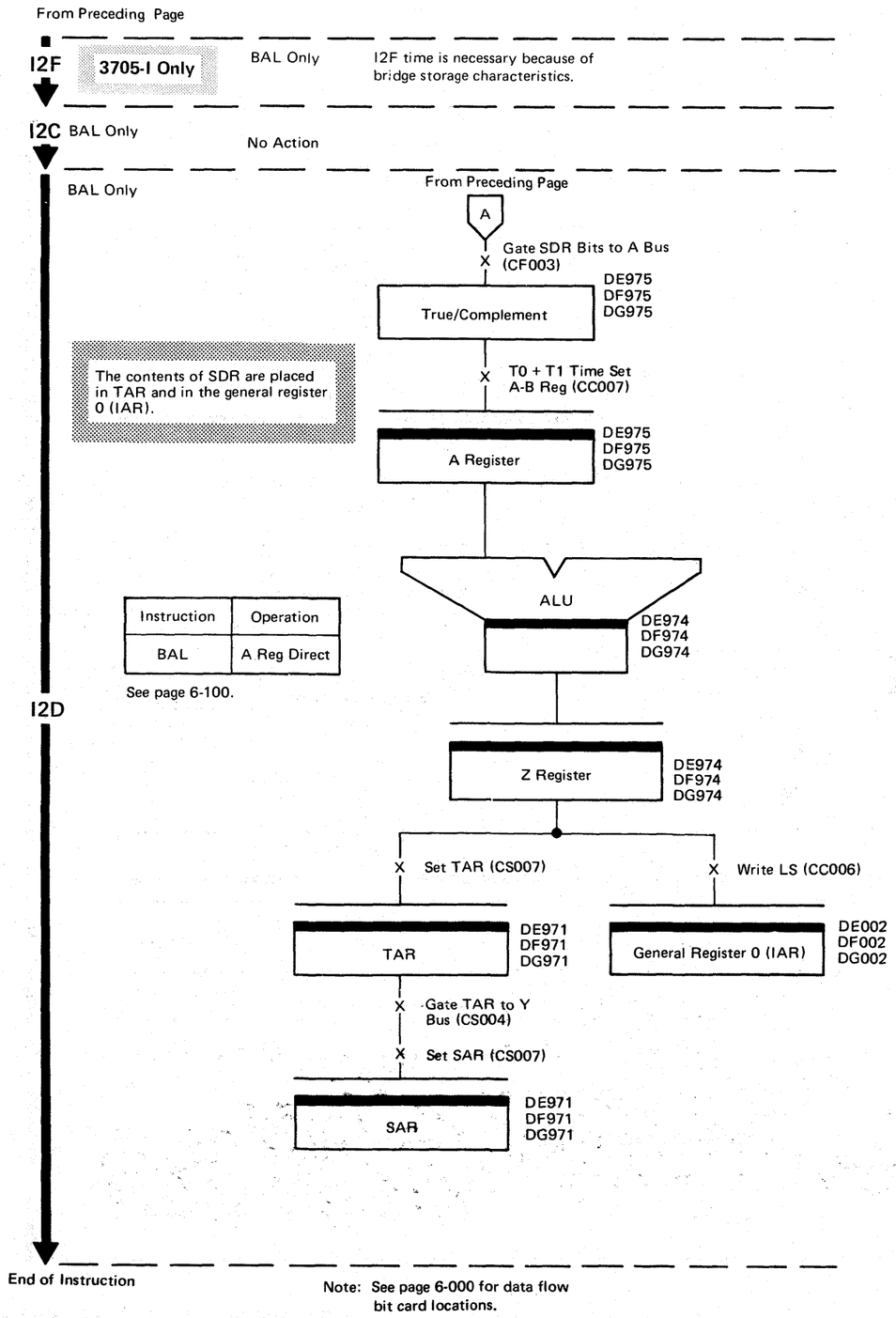
Display Register 2 — DE003 DF003 DG003

X Gate Displ Reg 2 to Ind (CU001)

Display B — AP011 AP012

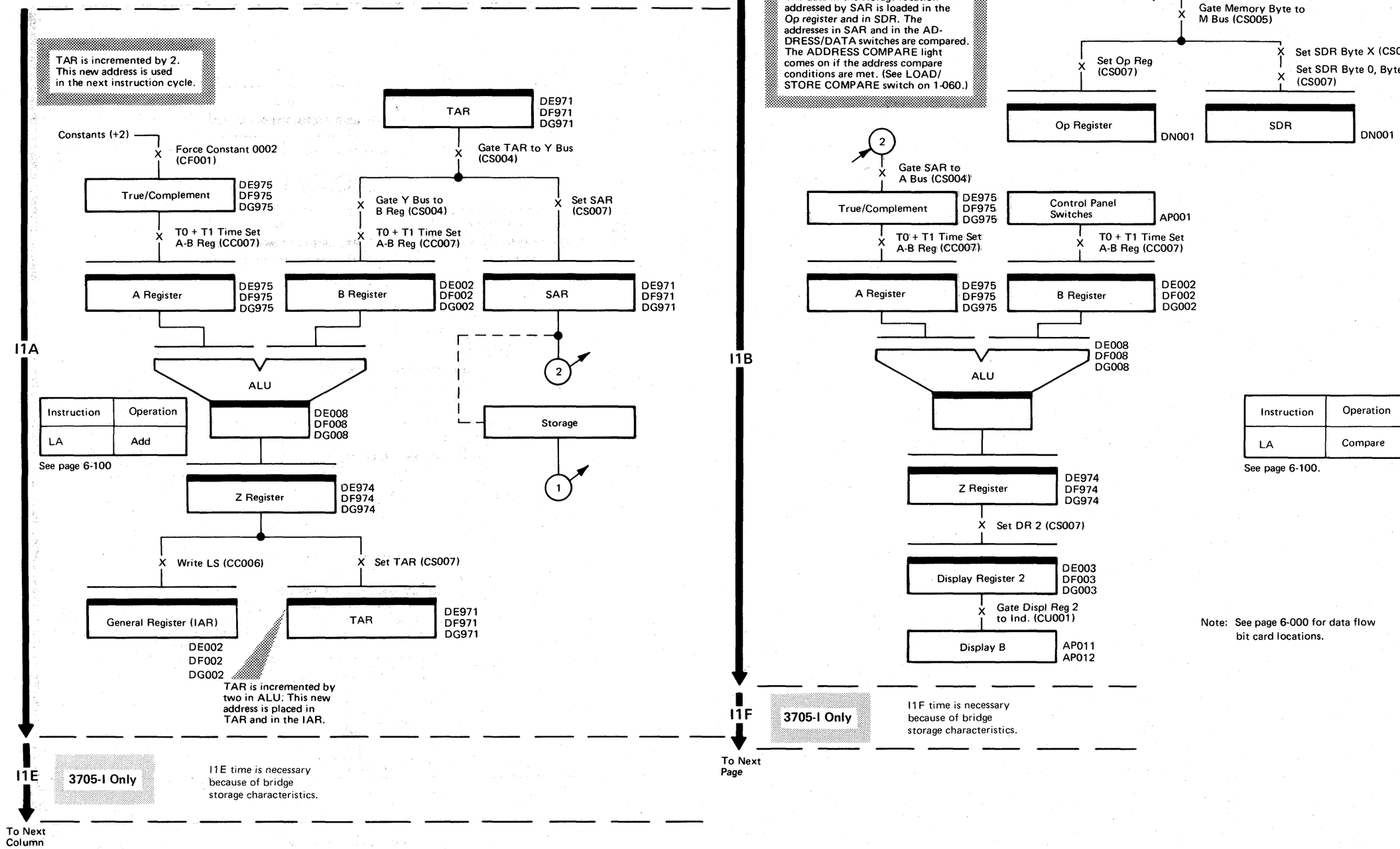
To Next Page

Note: See page 6-000 for data flow bit card locations.



Note: See page 6-000 for data flow bit card locations.

LA INSTRUCTION OPERATION



Note: See page 6-000 for data flow bit card locations.

From Preceding Page

LA Only

I1C

The address in SAR is loaded into LAR.

SAR — DE971 DF971 DG971

X Set LAR (CS001)

LAR — DE002 DF002 DG002

LA only

I1D

The address in TAR is loaded into SAR.

TAR — DE971 DF971 DG971

X Gate TAR to Y Bus (CS004)

X Set SAR (CS007)

SAR — DE971 DF971 DG971

(1)

LA Only

I2A

The address in TAR incremented by 2 and placed in IAR and in TAR. A storage fetch operation fetches the second halfword of the LA instruction.

Constant (+2)

X Force Constant 0002 (CF001)

True/ Complement — DE975 DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DE975 DF975 DG975

TAR — DE971 DF971 DG971

X Gate TAR to Y Bus (CS004)

X Gate Y Bus to B Reg (CS004)

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DE002 DF002 DG002

ALU — DE974 DF974 DG974

Instruction	Operation
LA	Add

See page 6-100

(1) Storage

Z Register — DE974 DF974 DG974

(2)

X Set TAR (CS007)

TAR — DE971 DF971 DG971

X Write LS (CC006)

General Register (IAR) — DE002 DF002 DG002

To Next Column

I1E

3705-I Only

LA Only

I2E time is necessary because of bridge storage characteristics.

LA Only

I2B

The address in the addressed storage location is loaded into bytes 0 and 1 of the SDR. The addresses in the SAR and in the ADDRESS/DATA switches are compared. The ADDRESS COMPARE light comes on if the address compare conditions are met. (See LOAD/ STORE ADDRESS COMPARE switch on page 1-060.

(1)

X Gate SAR to A Bus (CS004)

True/Complement — DE975 DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DE975 DF975 DG975

Control Panel Switches — AP001

X T0 + T1 Time A-B Reg

X Gate Y Bus Reg (CS00

B Register — DE002 DF002 DG002

ALU — DE974 DF974 DG974

Instruction	Operation
LA	Compare

See page 6-100.

(2)

X Gate Mem Byte to M Bus (CS005)

X Set SDR Byte (CS007)

SDR — DN001

A

To Next Page

Z Register — DE974 DF974 DG974

X Set DR2 (CS007)

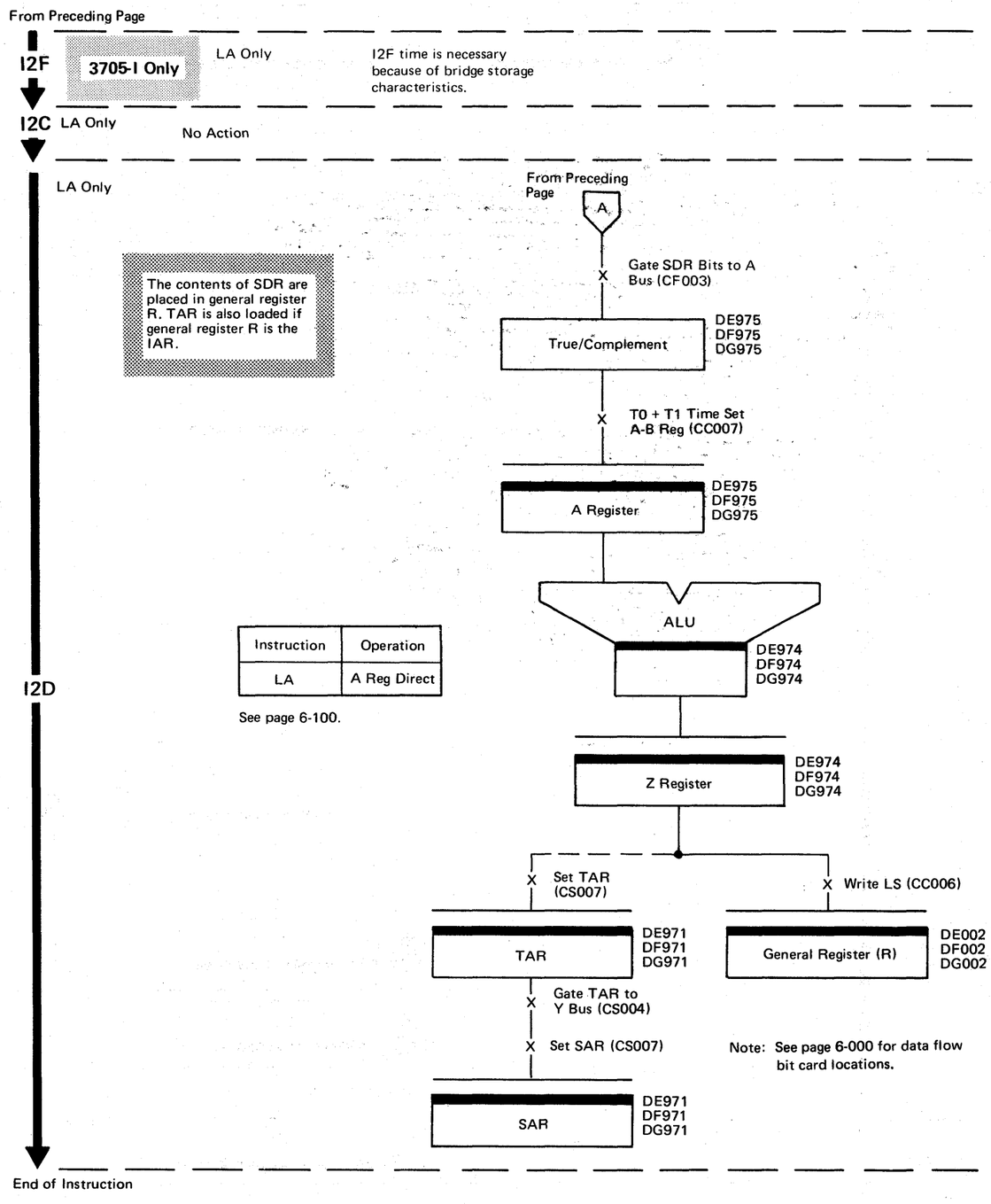
Display Register 2 — DE003 DF003 DG003

X Gate Displ Reg 2 to Ind (CU001)

Display B — AP011 AP012

To Next Page

Note: See page 6-000 for data flow bit card locations.


From Preceding Page
I2F
3705-I Only
LA Only
I2F time is necessary because of bridge storage characteristics.
I2C
LA Only
No Action
LA Only
The contents of SDR are placed in general register R. TAR is also loaded if general register R is the IAR.
From Preceding Page
A
X
Gate SDR Bits to A Bus (CF003)
True/Complement
DE975
DF975
DG975
X
T0 + T1 Time Set A-B Reg (CC007)
A Register
DE975
DF975
DG975
ALU
DE974
DF974
DG974
Z Register
DE974
DF974
DG974
X
Set TAR (CS007)
X
Write LS (CC006)
TAR
DE971
DF971
DG971
General Register (R)
DE002
DF002
DG002
X
Gate TAR to Y Bus (CS004)
X
Set SAR (CS007)
SAR
DE971
DF971
DG971
Note: See page 6-000 for data flow bit card locations.
I2D
Instruction
Operation
LA
A Reg Direct
See page 6-100.
End of Instruction

REGISTER BRANCH OR REGISTER AND BRANCH (RT) INSTRUCTIONS

The CCU takes on 11 cycle to execute any one of the five register branch, or register and branch instructions.

BRANCH DISPLACEMENT CALCULATIONS

The displacement in halfwords can be calculated as shown below (multiply by 2 for displacement in bytes):

If * = 0, Displacement halfwords = 1 + T
If * = 1, Displacement halfwords = 1 - T

Example: A800 is a NO OP.
A803 is a branch to itself indefinitely.

BRANCH (B)

0	1	2	3	4	5-14	15
1	0	1	0	1	T	*

*0 = + displacement
1 = - displacement

The displacement in the T field is added to the address in general register 0 (IAR) to form a "branch to" address. The displacement specified by the T field can be -1023 to +1023 halfwords. Bit 15 determines whether the displacement is positive or negative. An unconditional branch to the "branch to" address occurs.

The 'C' and 'Z' latches are not changed.

Note: Since register 0 is incremented before the instruction is executed, the displacement is with respect to the address of the next sequential instruction. Therefore, the displacement from the B instruction is -1022 to +1024 halfwords.

BRANCH ON BIT (BB)

0	1	2	3	4	5-6	7	8	9-14	15
1	1	M	M	1	R	N	M	T	*

*0 = + displacement
1 = - displacement

General Register = (2xR) + 1

The displacement in the T field is added to the address in general register 0 (IAR) to form a "branch to" address. The displacement specified by the T field can be -63 to +63 halfwords. Bit 15 determines whether the displacement is positive or negative. An unconditional branch to the "branch to" address occurs.

The M field specifies a bit in byte 0 (N=0) or byte 1 (N=1) of the general register designated by the R field. This bit is tested. If the bit is 0, the next sequential instruction is executed; if the bit is 1, the next instruction to be executed is at the "branch to" address.

The 'C' and 'Z' latches are not changed.

Note: Since register 0 is incremented before the instruction is executed, the displacement is with respect to the address of the next sequential instruction after the BB instruction. Therefore, the displacement from the BB instruction is -62 to +64 halfwords.

M field and N field decode

Bit to Be Tested	Instruction N 7	Instruction MMM—field 2 3 8—bit
0.0	0	0 0 0
1	0	0 0 1
2	0	0 1 0
3	0	0 1 1
4	0	1 0 0
5	0	1 0 1
6	0	1 1 0
7	0	1 1 1
1.0	1	0 0 0
1	1	0 0 1
2	1	0 1 0
3	1	0 1 1
4	1	1 0 0
5	1	1 0 1
6	1	1 1 0
7	1	1 1 1

BRANCH ON C LATCH (BCL)

0	1	2	3	4	5-14	15
1	0	0	1	1	T	*

*0 = + displacement
1 = - displacement

The displacement in the T field is added to the address in general register 0 (IAR) to form a "branch to" address. The displacement specified by the T field can be -1023 to +1023 halfwords. Bit 15 determines whether the displacement is positive or negative.

The 'C' latch is tested. If it is not set, the next sequential instruction is executed. If it is set, the next instruction to be executed is at the "branch to" address.

The 'C' and 'Z' latches are not changed.

Note: Since register 0 (IAR) is incremented before the instruction is executed, the displacement is with respect to the next sequential instruction after the BCL instruction. Therefore, the displacement from the BCL instruction is -1022 to +1024 halfwords.

BRANCH ON COUNT (BCT)

0	1	2	3	4	5-6	7	8	9-14	15
1	0	1	1	1	R	N	1	T	*

*0 = + displacement
1 = - displacement

General Register = (2xR) + 1

The displacement in the T field is added to the address in general register 0 (IAR) to form a "branch to" address. The displacement specified by the T field can be -63 to +63 halfwords. Bit 15 determines whether the displacement is positive or negative.

The count contained in byte 0 (N = 0) or bytes 0 and 1 (N=1) of the general register designated by the R field is decremented by 1 and then is tested. If the result is 0, the next sequential instruction is executed. If the result is not 0, the next instruction to be executed is at the "branch to" address.

If the byte count is X'00' or the halfword count is X'0000' before execution of this instruction, then the effective count value is 256 or 65,536, respectively.

The 'C' and 'Z' latches are not changed when this instruction is executed.

Note: Since register 0 (IAR) is incremented before the instruction is executed, the displacement is with respect to the next sequential instruction after the BCT instruction. Therefore, the displacement from the BCT instruction is -62 to +64 halfwords.

BRANCH ON Z LATCH (BZL)

0	1	2	3	4	5-14	15
1	0	0	0	1	T	*

*0 = + displacement
1 = - displacement

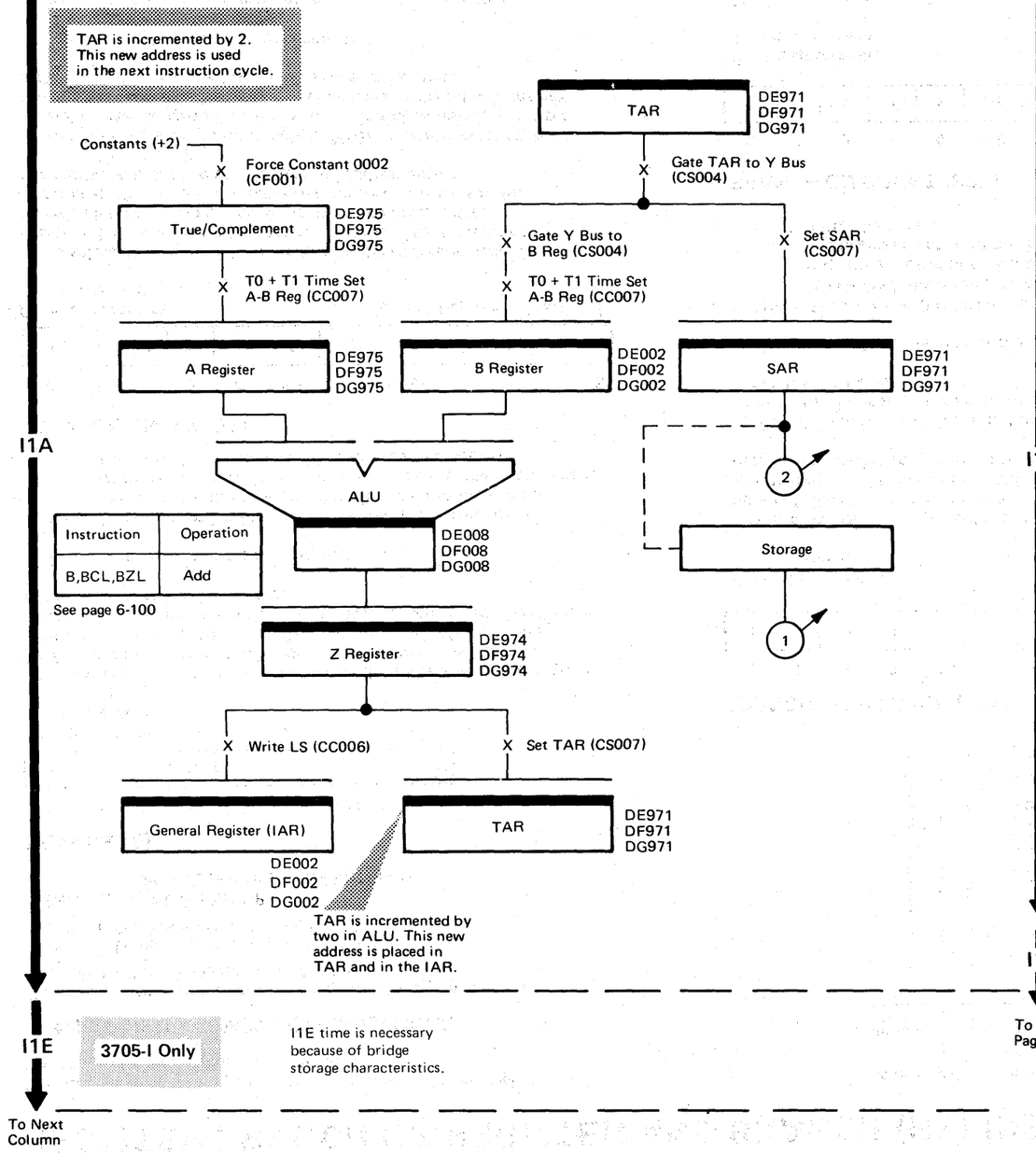
The displacement in the T field is added to the address in general register 0 (IAR) to form a "branch to" address. The displacement specified by the T field can be -1023 to +1023 halfwords. Bit 15 determines whether the displacement is positive or negative.

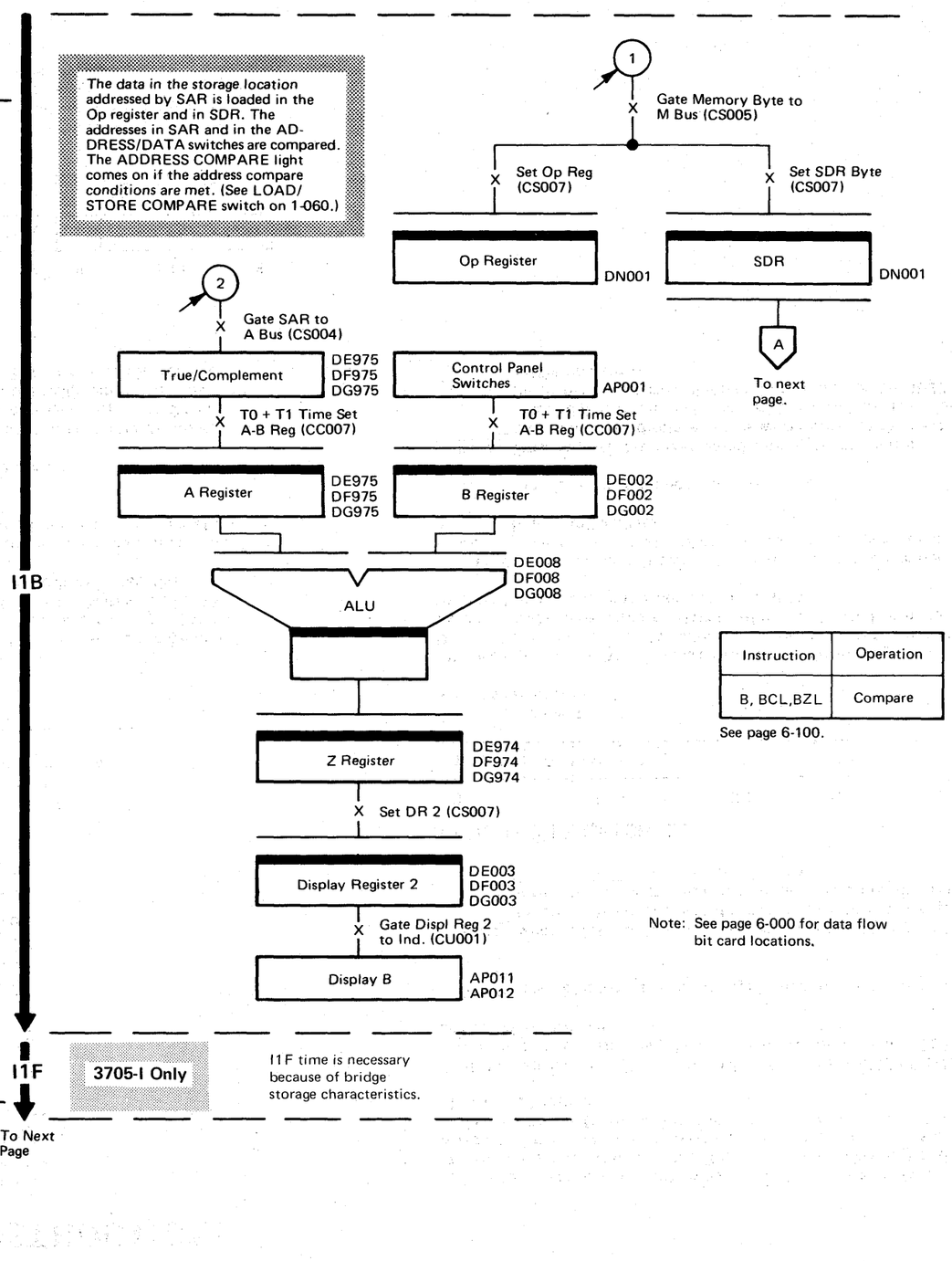
The 'Z' condition latch is tested. If not set, the next sequential instruction is executed. If set, the next instruction to be executed is at the "branch to" address

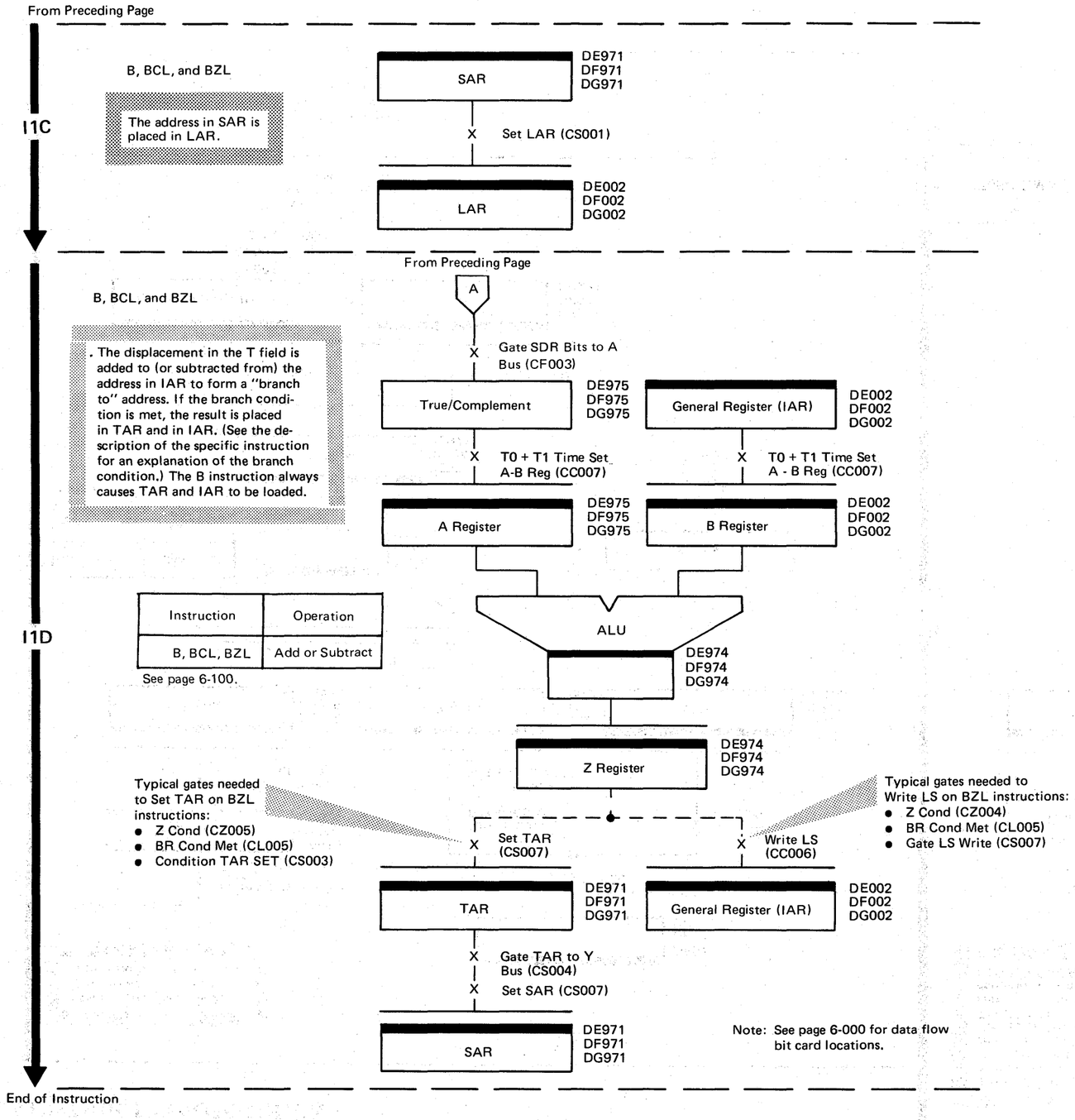
The 'C' and 'Z' latches are not changed.

Note: Since register 0 is incremented before the instruction is executed, the displacement is with respect to the next sequential instruction after the BZL instruction. Therefore, the displacement from the BZL instruction can be -1022 to +1024 halfwords.

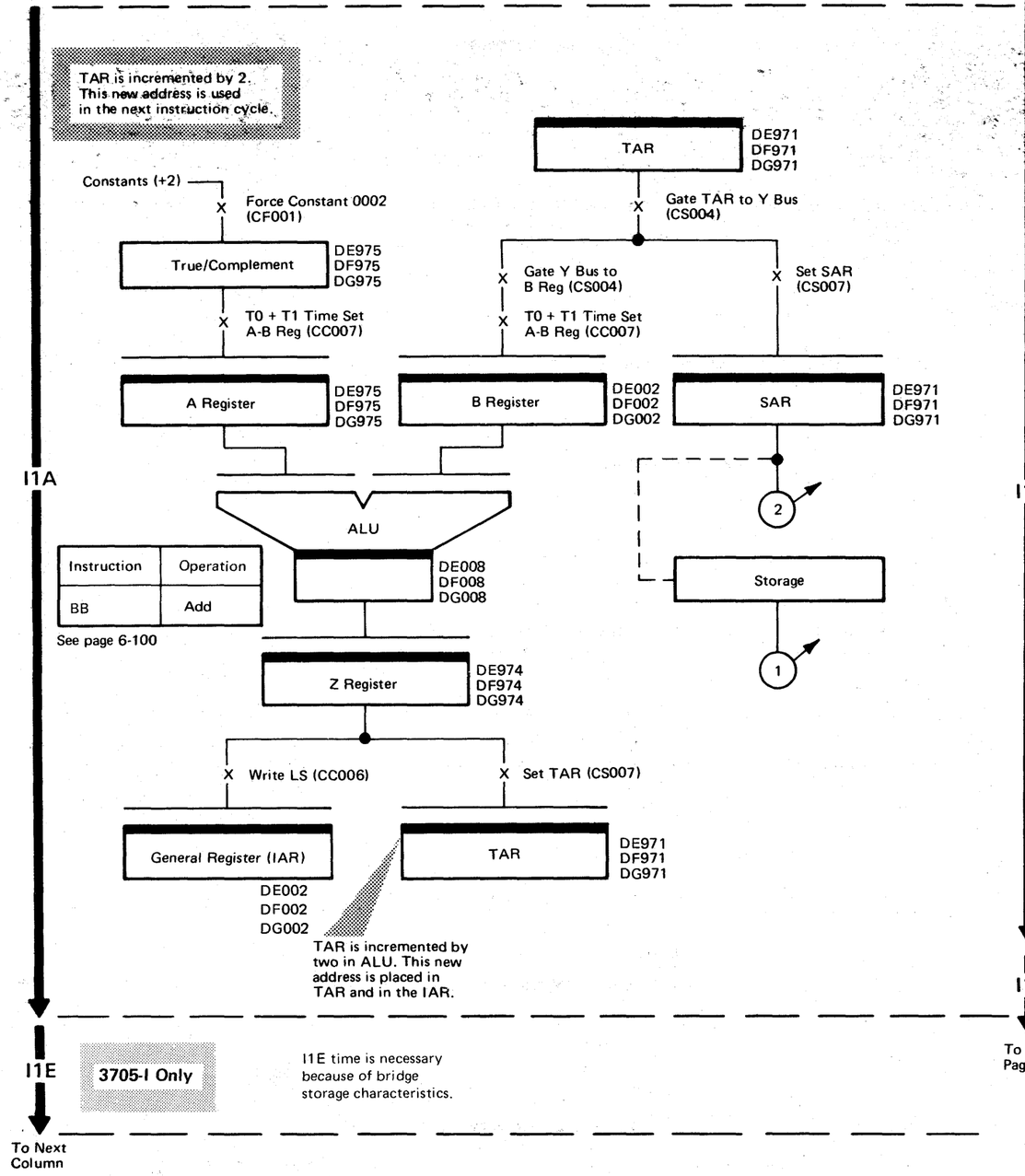
B, BCL, AND BZL INSTRUCTION OPERATION

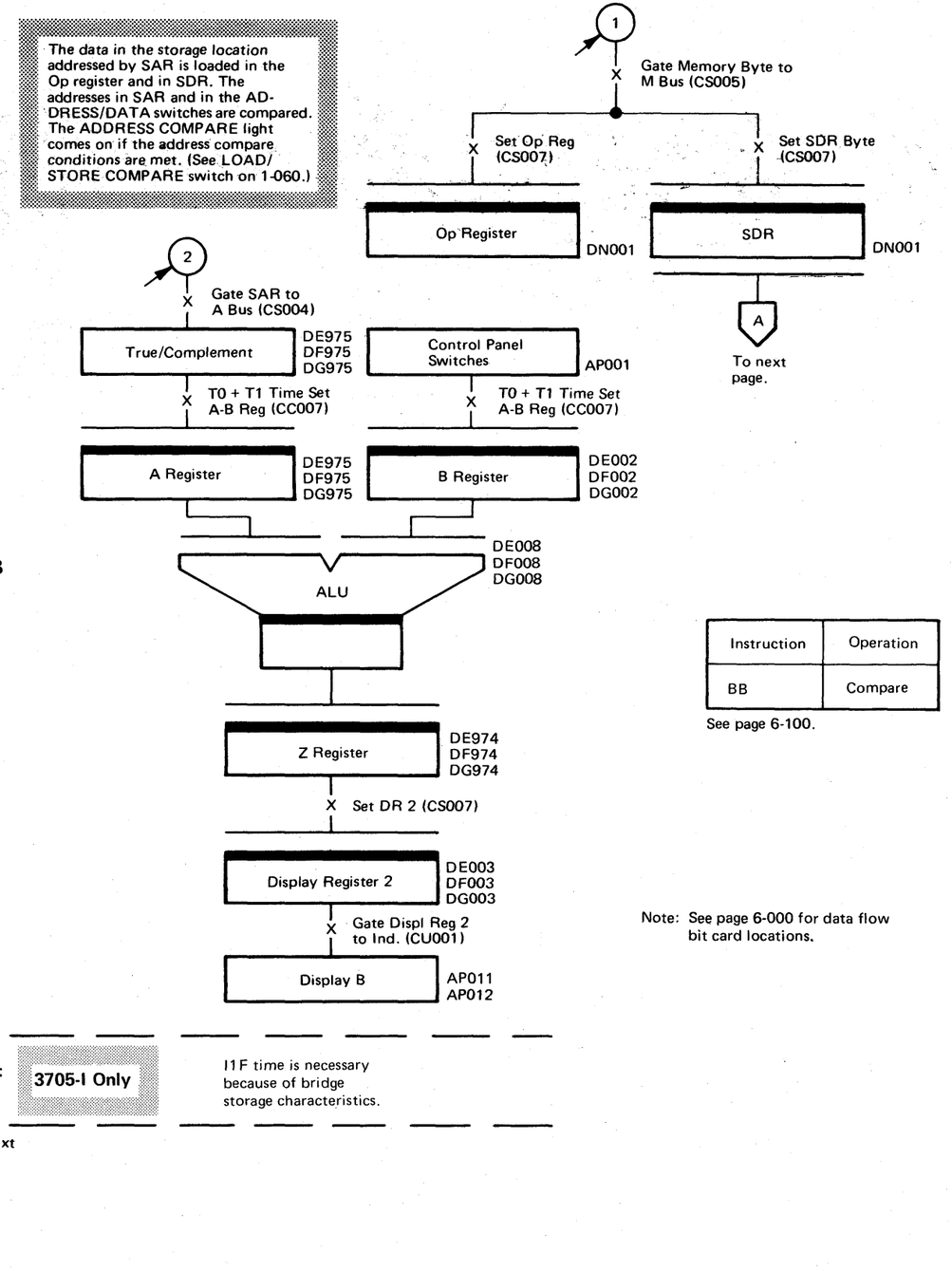





From Preceding Page
I1C
B, BCL, and BZL
The address in SAR is placed in LAR.
SAR
DE971
DF971
DG971
X Set LAR (CS001)
LAR
DE002
DF002
DG002
From Preceding Page
I1D
B, BCL, and BZL
. The displacement in the T field is added to (or subtracted from) the address in IAR to form a "branch to" address. If the branch condition is met, the result is placed in TAR and in IAR. (See the description of the specific instruction for an explanation of the branch condition.) The B instruction always causes TAR and IAR to be loaded.
A
X Gate SDR Bits to A Bus (CF003)
True/Complement
DE975
DF975
DG975
General Register (IAR)
DE002
DF002
DG002
X T0 + T1 Time Set A-B Reg (CC007)
X T0 + T1 Time Set A - B Reg (CC007)
A Register
DE975
DF975
DG975
B Register
DE002
DF002
DG002
ALU
DE974
DF974
DG974
Instruction
Operation
B, BCL, BZL
Add or Subtract
See page 6-100.
Z Register
DE974
DF974
DG974
Typical gates needed to Set TAR on BZL instructions:
• Z Cond (CZ005)
• BR Cond Met (CL005)
• Condition TAR SET (CS003)
X Set TAR (CS007)
X Write LS (CC006)
Typical gates needed to Write LS on BZL instructions:
• Z Cond (CZ004)
• BR Cond Met (CL005)
• Gate LS Write (CS007)
TAR
DE971
DF971
DG971
General Register (IAR)
DE002
DF002
DG002
X Gate TAR to Y Bus (CS004)
X Set SAR (CS007)
SAR
DE971
DF971
DG971
Note: See page 6-000 for data flow bit card locations.
End of Instruction

BB INSTRUCTION OPERATION





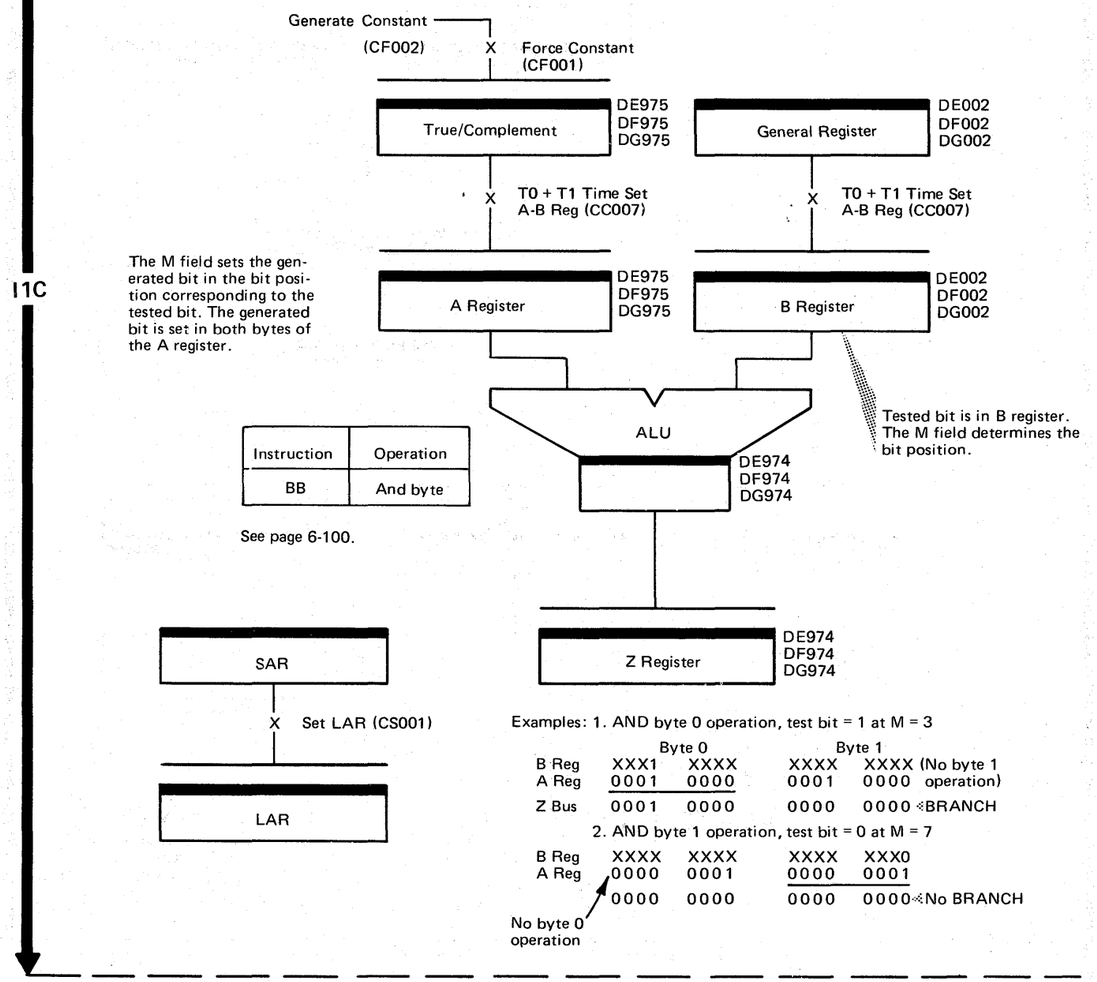
Note: See page 6-000 for data flow bit card locations.

From Preceding Page

BB only

A one is forced in the bit position (determined by the M field of the Op reg) of both byte 0 and byte 1 of the A reg. The general register content (includes the bit to be tested) is placed in the B reg. ALU performs an 'AND byte 0' or 'AND byte 1' operation (determined by the N field). Test results:

- If the Z bus byte 0 or 1 contains a one, gate the branch to address to TAR and IAR at I1D time.
- If the Z bus byte 0 and 1 both contain zeros, inhibit gating the branch to address to TAR and IAR leaving the next sequential address in TAR and IAR.



I1C

The M field sets the generated bit in the bit position corresponding to the tested bit. The generated bit is set in both bytes of the A register.

Instruction	Operation
BB	And byte

See page 6-100.

Tested bit is in B register. The M field determines the bit position.

Examples: 1. AND byte 0 operation, test bit = 1 at M = 3

	Byte 0		Byte 1	
B Reg	XXX1	XXXX	XXXX	XXXX (No byte 1
A Reg	0001	0000	0001	0000 operation)
Z Bus	0001	0000	0000	0000 ⇐BRANCH

2. AND byte 1 operation, test bit = 0 at M = 7

B Reg	XXXX	XXXX	XXXX	XXX0
A Reg	0000	0001	0000	0001
	0000	0000	0000	0000 ⇐No BRANCH

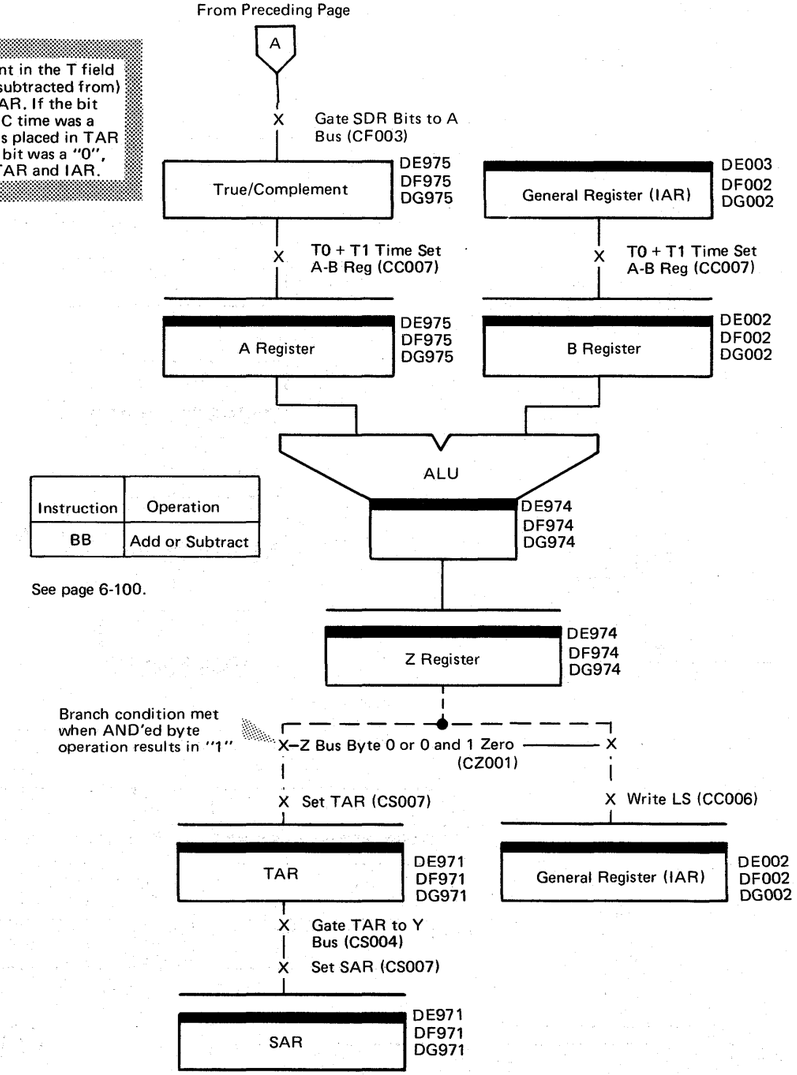
No byte 0 operation

To Next Column

BB only

The displacement in the T field is added to (or subtracted from) the address in IAR. If the bit tested during I1C time was a "1", the result is placed in TAR and IAR. If the bit was a "0", inhibit setting TAR and IAR.

From Preceding Page



I1D

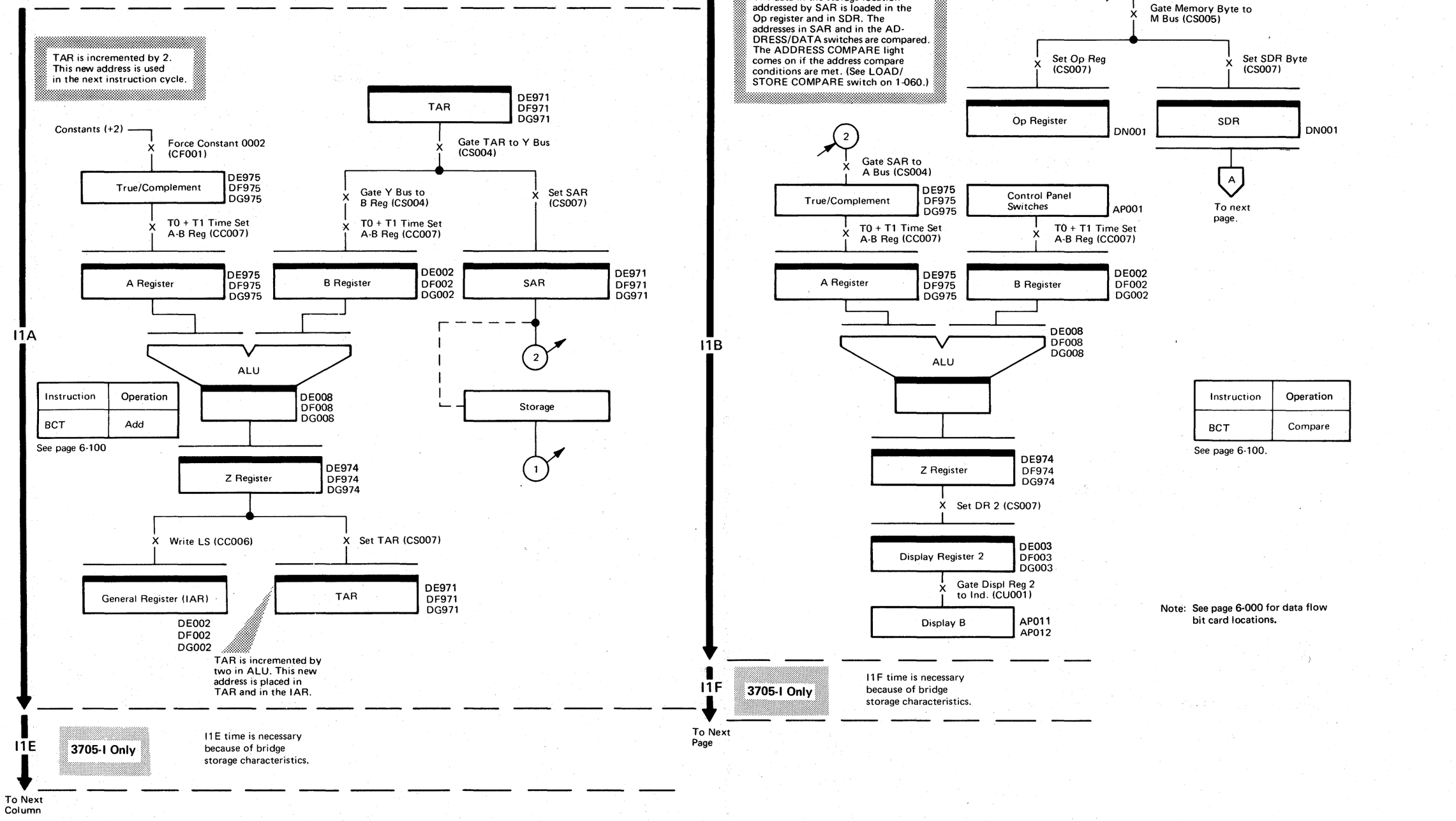
Instruction	Operation
BB	Add or Subtract

See page 6-100.

End of Instruction

Note: See page 6-000 for data flow bit card locations.

BCT INSTRUCTION OPERATION

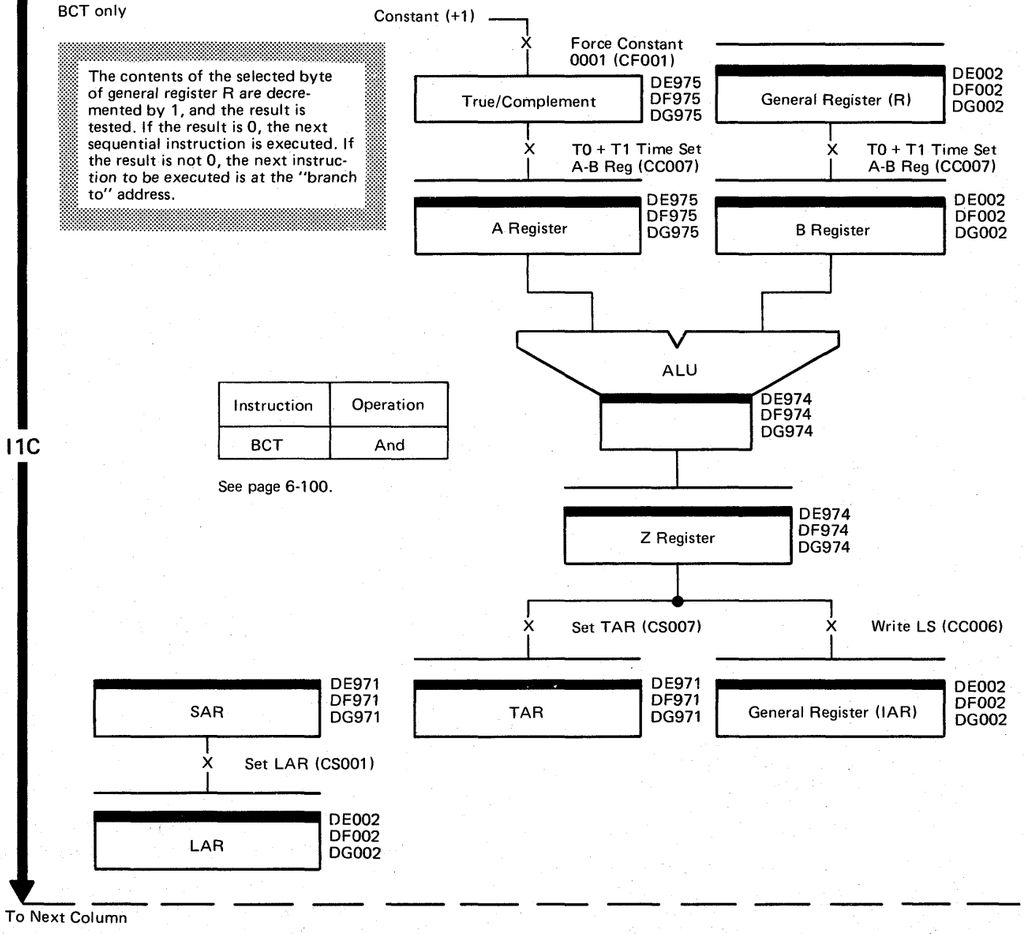


Note: See page 6-000 for data flow bit card locations.

From Preceding Page

BCT only

The contents of the selected byte of general register R are decremented by 1, and the result is tested. If the result is 0, the next sequential instruction is executed. If the result is not 0, the next instruction to be executed is at the "branch to" address.

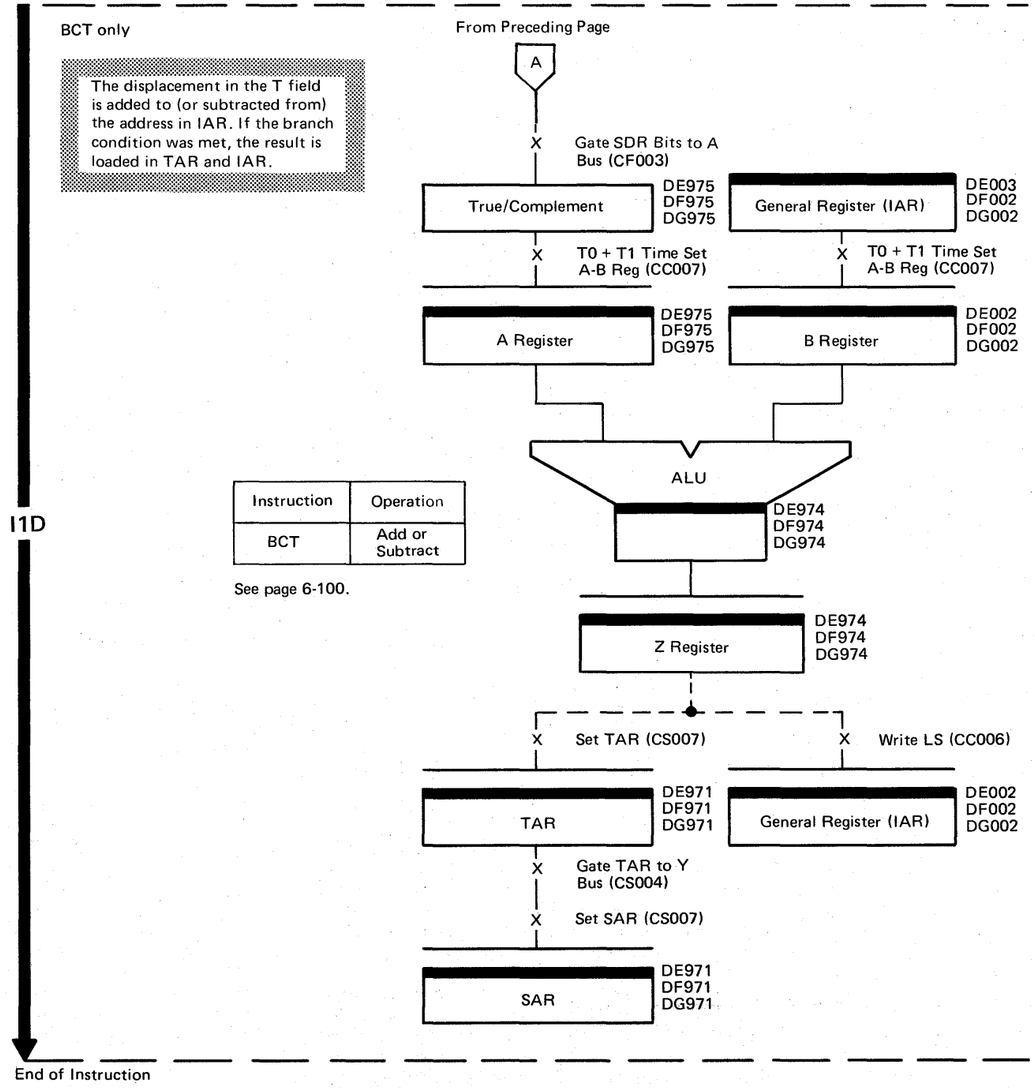


Instruction	Operation
BCT	And

See page 6-100.

BCT only

The displacement in the T field is added to (or subtracted from) the address in IAR. If the branch condition was met, the result is loaded in TAR and IAR.



Instruction	Operation
BCT	Add or Subtract

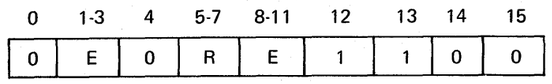
See page 6-100.

Note: See page 6-000 for data flow bit card locations.

REGISTER AND EXTERNAL REGISTER (RE) INSTRUCTIONS

An 'input' or 'output' or 'exit' instruction takes one 11 cycle for execution.

INPUT



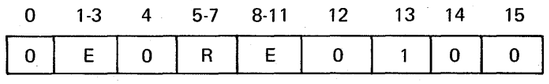
This instruction loads the general register specified by the R field with the contents of the external register specified by the E field. See 6-151 for the addresses of the 128 input-addressable external registers.

The 'C' and 'Z' latches are not changed when an 'input' instruction is executed.

An 'input' instruction can be executed at program level 1, 2, 3, or 4. An attempt to execute this instruction at program level 5 causes the L1 input/output check interrupt request to be set. The check is also set if the external register address is not assigned or is not recognized by any adapter. It is also set if incorrect parity is detected on the CCU inbus when an input instruction is executed.

Note: If register 0 (IAR) is specified as R, a branch to the effective address formed in register 0 occurs.

OUTPUT



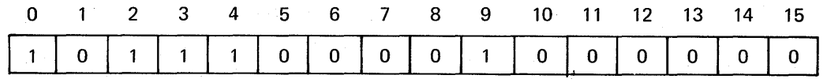
This instruction places the contents of the general register specified by the R field in the external register specified by the E field. The addresses of the 128 output-addressable registers are shown on 6-151.

The 'C' and 'Z' latches are not changed when an 'output' instruction is executed.

An 'output' instruction can be executed at program level 1, 2, 3, or 4. An attempt to execute this instruction at program level 5 causes the L1 input/output check interrupt request to set. The check also sets if the external register address is not assigned or is not recognized by any adapter. An output instruction executed at program level 2, 3, or 4, or level 1 during IPL phase 3 also causes the CRC data register in the CCU to be loaded with the contents of byte 1 of the register specified by R.

Note: If register 0 (IAR) is specified by E, a branch to the effective address formed in register 0 occurs. If register 0 is specified by R and one of the general registers is specified by E, the content of the general register is not changed, and parity is regenerated.

EXIT



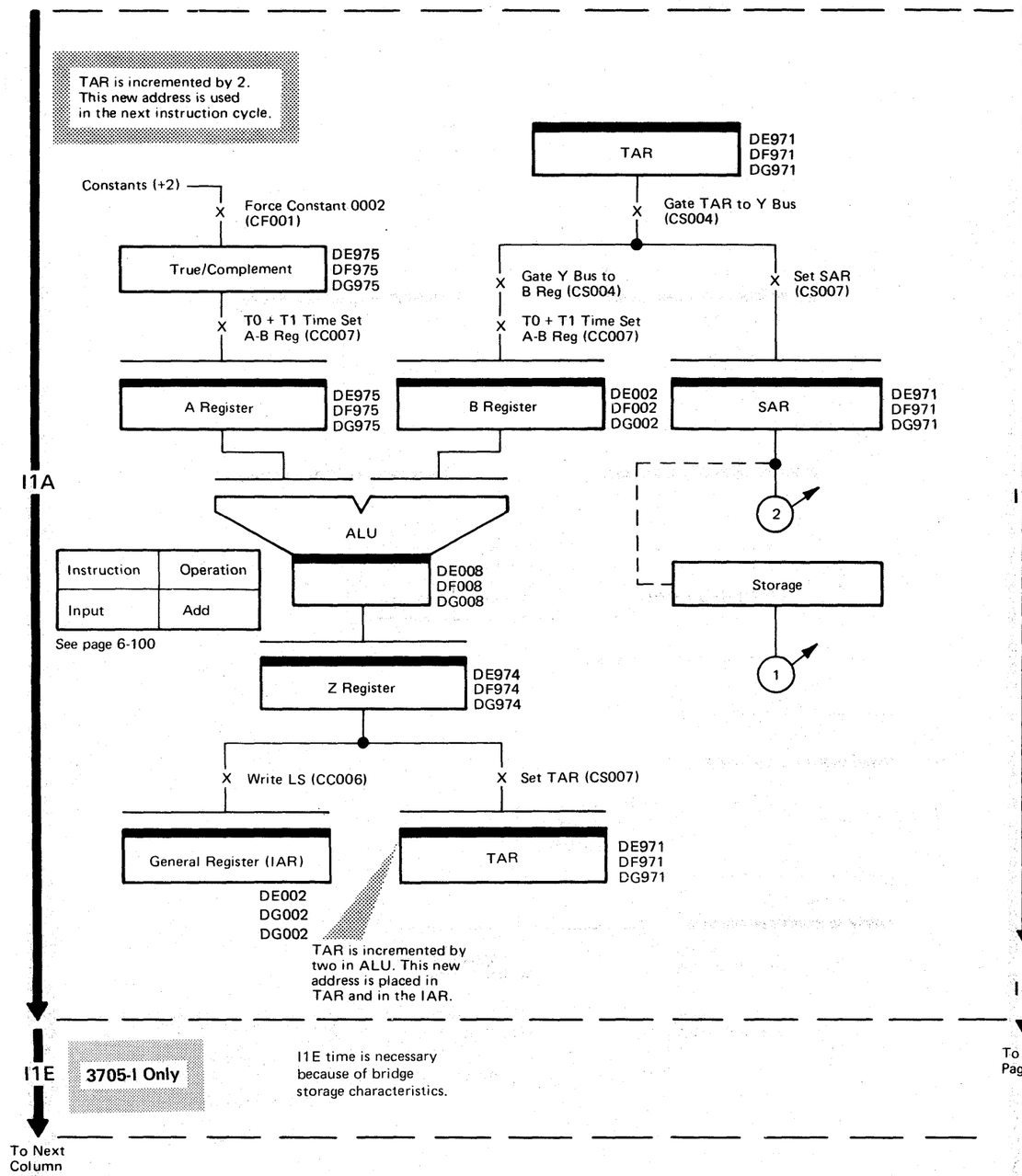
This instruction is used to leave any of the five program levels. When an 'exit' instruction is executed at a program level, the 'interrupt entered' latch for that program level is reset.

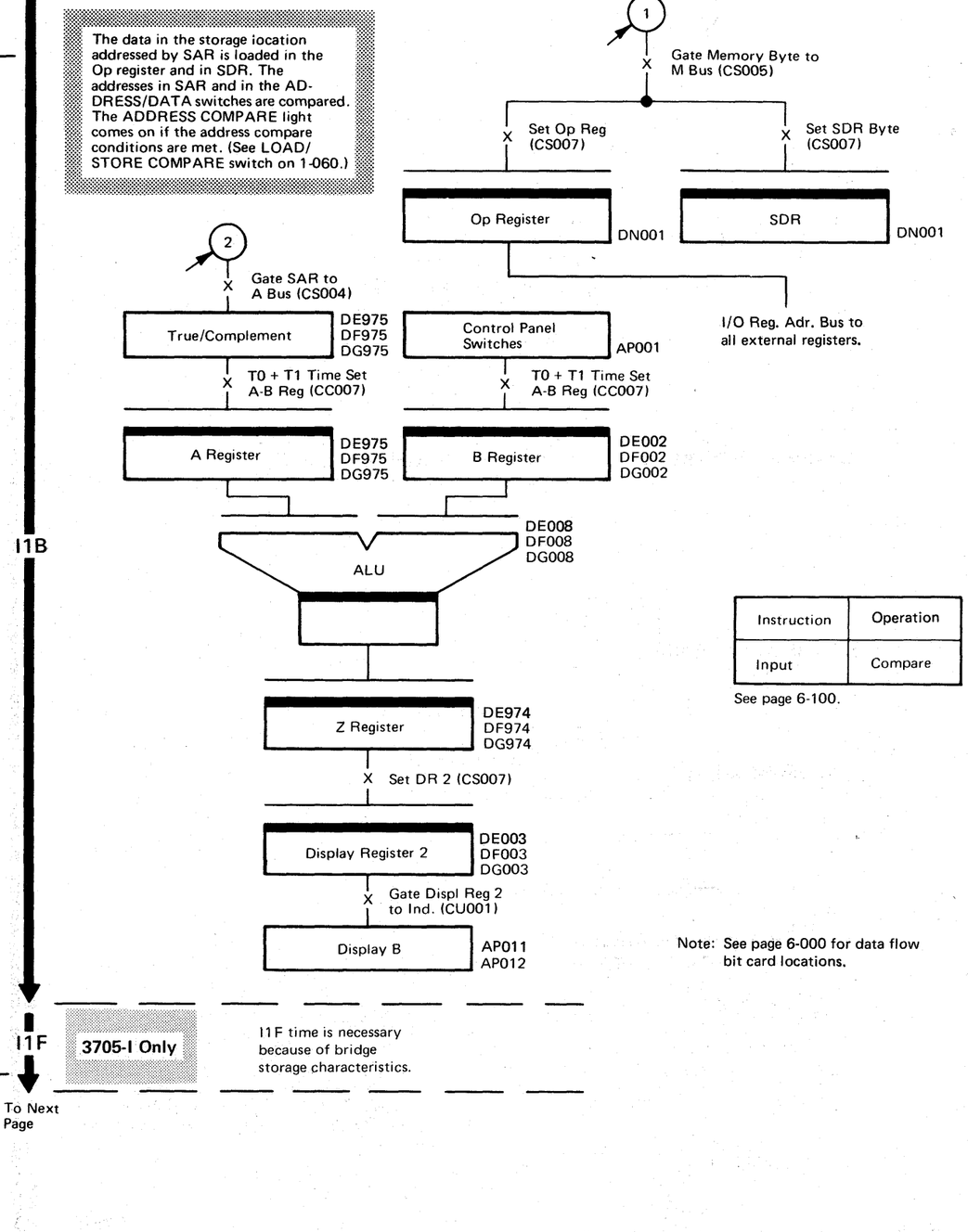
If 'exit' is executed at program level 5, the program level 4 supervisor interrupt request is set. If no other interrupt requests are present, the next instruction executed is the instruction at the starting address for program level 4. If other interrupt requests are present, the next instruction executed is the instruction at the starting address of the highest program level requested.

If level 5 is masked off and no interrupt requests are pending at any level, then an 'exit' instruction will cause the CCU to go into the "Wait" state (take idle cycles) until an interrupt occurs.

The 'C' and 'Z' latches are not changed.

INPUT INSTRUCTION OPERATION





From Preceding Page

Input Only

I1C

The contents of the register specified by the E field are placed in the SDR.

CCU External Registers

X Input Instruction (CD003)

X Gate CCU Indata to Y Bus (CS004)

Adapters

X Input Instruction (CD003)

X Gate Inbus to Y Bus (CS004)

General Register

X Gate Y Bus to B Reg (CS004)

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DE002 DF002 DG002

ALU — DE974 DF974 DG974

Instruction	Operation
Input	B Reg Direct

See page 6-100.

SAR

X Set LAR (CS001)

LAR

Z Register — DE974 DF974 DG974

X Gate Z Bus to M Bus (CS005)

X Set SDR Byte (CS007)

SDR — DN001

(1)

To Next Column

Input Only

I1D

The contents of the SDR are loaded into the general register specified by the R field. TAR is also loaded if this general register is IAR. The contents of TAR are loaded into SAR.

(1)

X Gate SDR Bits to A Bus (CF003)

True/Complement — DE975 DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DE975 DF975 DG975

ALU — DE974 DF974 DG974

Instruction	Operation
Input	A Reg Direct

See page 6-100.

Z Register — DE974 DF974 DG974

X Set TAR (CS007)

X Write LS (CC006)

TAR — DE971 DF971 DG971

General Register (R) — DE002 DF002 DG002

X Gate TAR to Y Bus (CS004)

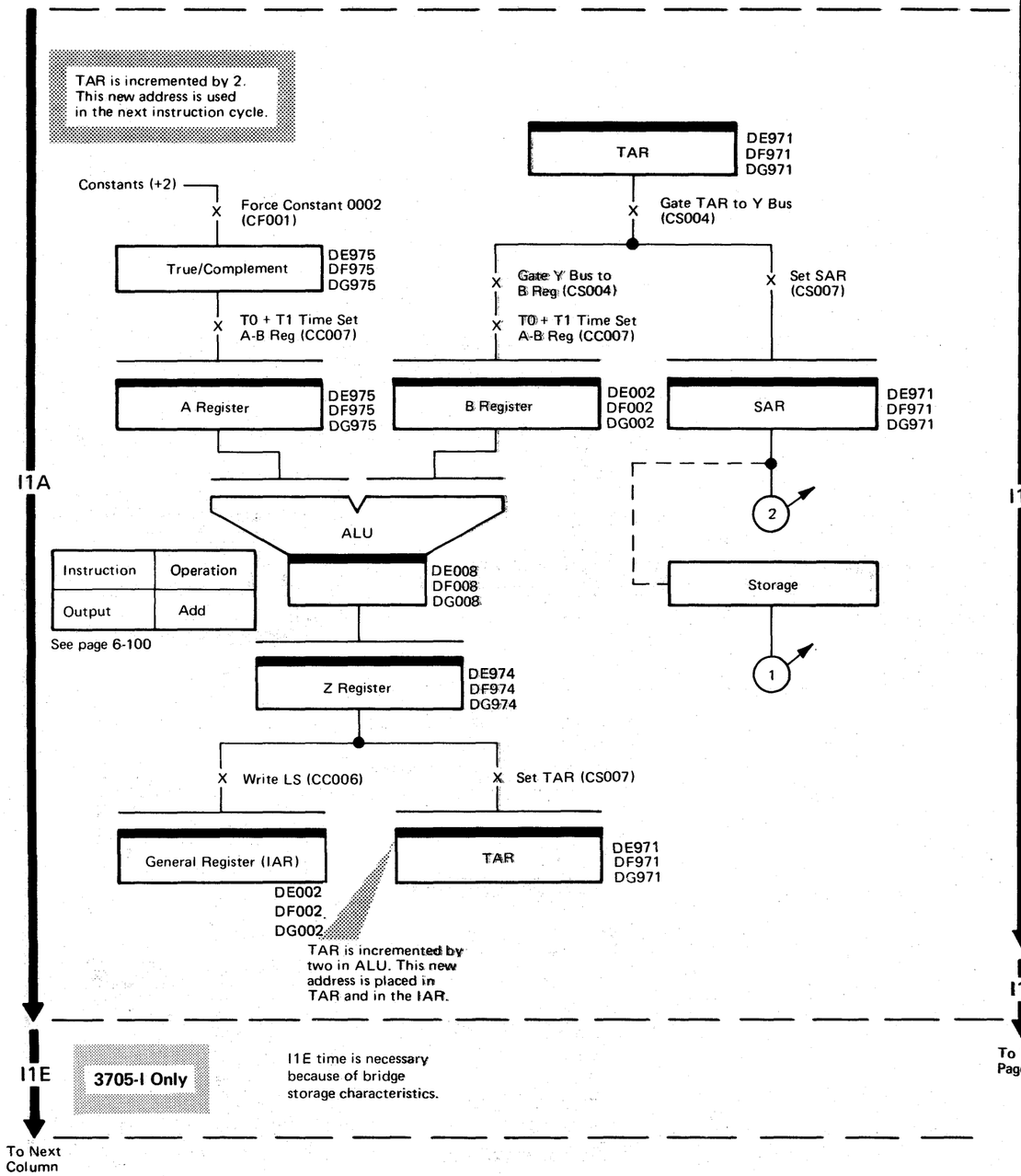
X Set SAR (CS007)

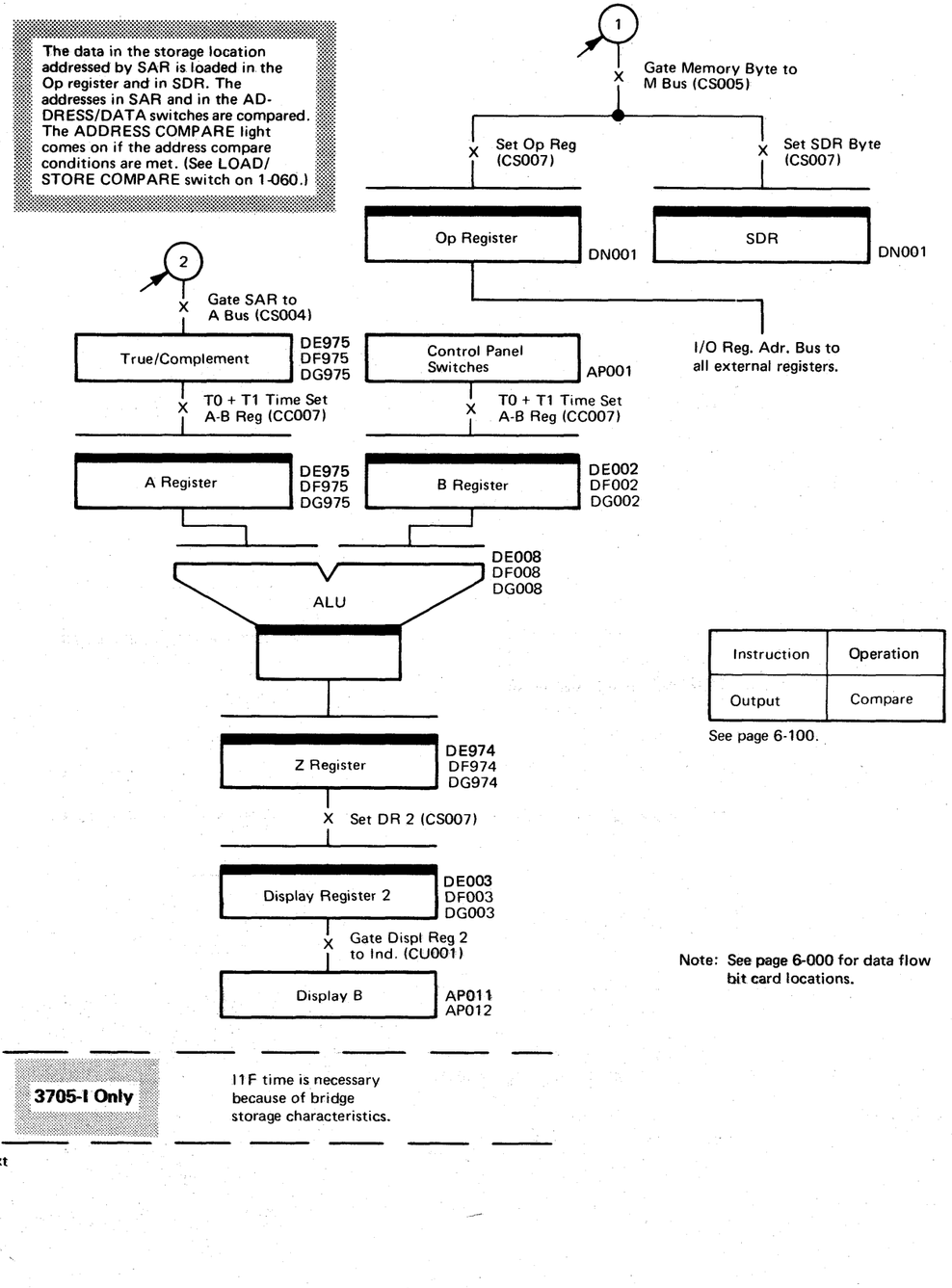
SAR — DE971 DF971 DG971

End of Instruction

Note: See page 6-000 for data flow bit card locations.

OUTPUT INSTRUCTION OPERATION





Note: See page 6-000 for data flow bit card locations.

From Preceding Page

Output Only

If the external register specified by E is not a general register, the contents of the general register specified by the R field are placed on the 'out bus' to the adapters. If the external register specified by E is a general register, the contents of the general register specified by R are loaded into SDR.

I1C

Instruction	Operation
Output	B Reg Direct

See page 6-100.

General Register (R) — DE002 DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DE002 DF002 DG002

ALU — DE974 DF974 DG974

Z Register — DE974 DF974 DG974

SAR — DE971 DF971 DG971

X Set LAR (CS001)

LAR — DE002 DF002 DG002

Outbus to Adapters

X Gate Z Bus to M Bus (CS005)

X Set SDR Byte (CS007)

SDR — DN001

X CCU Sample Output Data (CQ001)

1.0 1.7

Q Register (CRC Data Register)

(1)

Note 1: The line Output Inst (CD003) generates the line CCU Sample Output Data (CQ001) which is active during CD time.

Note 2: The line CCU Sample Output Data causes the contents of the Z Register byte 1 to be set in the CRC data register.

To Next Column

Output Only

The contents of SDR are loaded into external register E, if external register E is a general register. If external register E is the IAR, the contents of SDR are loaded into TAR also. If external register E is not a general register, the data from the 'out bus' is loaded into external register E. In any case, the contents of TAR are loaded into SAR.

I1D

Instruction	Operation
Output	A Reg Direct

See page 6-100.

TAR — DE971 DF971 DG971

X Gate TAR to Y Bus (CS004)

X Set SAR (CS007)

SAR — DE971 DF971 DG971

(1)

X Gate SDR Bits to A Bus (CF003)

True/Complement — DE975 DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DE975 DF975 DG975

ALU — DE974 DF974 DG974

Z Register — DE974 DF974 DG974

X Write LS (CC006)

General Register (E) — DE002 DF002 DG002

End of Instruction

Note: See page 6-000 for data flow bit card locations.

EXIT INSTRUCTION OPERATION

TAR is incremented by 2. This new address is used in the next instruction cycle.

TAR — DE971 DF971 DG971

Constants (+2) → X Force Constant 0002 (CF001) → True/Complement — DE975 DF975 DG975 → X T0 + T1 Time Set A-B Reg (CC007) → A Register — DE975 DF975 DG975

TAR → X Gate TAR to Y Bus (CS004)

X Gate Y Bus to B Reg (CS004) → B Register — DE002 DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007) → B Register

X Set SAR (CS007) → SAR — DE971 DF971 DG971

A Register, B Register → ALU

ALU → DE008 DF008 DG008

Instruction	Operation
Exit	Add

See page 6-100

DE008 DF008 DG008 → Z Register — DE974 DF974 DG974

Z Register → X Write LS (CC006) → General Register (IAR) — DE002 DF002 DG002

Z Register → X Set TAR (CS007) → TAR — DE971 DF971 DG971

TAR is incremented by two in ALU. This new address is placed in TAR and in the IAR.

SAR → (2) → Storage → (1)

I1A

I1E — 3705-I Only

I1E time is necessary because of bridge storage characteristics.

To Next Column

I1B

The data in the storage location addressed by SAR is loaded in the Op register and in SDR. The addresses in SAR and in the ADDRESS/DATA switches are compared. The ADDRESS COMPARE light comes on if the address compare conditions are met. (See LOAD/STORE COMPARE switch on 1-060.)

(1) → X Gate Memory Byte to M Bus (CS005)

X Set Op Reg (CS007) → Op Register — DN001

X Set SDR Byte (CS007) → SDR — DN001

(2) → X Gate SAR to A Bus (CS004)

True/Complement — DE975 DF975 DG975 → X T0 + T1 Time Set A-B Reg (CC007) → A Register — DE975 DF975 DG975

Control Panel Switches — AP001 → X T0 + T1 Time Set A-B Reg (CC007) → B Register — DE002 DF002 DG002

A Register, B Register → ALU

ALU → DE008 DF008 DG008

DE008 DF008 DG008 → Z Register — DE974 DF974 DG974

Z Register → X Set DR 2 (CS007) → Display Register 2 — DE003 DF003 DG003

Display Register 2 → X Gate Displ Reg 2 to Ind. (CU001) → Display B — AP011 AP012

Instruction	Operation
Exit	Compare

See page 6-100.

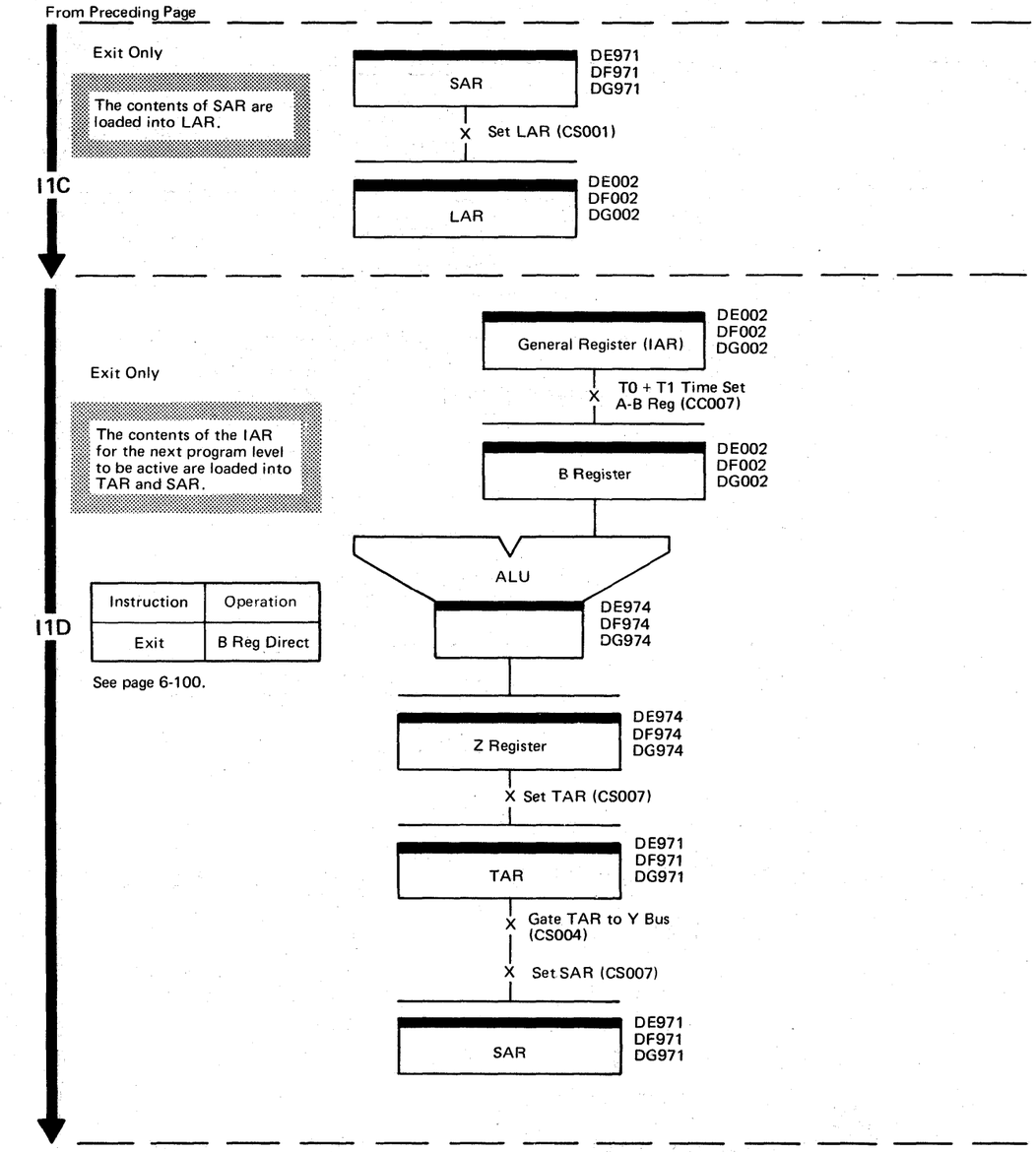
Note: See page 6-000 for data flow bit card locations.

I1F — 3705-I Only

I1F time is necessary because of bridge storage characteristics.

To Next Page

CCU



Note: See page 6-000 for data flow bit card locations.

CCU INPUT INSTRUCTIONS

The central control unit (CCU) has 44 assigned input instructions. These input instructions set bits in a general register to indicate various hardware conditions.

INPUTS X'00' TO X'1F' GENERAL REGISTERS

Inputs X'00'-X'1F' load the contents of the general register specified by the E field into the general register specified by the R field.

The contents of the general register specified by the E field are set in the B register at I1C time. Refer to the input instruction on page 6-710.

Storage Size	Bit Position 0.0	0.1	0.2	0.3
16K	0	0	0	1
48K	0	0	1	1
80K	0	1	0	1
112K	0	1	1	1
144K	1	0	0	1
176K	1	0	1	1
208K	1	1	0	1
240K	1	1	1	1

Note: The 16K BSM must be jumpered as the last logical BSM in the addressing scheme.

INPUT X'70' STORAGE SIZE INSTALLED

Input X'70' causes the general register specified by the R field to be loaded with a combination of bits that indicate the amount of storage installed.

GENERAL REGISTER BIT DEFINITIONS

3705-I (Bridge Storage)

0.0 A "1" indicates that the amount of storage installed in the 3705-I is either 144, 176, 208, or 240K.

0.1 A "1" indicates that the amount of storage installed in the 3705-I is either 80, 112, 208, or 240K.

0.2 A "1" indicates that the amount of storage installed in the 3705-I is either 48, 112, 176, or 240K.

0.3 A "1" indicates that the amount of storage installed in the 3705-I is either 16, 48, 80, 112, 144, 176, 208, or 240K.

0.4 These bits are 0. 1.7

0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7
General Register (In CCU)															

3705-II (FET Storage)

Storage Size	Bit Position 0.2	0.3	0.4	0.5	0.6
32K	0	0	0	0	1
64K	0	0	0	1	0
96K	0	0	0	1	1
128K	0	0	1	0	0
160K	0	0	1	0	1
192K	0	0	1	1	0
224K	0	0	1	1	1
256K	0	1	0	0	0
320K	0	1	0	1	0
384K	0	1	1	0	0
448K	0	1	1	1	0
512K	1	0	0	0	0

0.2 A "1" indicates that the amount of storage installed in the 3705-11 is 512K.

0.3 A "1" indicates that the amount of storage installed in the 3705-II is 256, 320, 384, or 448K.

0.4 A "1" indicates that the amount of storage installed in the 3705-II is either 128K, 160K, 192K, 224, 384, or 448K.

0.5 A "1" indicates that the amount of storage installed in the 3705-II is either 64K, 96K, 192K, 224, 320, or 448K.

0.6 A "1" indicates that the amount of storage installed in the 3705-II is either 32K, 96K, 160K, or 224K.

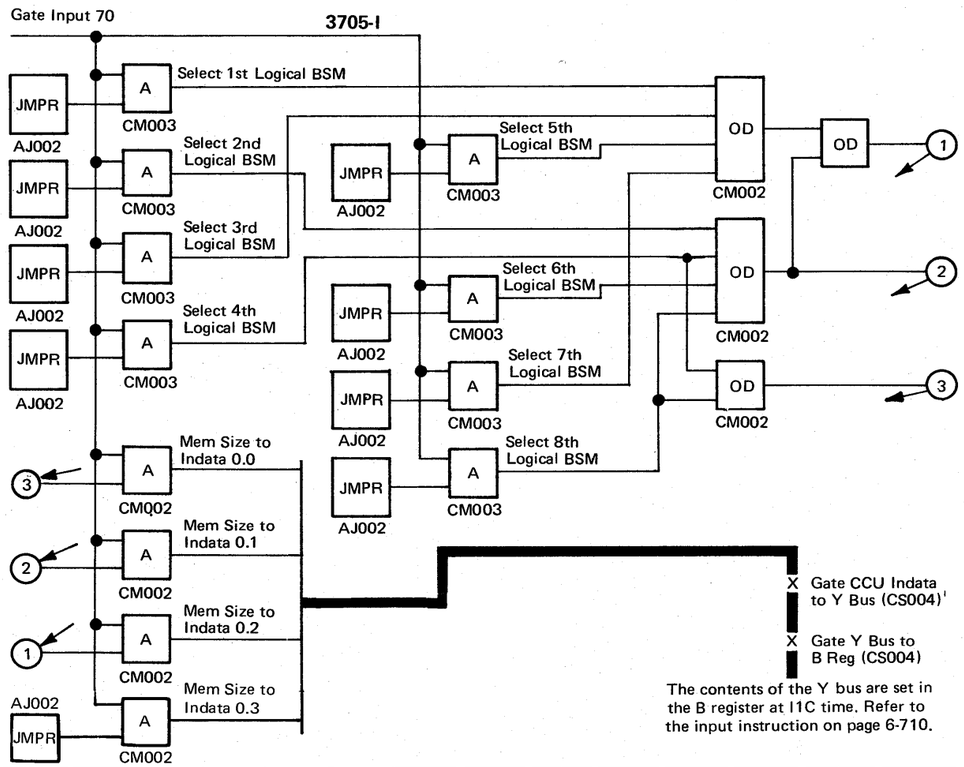
These bits are 0. 0.0 0.1

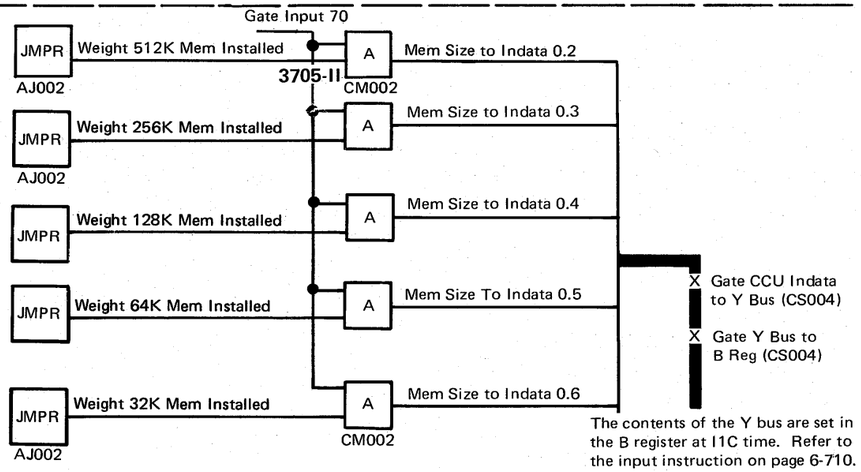
0.7 These bits are 0. 1.6

A "1" indicates that 20-bit addressing is installed.

0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7
General Register (In CCU)															

HARDWARE FUNCTION

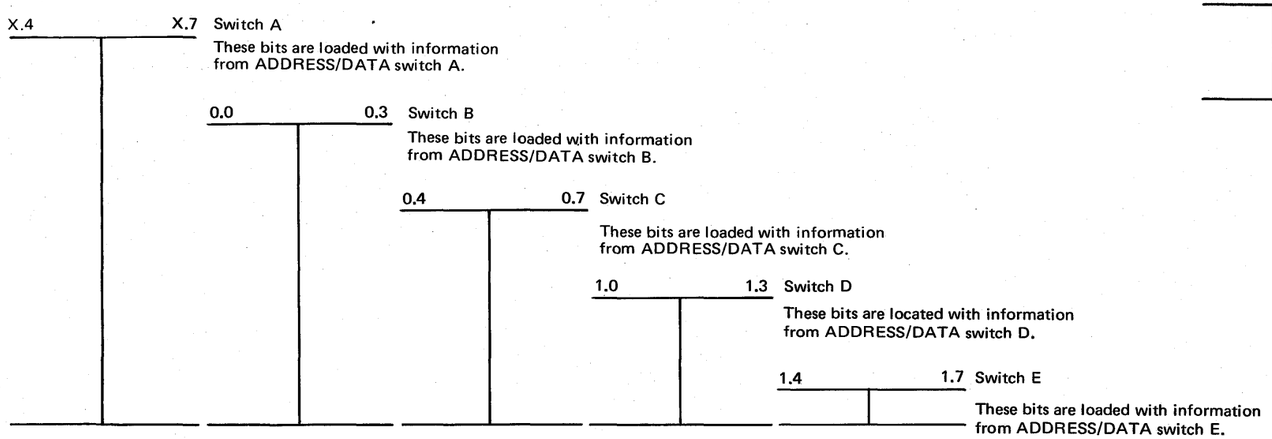




INPUT X'71' PANEL ADDR/DATA ENTRY DIGITS

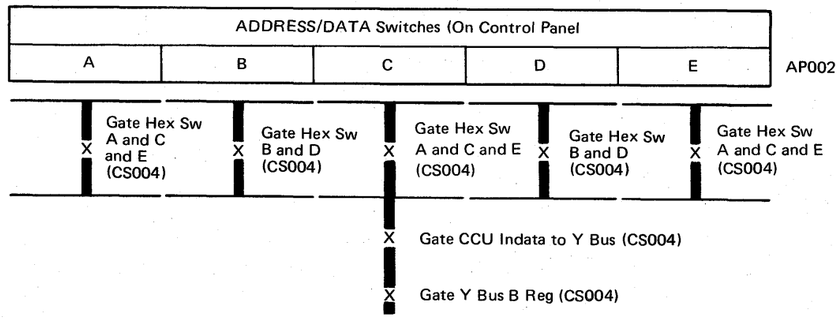
Input X'71' causes the general register specified by the R field to be loaded according to the setting of the ADDRESS/DATA switches on the control panel.

GENERAL REGISTER BIT DEFINITIONS



X.4	X.5	X.6	X.7	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7
General Register R (In CCU)																			

HARDWARE FUNCTION



The contents of the Y bus are set in the B register at I1C time. Refer to the input instruction on page 6-710.

INPUT X'72' DISPLAY/FUNCTION SELECT SWITCH

Input X'72' causes the general register specified by the R field to be loaded with information indicating the position of the DISPLAY/FUNCTION SELECT switch.

GENERAL REGISTER BIT DEFINITIONS

0.0 — 0.2 These bits are "0".

0.3 Storage Address

A "1" indicates that the DISPLAY/FUNCTION SELECT switch is in STORAGE ADDRESS.

0.4 Register Address

A "1" indicates that the DISPLAY/FUNCTION SELECT switch is in REGISTER ADDRESS.

0.5 — 0.7 These bits are "0".

1.0 This bit is "0".

1.1 Function Select 1

A "1" indicates that the DISPLAY/FUNCTION SELECT switch is in FUNCTION 1.

1.2 Function Select 2

A "1" indicates that the DISPLAY/FUNCTION SELECT switch is in FUNCTION 2.

1.3 Function Select 3

A "1" indicates that the DISPLAY/FUNCTION SELECT switch is in FUNCTION 3.

1.4 Function Select 4

A "1" indicates that the DISPLAY/FUNCTION SELECT switch is in FUNCTION 4.

1.5 Function Select 5

A "1" indicates that the DISPLAY/FUNCTION SELECT switch is in FUNCTION 5.

1.6 Function Select 6

A "1" indicates that the DISPLAY/FUNCTION SELECT switch is in FUNCTION 6.

1.7 This bit is "0".

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0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7
General Register (In CCU)															

HARDWARE FUNCTION

DISPLAY/FUNCTION SELECT Switch — AP005

X Gate Input 72 (CQ004)

X Gate CCU Indata to Y Bus (CS004)

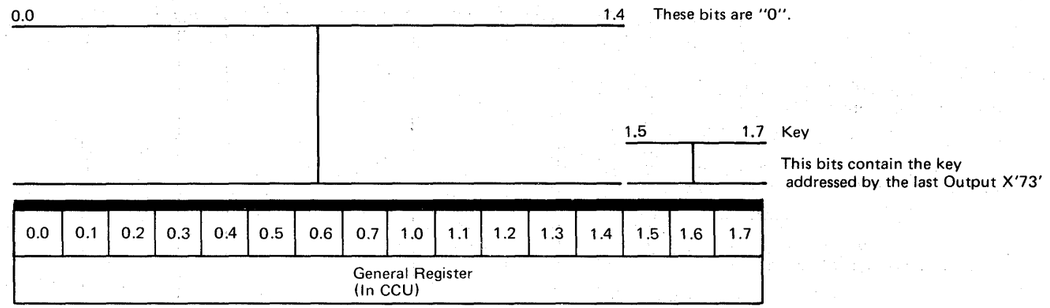
X Gate Y Bus to B Reg (CS004)

The contents of the Y bus are set in the B register at I1C time. Refer to the input instruction on page 6-710.

INPUT X'73' INSERT KEY

Input X'73' is associated with storage protection. When executed, the key addressed by the last Output X'73' is inserted into bits 1.5-1.7 of the general register specified by the R field.

GENERAL REGISTER BIT DEFINITIONS



HARDWARE FUNCTION

The contents of the Y bus are set in the B register at I1C time. Refer to the input instruction on page 6-710.

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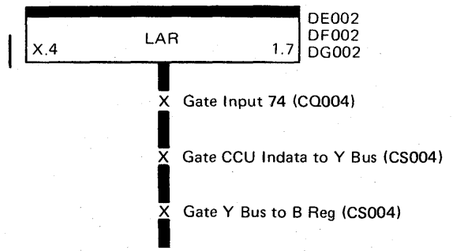
INPUT X'74' LAGGING ADDRESS REGISTER

When an Input X'74' is executed, the contents of the lagging address register (LAR) are transferred to the register specified by the R field. If this input is executed at program level 2, 3, or 4, the address from LAR is of the last instruction executed before the input. If this input is executed in program level 1, the address from LAR is of the last instruction executed before entering level 1.



The contents of the Y bus are set in the B register at I1C time. Refer to the input instruction on page 6-710.

INPUT X'76' ADAPTER LEVEL 1 INTERRUPT REQUESTS

Input X'76' is associated with program level 1 interrupt requests. Execution of this instruction loads the general register specified by the R field with bits that indicate the origin of an adapter level 1 interrupt request.

GENERAL REGISTER BIT DEFINITIONS

0.0 Type 4 CA #1, #2, #3, or #4
A "1" indicates that type 4 CA #1, 2, 3, or 4 has requested a program level 1 interrupt.

0.1 Type 1, 2, or 3 Scanner # 1 L1
A "1" indicates that type 1, 2, or 3 scanner # 1 has requested a program level 1 interrupt.

0.2 Type 2 or 3 Scanner # 2 L1
A "1" indicates that type 2 or 3 scanner # 2 has requested a program level 1 interrupt.

0.3 Type 2 or 3 Scanner # 3 L1
A "1" indicates that type 2 or 3 scanner # 3 has requested a program level 1 interrupt.

0.4 Type 2 or 3 Scanner # 4 L1
A "1" indicates that type 2 or 3 scanner # 4 has requested a program level 1 interrupt.

0.5 Type 1, 2, or 3 CA # 1 or Selected Type 4 CA L1
A "1" indicates that a type 1, 2, or 3 CA # 1 or selected type 4 CA has requested a program level 1 interrupt.

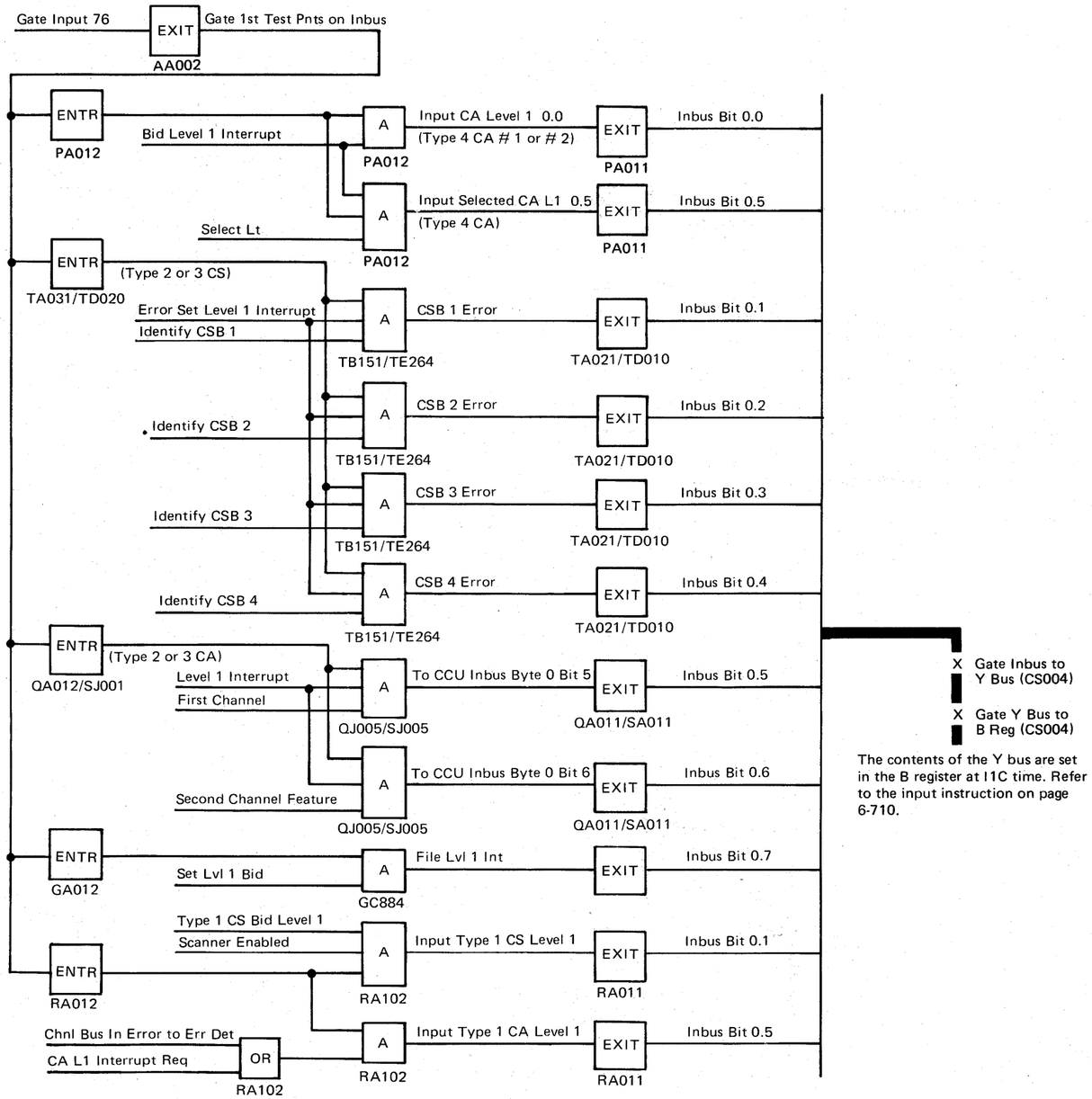
0.6 Type 2 or Type 3 CA # 2 L1
A "1" indicates that the type 2 or 3 CA #2 has requested a program level 1 interrupt.

0.7 Remote Program Loader L1
A "1" indicates that the Remote Diskette Controller has requested a program level 1 interrupt.

1.0 These bits are 0 1.7

0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7
General Register (In CCU)															

HARDWARE FUNCTION



The contents of the Y bus are set in the B register at I1C time. Refer to the input instruction on page 6-710.

INPUT X'77' ADAPTER LEVEL 2 OR 3 INTERRUPT REQUESTS

Input X'77' is associated with program level 2 and level 3 interrupt requests. Execution of this instruction loads the general register specified by the R field with bits to indicate the origin of an adapter level 2 or 3 interrupt request.

When priority selection is required with two type 4 CAs, this instruction sets or resets the selected latch in each type 4 CA according to the state of the 'CA4 has priority' latch. It also resets the 'prime priority select' latch.

GENERAL REGISTER BIT DEFINITIONS

0.0 This bit is 0.

0.1 Type 1, 2, or 3 Scanner L2
A "1" indicates that a scanner has requested a program level 2 interrupt.

0.2 – 0.7 These bits are 0

1.0 Type 4 CA L3
A "1" indicates that type 4 CA #1, #2, #3, or #4 has requested a program level 3 interrupt.

1.1 Remote Program Loader L3
A "1" indicates that the Remote Diskette Controller has requested a program level 3 interrupt.

1.2 Type 2 or Type 3 CA # 2 L3
A "1" indicates that a type 2 or 3 CA #2 has requested a program level 3 interrupt.

1.3 Type 1 or Selected Type 4 CA Data/Status L3
A "1" indicates that a type 1 or selected type 4 CA has requested a program level 3 data service interrupt.

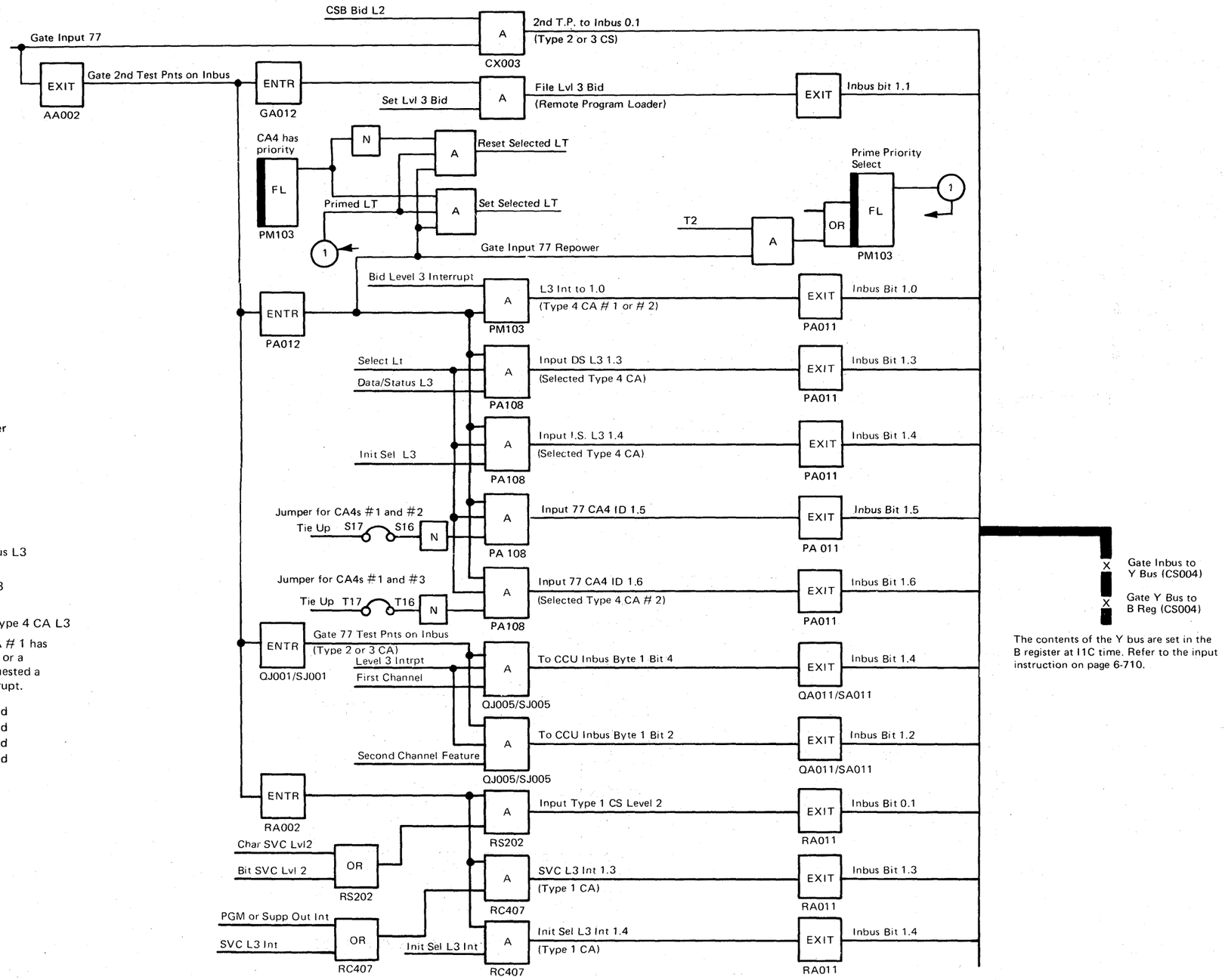
1.4 Type 1, 2, or 3 CA # 1 or Selected Type 4 CA L3
A "1" indicates that a type 2 or 3 CA # 1 has requested a program level 3 interrupt or a type 1 or selected type 4 CA has requested a program level 3 initial selection interrupt.

1.5, 1.6
00 – Type 4 CA #1 selected
01 – Type 4 CA #2 selected
10 – Type 4 CA #3 selected
11 – Type 4 CA #4 selected

1.7 This bit is 0.

0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7
General Register R (In CCU)															

HARDWARE FUNCTION



The contents of the Y bus are set in the B register at I1C time. Refer to the input instruction on page 6-710.

INPUT X'79' UTILITY

Input X'79' causes the general register specified by the R field to be loaded with information indicating (1) the state of the program level 5 C and Z condition latches, (2) the last program level to be active before a level 1 interrupt, (3) the state of the IPL escape control, and (4) the type CA installed in the first frame position.

GENERAL REGISTER BIT DEFINITIONS

0.0 - 0.4 These bits are 0.

0.5 A "1" indicates 900 nanosecond cycle time.

0.6 Program Level 5, C Condition

A "1" indicates that the 'C Condition' latch for program level 5 is on.

0.7 Program Level 5, Z Condition

A "1" indicates that the 'Z condition' latch for program level 5 is on.

1.0 Program Level 2

A "1" indicates that program level 2 was interrupted by program level 1. See Note 1.

1.1 Program Level 3

A "1" indicates that program level 3 was interrupted by program level 1. See Note 1.

1.2 Program Level 4

A "1" indicates that program level 4 was interrupted by program level 1. See Note 1.

1.3 Program Level 5

A "1" indicated that program level 5 or the "WAIT" state was interrupted by program level 1. See Note 1.

1.4 FET Storage

A "1" indicates that the 3705 contains FET Storage.
A "0" indicates that the 3705 contains a bridge storage.

1.5 See Note 2

A '0' indicates a 3705 Communications Controller
A'1' indicates a 3704 Communications Controller

1.6 A '1' indicates that a Type 1 CA or Type 4 CA is installed in the first frame position. See Note 1.

1.7 IPL Escape Control

A '0' indicates that a jumper has been installed by a CE at the customer's request. By forcing a branch to storage location X'06FC', this jumper causes a bypass of the part of the bootstrap program that controls the initial program load. See Note 1.

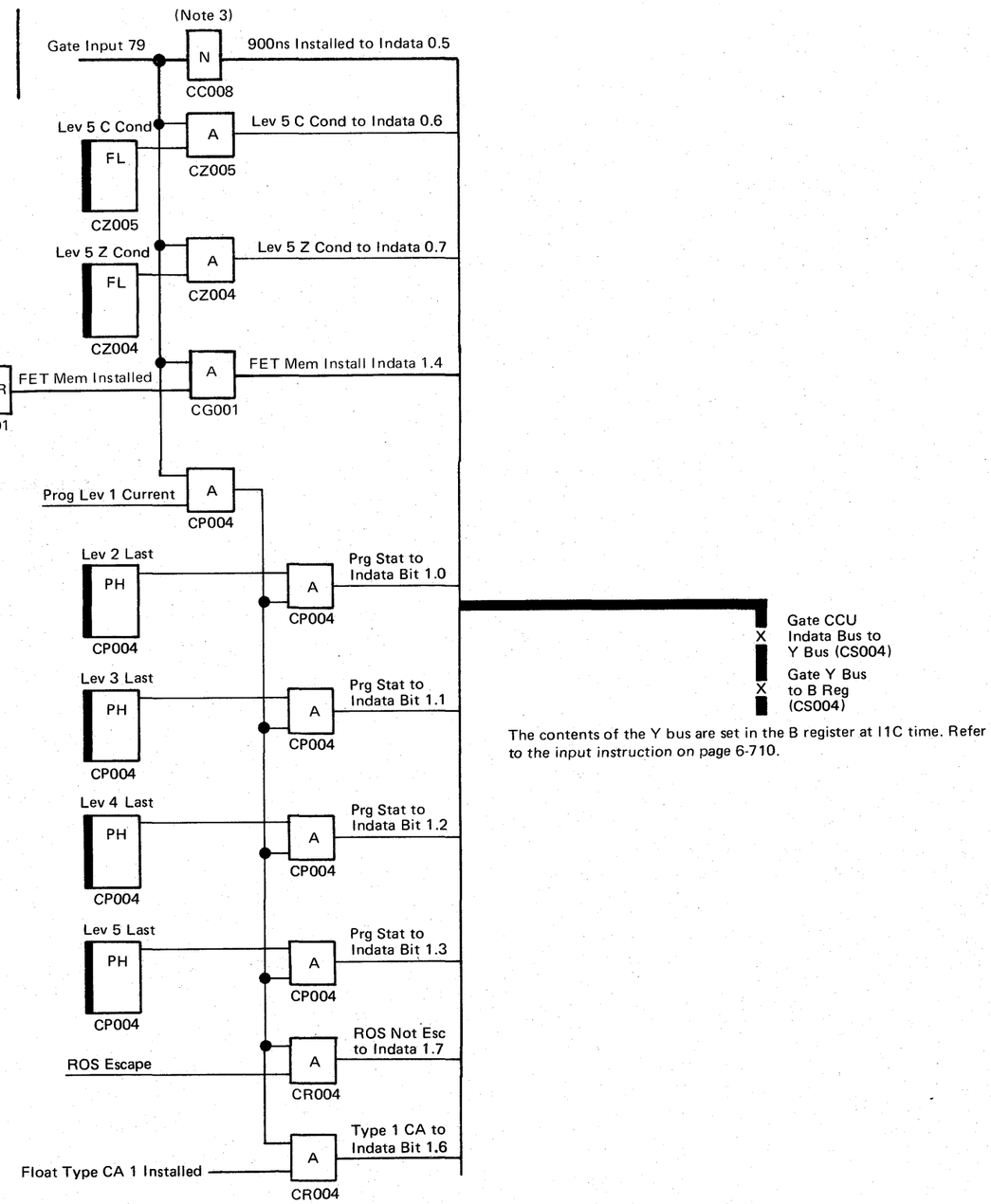
0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7
General Register (In CCU)															

Note 1: Bits 1.0-1.3 and 1.6-1.7 are 0 if input X'79' is executed when not in program level 1.

Note 2: The 3705 Communications Controller has no hardware to force a 0 in bit 1.5- it results as a default condition. The 3704 Communications Controller has the hardware to force a 1 in 1.5.

Note 3: Present only with 900 nanosecond cycle time (17.778 MHz oscillator).

HARDWARE FUNCTION



The contents of the Y bus are set in the B register at I1C time. Refer to the input instruction on page 6-710.

INPUT X'7A' CYCLE UTILIZATION COUNTER REGISTER

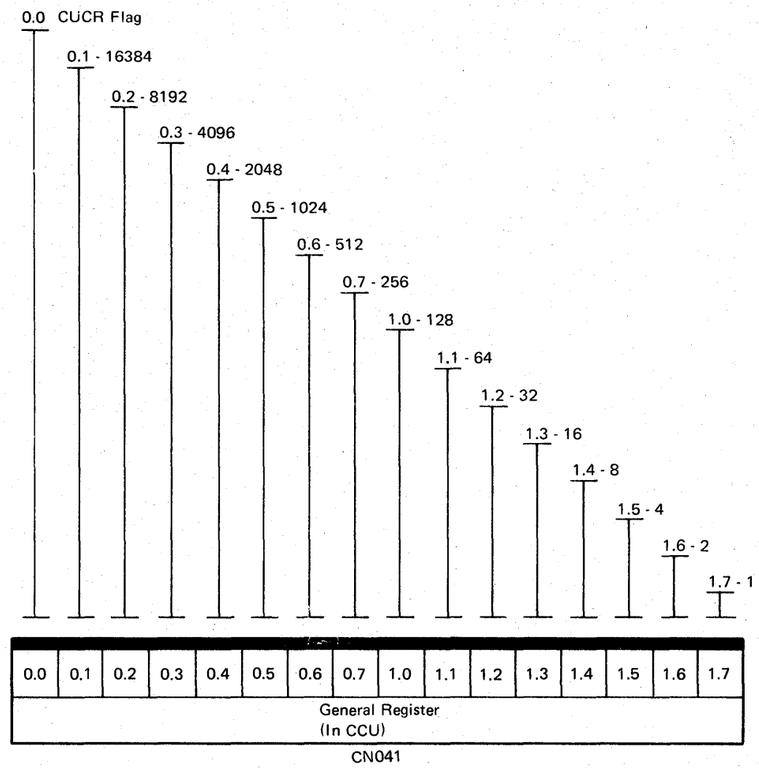
The Cycle Utilization Counter Register (CUCR) is accessed via an Input X'7A' instruction. Input X'7A' provides 15 data bits and a flag bit which sets to 1 to indicate CUCR. The data bits are incremented once for each 8 cycles that are utilized. Utilized cycles are defined as cycles taken for:

- Instruction execution
- Cycle steal operations
- Maintenance cycles (e.g., panel operations)

Notes:

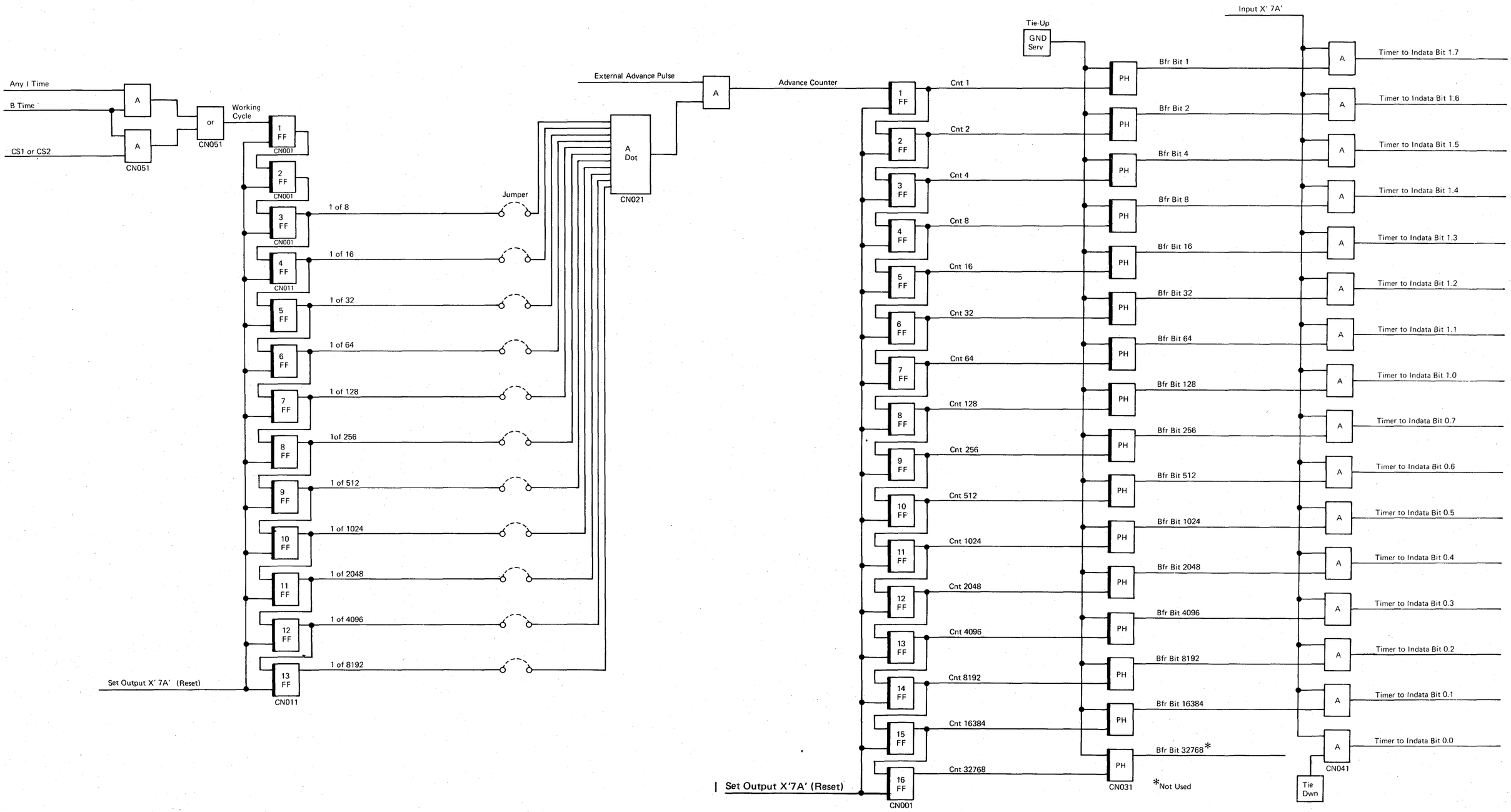
1. The Cycle Utilization Counter Register is a standard feature on 3705 Models J-L only. The counter is also available for 3705 Models E-H, but only on an RPQ basis.
2. For 3705 Models E-H containing a Cycle Utilization Counter Register RPQ, the register must be cleared to zero. To determine if a Cycle Utilization Counter Register RPQ is installed and clear the register:
   a. Execute a Load Halfword instruction (storage = X'0000').
   b. Execute any Output instruction with the register specified equal to X'0000'.
   c. Execute an Input X'7A' instruction to determine if bit 0.0 of the CUCR is set to "1". If bit 0.0 of the CUCR is set to "1" the CUCR is installed.

GENERAL REGISTER BIT DEFINITIONS



CN041

CYCLE UTILIZATION COUNTER REGISTER OPERATION



INPUT X'7B' BSC CRC REGISTER

The old CRC accumulation in the P register and the new character in the Q register are combined in the new CRC generation circuitry. Input X'7B' selects the output lines (S0 to S15) from the new CRC generation circuitry that corresponds to BSC CRC checking.

CRC GENERATION EXAMPLE

A typical update of the CRC, located in the Character Control Block area, is provided below.

1 Output X'7E' (Set Mask Bits)—to prevent interrupts.

2 Load Halfword—loads the P register with the old CRC accumulation. Each Load Halfword executed changes the contents of the P register; therefore, a Load Halfword instruction should not be executed again until the new accumulated CRC is loaded into a CCU general register.

3 Insert Character—places the new character in a general register.

4 Any output instruction—places the new character in the Q register when the general register used in step 3 is specified in the 'R' field.

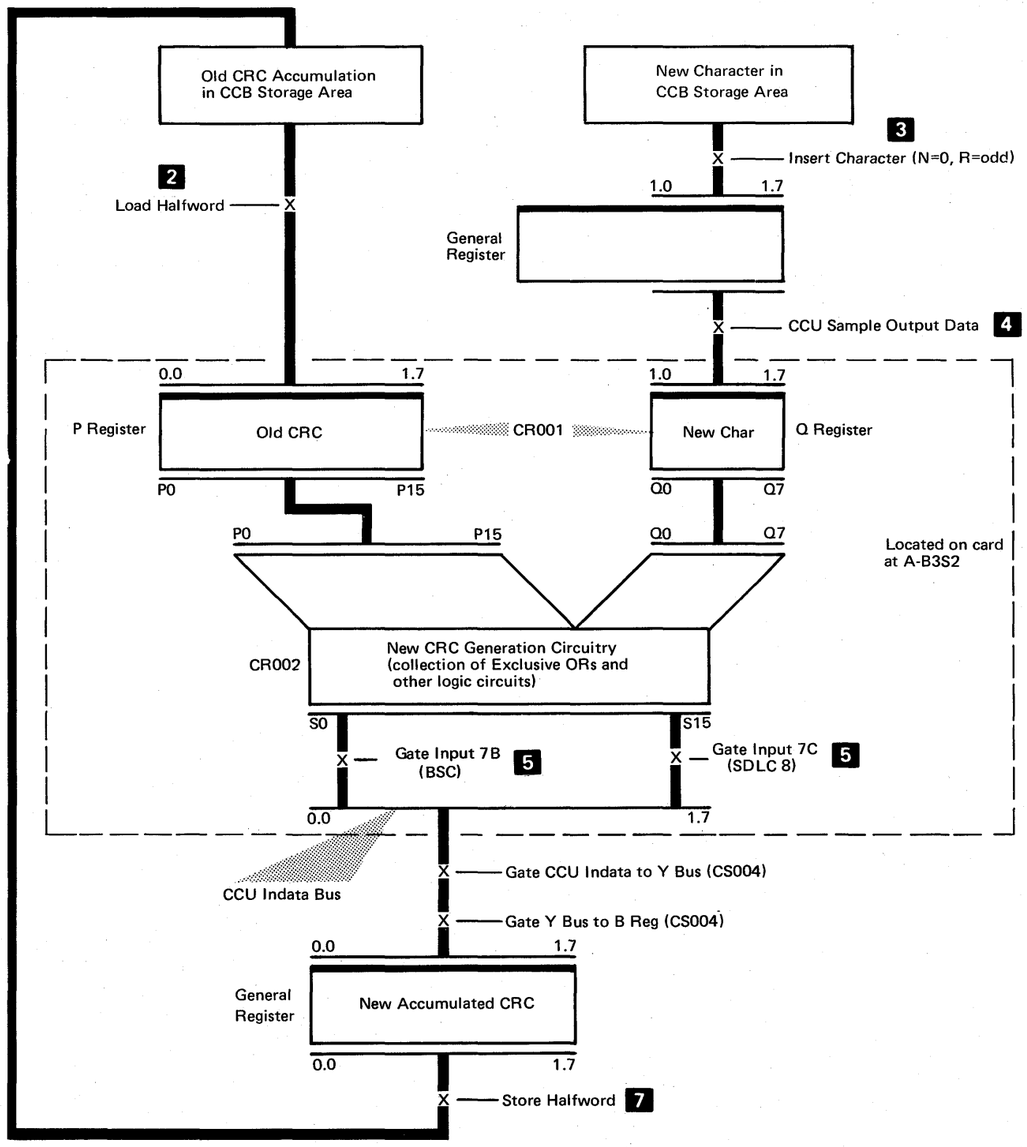
5 Input X'7B' (BSC CRC Register) or
Input X'7C' (SDLC 8 CRC Register) —selects the corresponding outputs of the new CRC generation circuitry and places the new accumulated CRC in the general register specified in the 'R' field.

6 Output X'7F' (Reset Mask Bits)—allows interrupts.

7 Store Halfword—stores new CRC accumulation in the CCB area on storage.

INPUT X'7C' SDLC 8 CRC REGISTER

The old CRC accumulation in the P register and the new character in the Q register are combined in the new CRC generation circuitry. Input X'7C' selects the output lines (S0 to S15) from the new CRC generation circuitry that corresponds to SDLC 8 CRC checking.



INPUT X'7D' CCU CHECK REGISTER

Input X'7D' sets the bits in the general register specified by the R field to correspond to the CCU check register. Pages 6-050 and 6-051 show the CCU check register.

GENERAL REGISTER BIT DEFINITION

0.0 Byte X Check

A "1" indicates a parity check in byte X (except for SDR).

0.1 Byte 0 Check

A "1" indicates a parity check in byte 0.

0.2 Byte 1 Check

A "1" indicates a parity check in byte 1 (bytes 1 or X for SDR).

0.3 L1 Program Check

A "1" indicates that a program check occurred while in program level 1.

0.4 SAR Check

A "1" indicates a storage address register parity check. Bit 0.0, 0.1, or 0.2 indicates which byte of the storage address register caused the check.

05. SDR Check

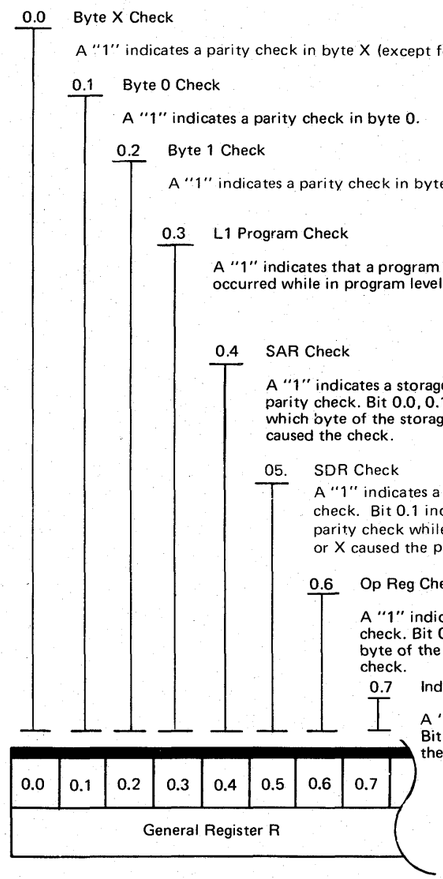
A "1" indicates a storage data register parity check. Bit 0.1 indicates SDR byte 0 caused the parity check while bit 0.2 indicates SDR bytes 1 or X caused the parity check.

0.6 Op Reg Check

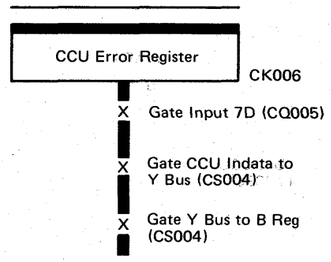
A "1" indicates an operation register parity check. Bit 0.0, 0.1, or 0.2 indicates which byte of the operation register caused the check.

0.7 Indata Bus Check

A "1" indicates an indata bus parity check. Bit 0.0, 0.1, or 0.2 indicates which byte of the indata bus caused the check.



HARDWARE FUNCTION



The contents of the Y bus are set in the B register out I1C time. Refer to the input instruction on page 6-710.

1.0 Cycle Counter Check

A "1" indicates that the CCU cycle counter signaled an even number of time slots to the CCU.

1.1 1.2 These bits are 0.

1.3 IPL Diskette Controller Error (see note)

1.4 IPL Media Error (see note)

1.5 CCU Checks

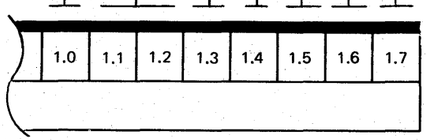
A "1" indicates the presence of a CCU check. This is a summary bit that is set to "1" whenever any of the CCU checks in this input are on. This bit should be checked first when checking for a CCU check condition.

1.6 Type 2 Attachment Base Clock Check.

A "1" indicates a type 2 attachment base clock check. The type 2 scanner clock signaled an incorrect number of time slots.

1.7 CCU Clock Check

A "1" indicates a central control unit clock check. The CCU clock signaled an incorrect number of time slots.

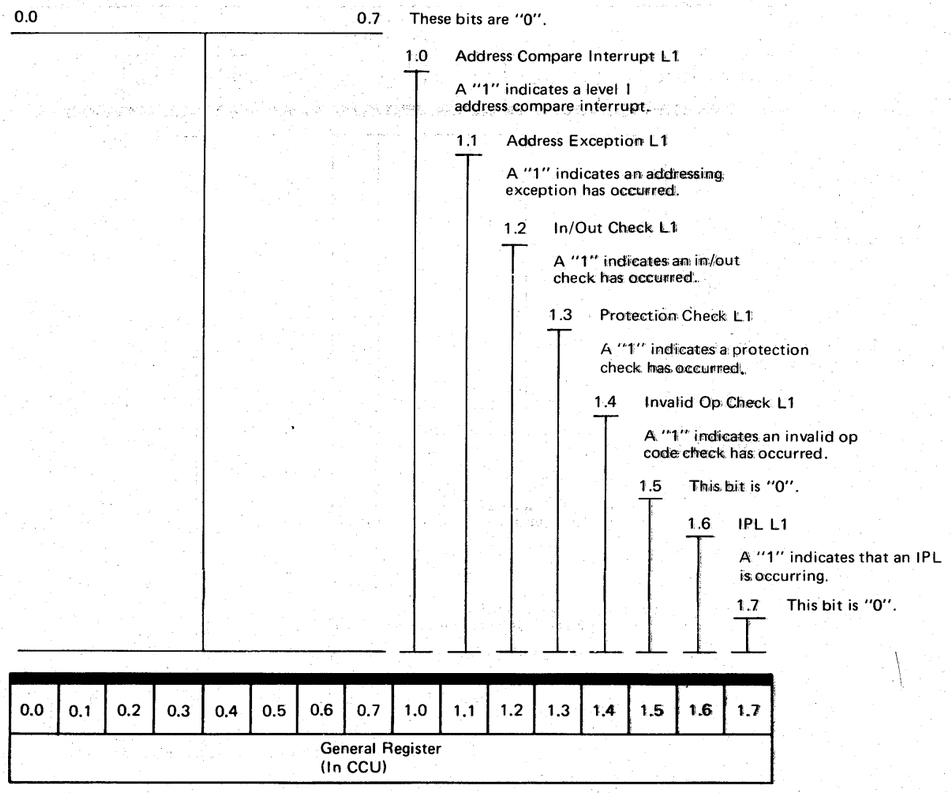


Note: A "1" indicates that an error message is stored at location X'0020'–X'003F'. Load Program 1 sets the indicator when the message is stored.

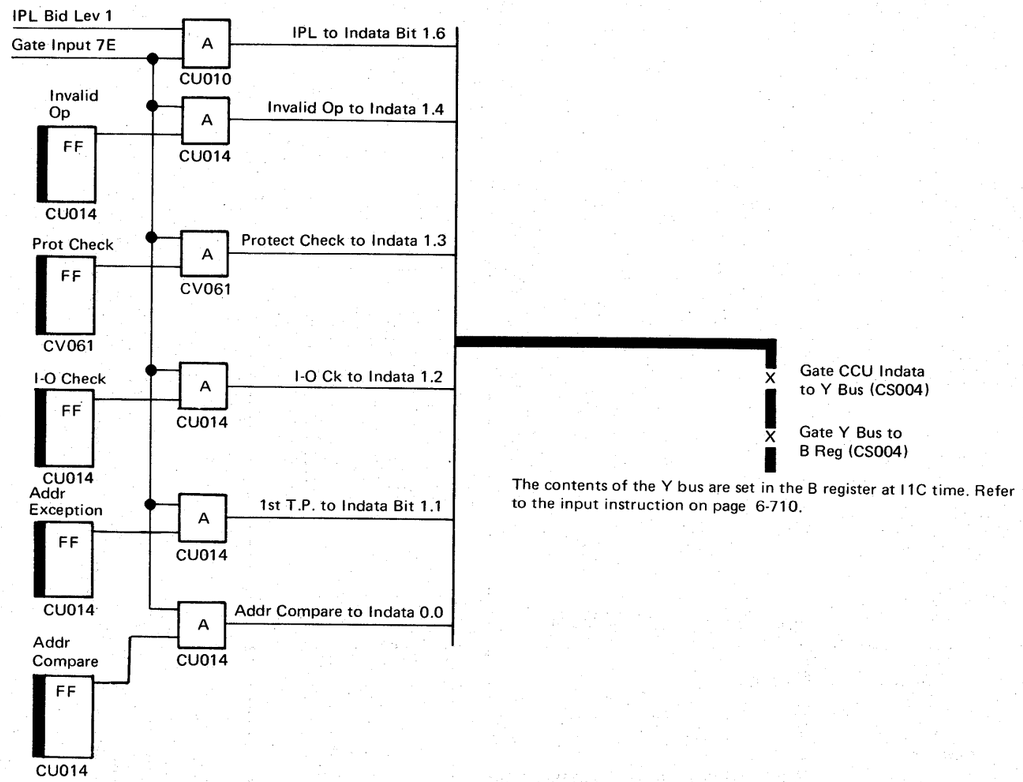
INPUT X'7E' CCU LEVEL 1 INTERRUPT REQUESTS

Input X'7E' sets the bits in the register specified by the R field to indicate which level 1 interrupt request is set. Bits 1.1–1.4 are set as the result of a program check in any level and cause a level 1 interrupt if the error occurred in program level 2-5. A program check in program level 1 causes an IPL. If a program check occurs during IPL, it causes a hard stop.

GENERAL REGISTER BIT DEFINITIONS



HARDWARE FUNCTION

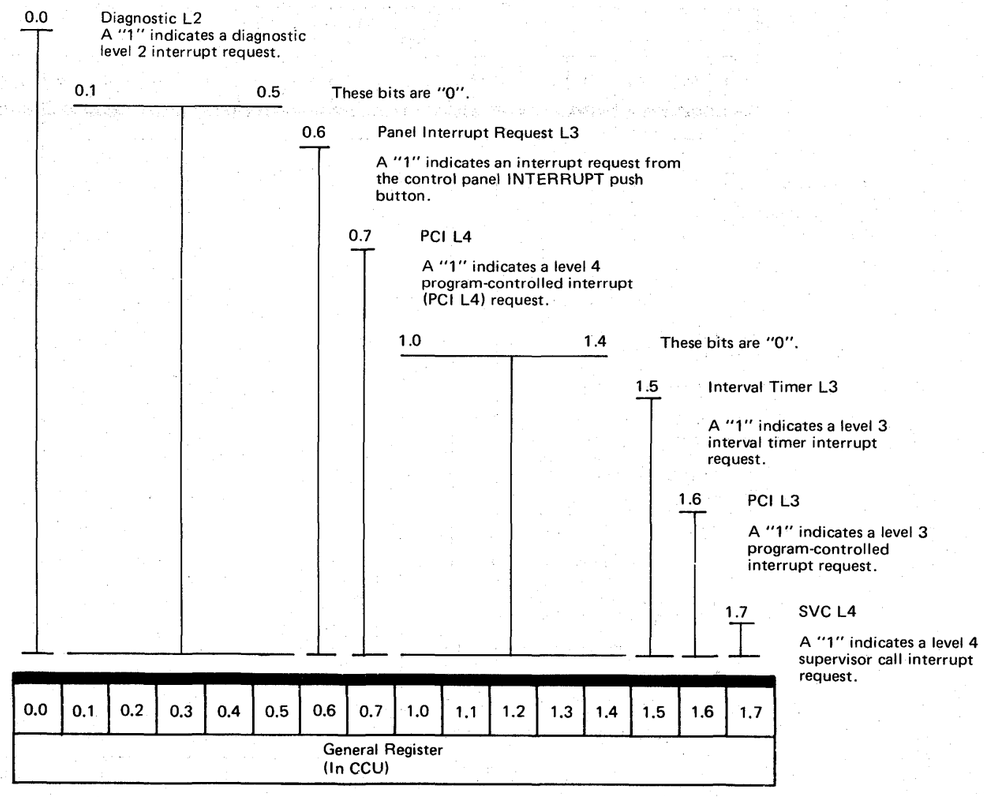


The contents of the Y bus are set in the B register at I1C time. Refer to the input instruction on page 6-710.

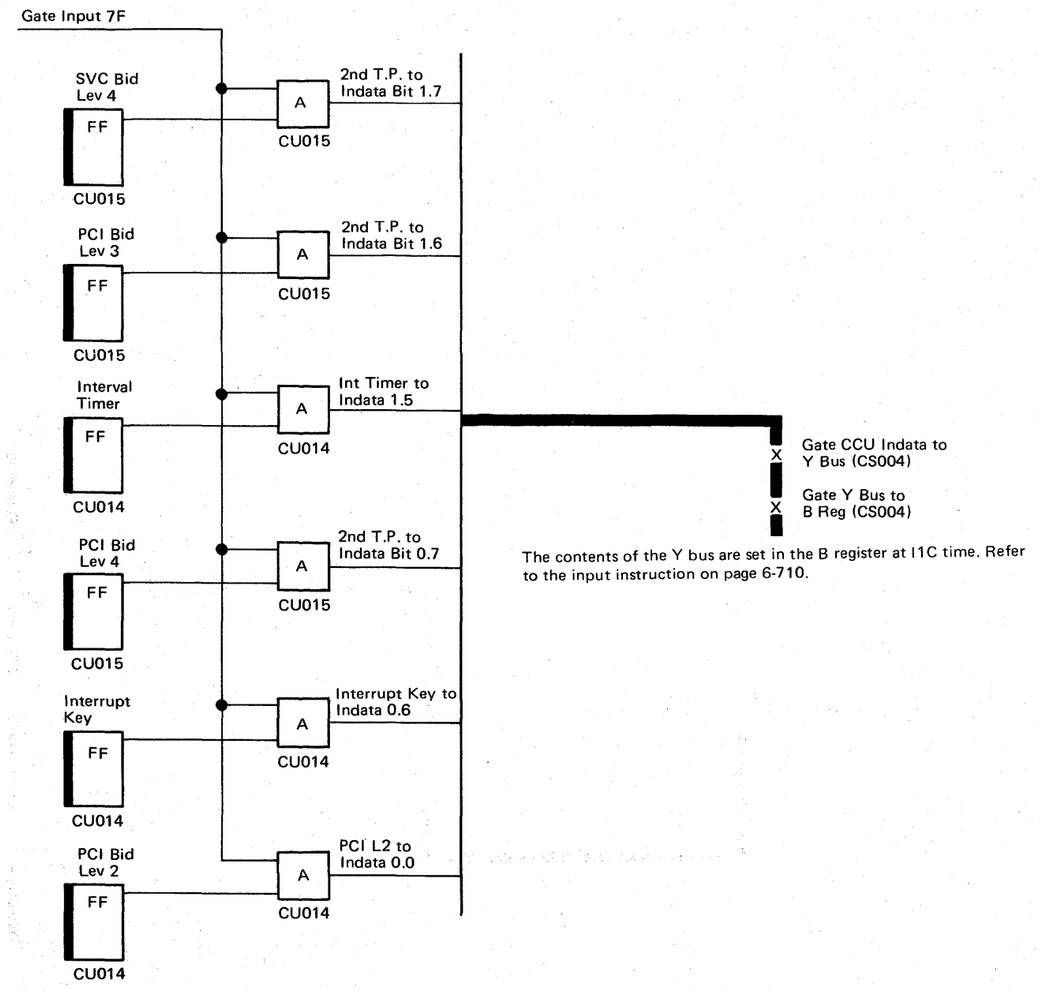
INPUT X'7F' CCU LEVEL 2, 3, OR 4 INTERRUPT REQUESTS

Input X'7F' sets bits in the general register specified by the R field to indicate which level 2, 3, or 4 interrupt requests are set.

GENERAL REGISTER BIT DEFINITIONS



HARDWARE FUNCTION



The contents of the Y bus are set in the B register at I1C time. Refer to the input instruction on page 6-710.

CCU OUTPUT INSTRUCTIONS

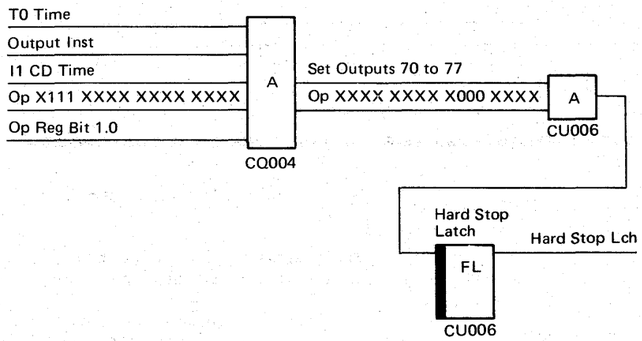
The CCU has 43 assigned output instructions. These output instructions set and reset various CCU latches and load external registers with data from general registers.

OUTPUTS X'00' TO X'1F' GENERAL REGISTERS

Outputs X'00'-X'1F' load the contents of the general register specified by the R field into the general register specified by the E field.
At I1D time, the contents of the Z bus (contents of the register specified by the R field) are set in the general register specified by the E field. Refer to the output instruction on page 6-730.

OUTPUT X'70' HARDSTOP

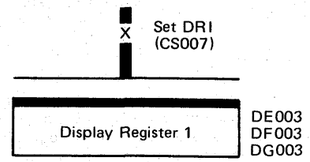
Output X'70' causes the 'hardstop' latch to set. The 3705 comes to a complete stop, and IPL is required to continue processing using the adapters. The bit settings are ignored since this output performs performs a control function.

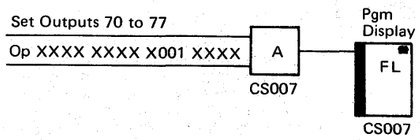


OUTPUT X'71' DISPLAY REGISTER 1

Output X'71' causes the contents of the general register designated by the R field to be loaded in display register 1. The PROGRAM DISPLAY light also turns on.

At I1D time, the contents of the Z bus (contents of the general register specified by the R field) are set in display register 1. Refer to the output instruction on page 6-730.

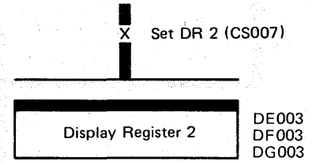


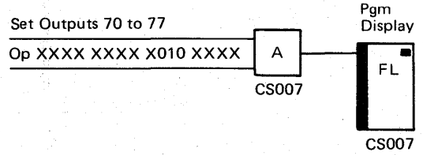


OUTPUT X'72' DISPLAY REGISTER 2

Executing Output X'72' causes the contents of the general register specified by the R field to be loaded in display register 2. The PROGRAM DISPLAY light also turns on.

At I1D time, the contents of the Z bus (contents of the general register specified by the R field) are set in display register 2. Refer to the output instruction on page 6-730.



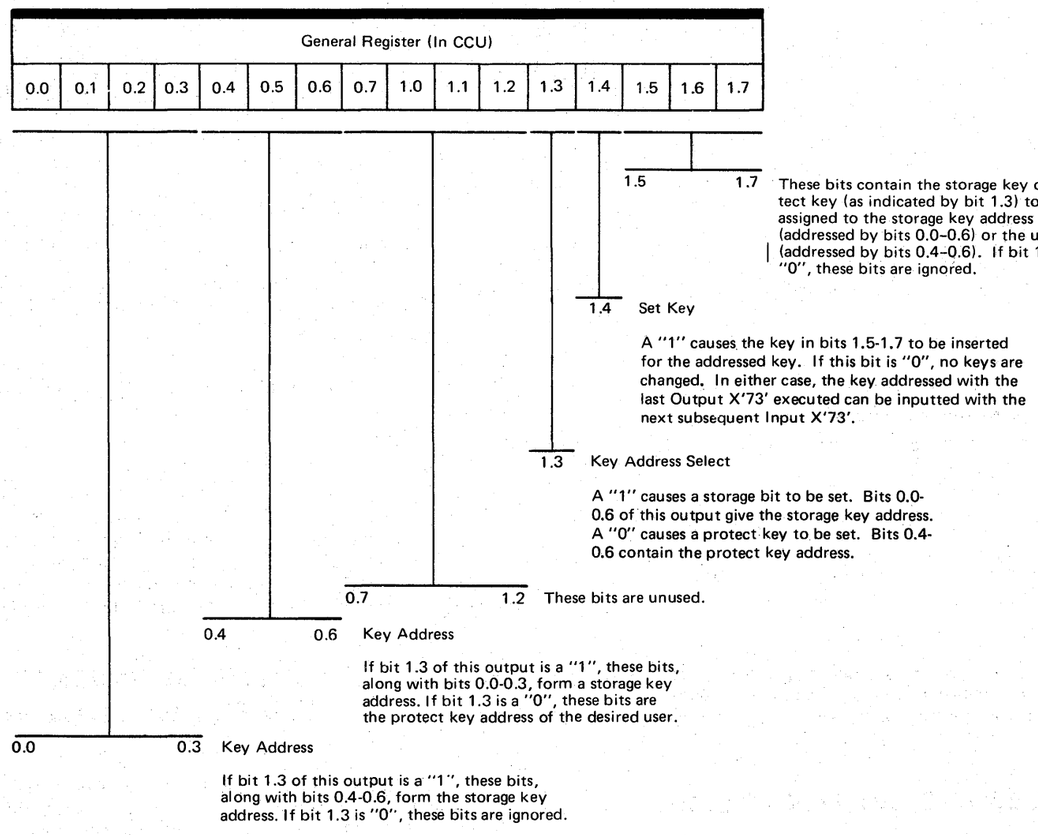


OUTPUT X'73' SET KEY – 3705s WITH UNDER 256K (PART 1)

Output X'73' is associated with storage protection. It is used to set either a storage key or a protect key with the contents of bits 1.5-1.7 of the general register designated by the R field. Bit 1.3 controls the selection of either a storage key or a protect key. If bit 1.4 is "1", the addressed key is set according to bits 1.5-1.7. If bit 1.4 is "0", the addressed key is not set.

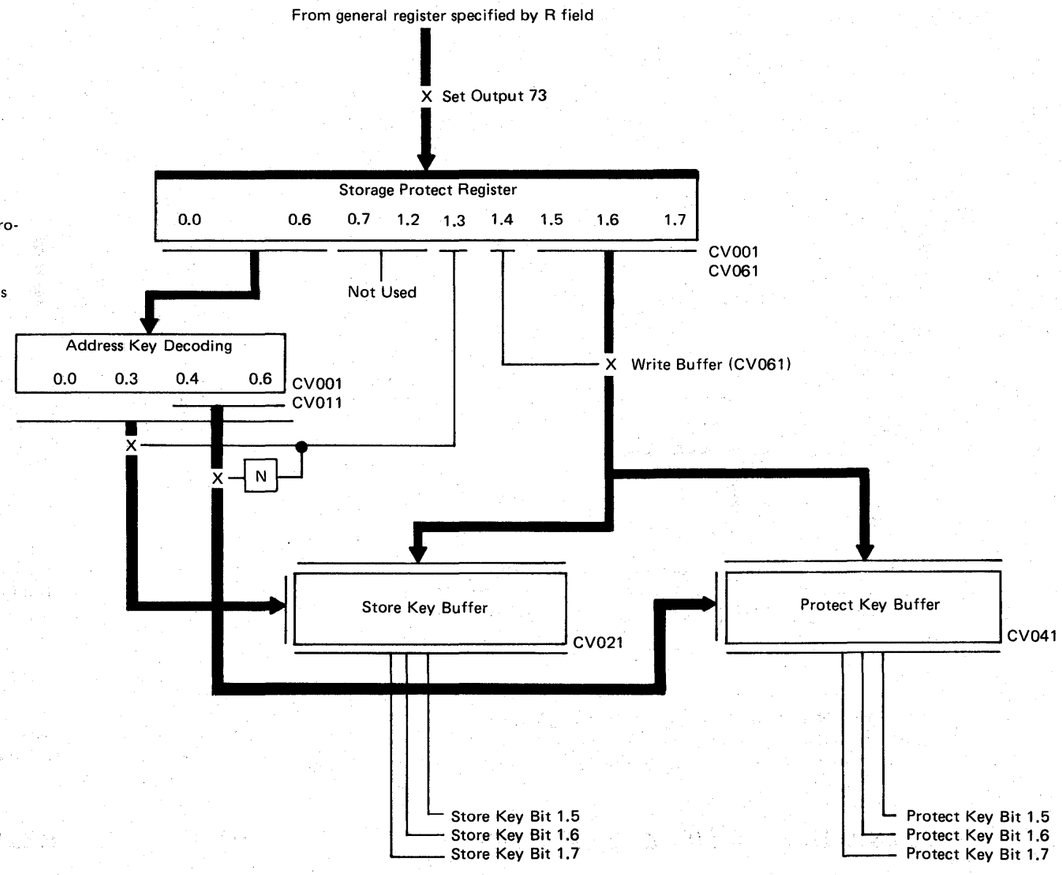
Input X'73' can be used to set bits in a general register according to the key addressed by the last Output X'73'.

GENERAL REGISTER BIT DEFINITIONS

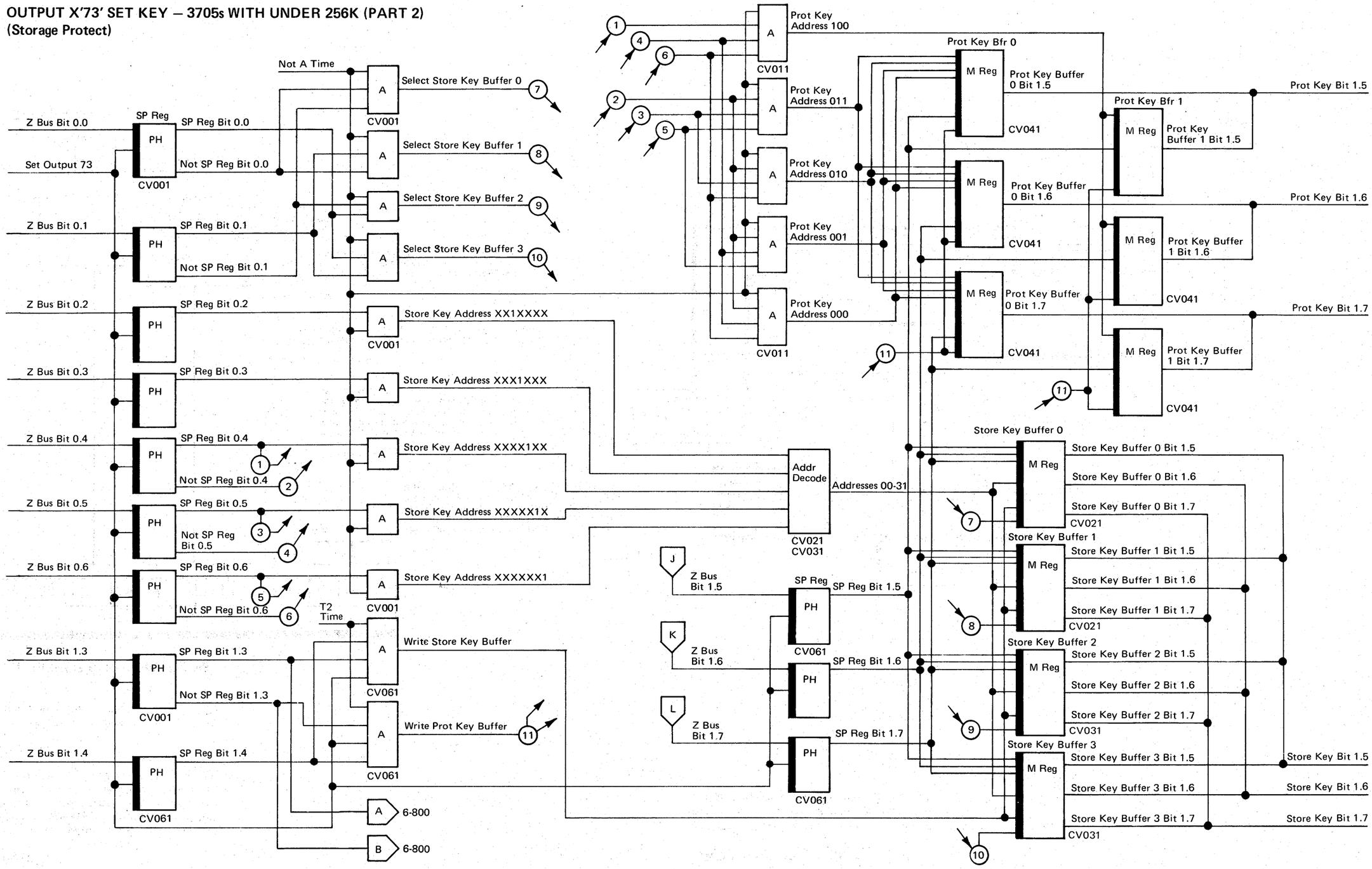


HARDWARE FUNCTION

The contents of the Z bus (contents of the general register specified by the R field) set storage protection at I1D time. Refer to the output instruction on page 6-730.



OUTPUT X'73' SET KEY – 3705s WITH UNDER 256K (PART 2)
(Storage Protect)



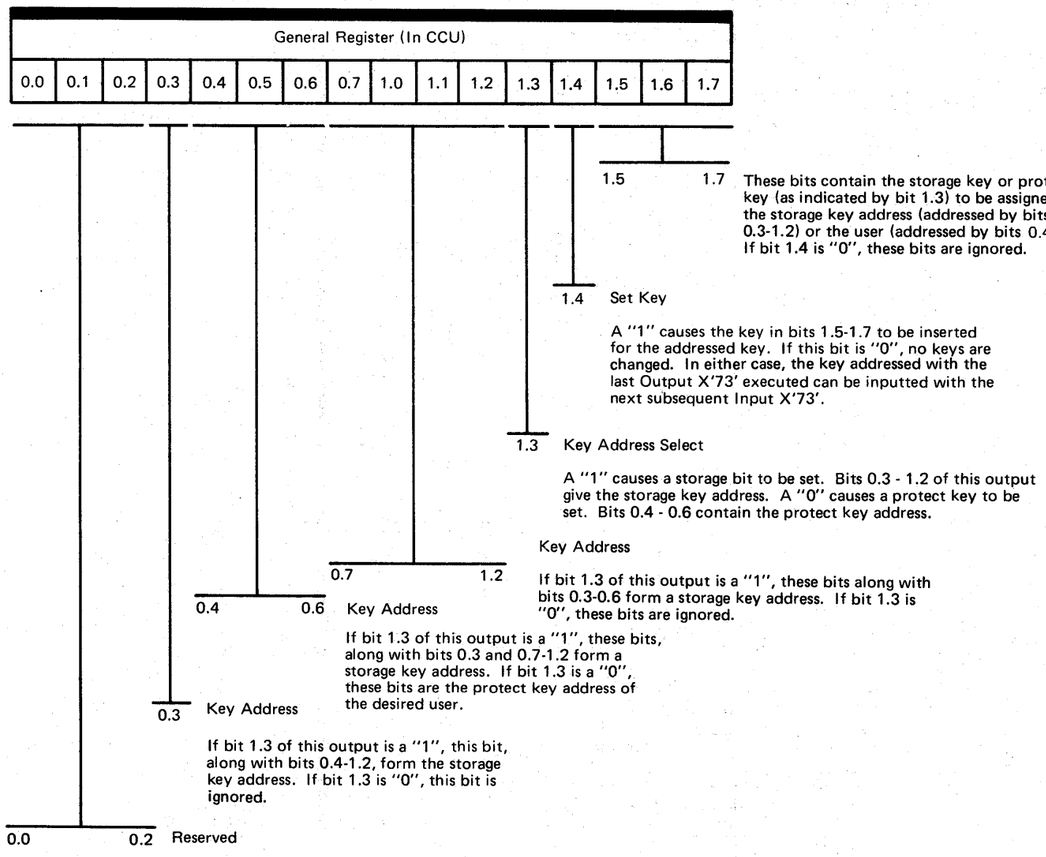
OUTPUT X'73' SET KEY – 3705s WITH OVER 256K (PART 1)

(Storage Protect)

Output X'73' is associated with storage protection. It is used to set either a storage key or a protect key with the contents of bits 1.5-1.7 of the general register designated by the R field. Bit 1.3 controls the selection of either a storage key or a protect key. If bit 1.4 is "1", the addressed key is set according to bits 1.5-1.7. If bit 1.4 is "0", the addressed key is not set.

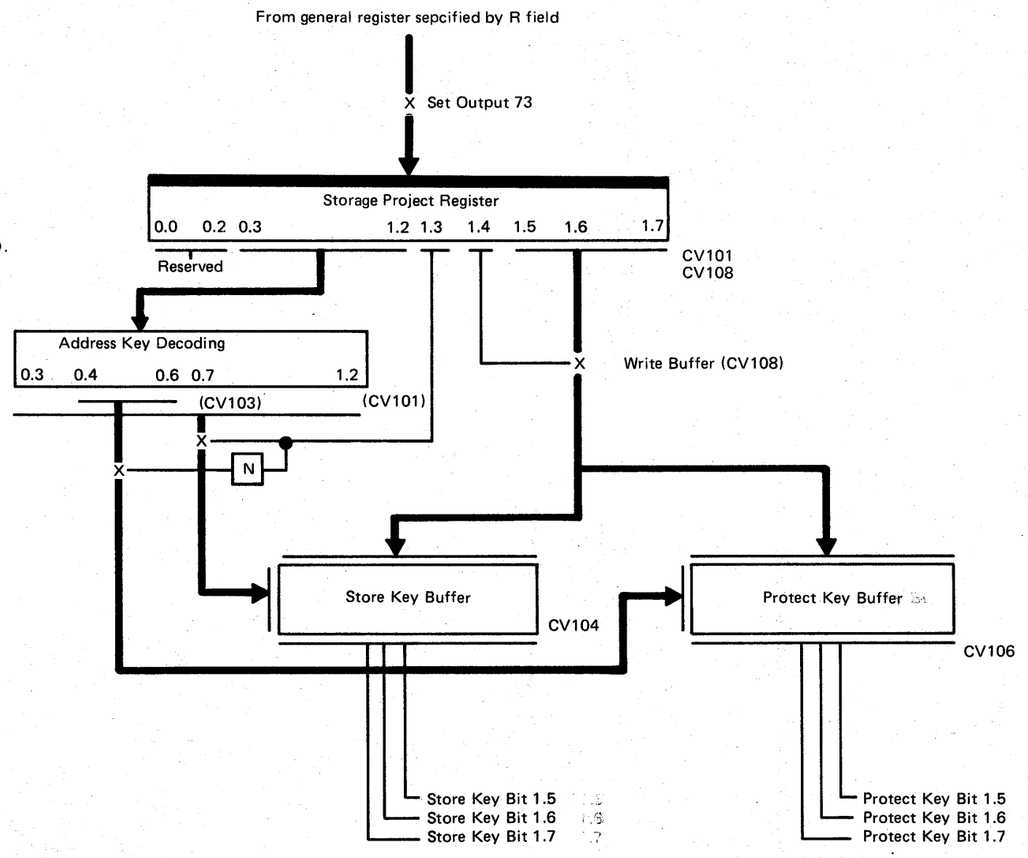
Input X'73' can be used to set bits in a general register according to the key addressed by the last Output X'73'.

GENERAL REGISTER BIT DEFINITIONS

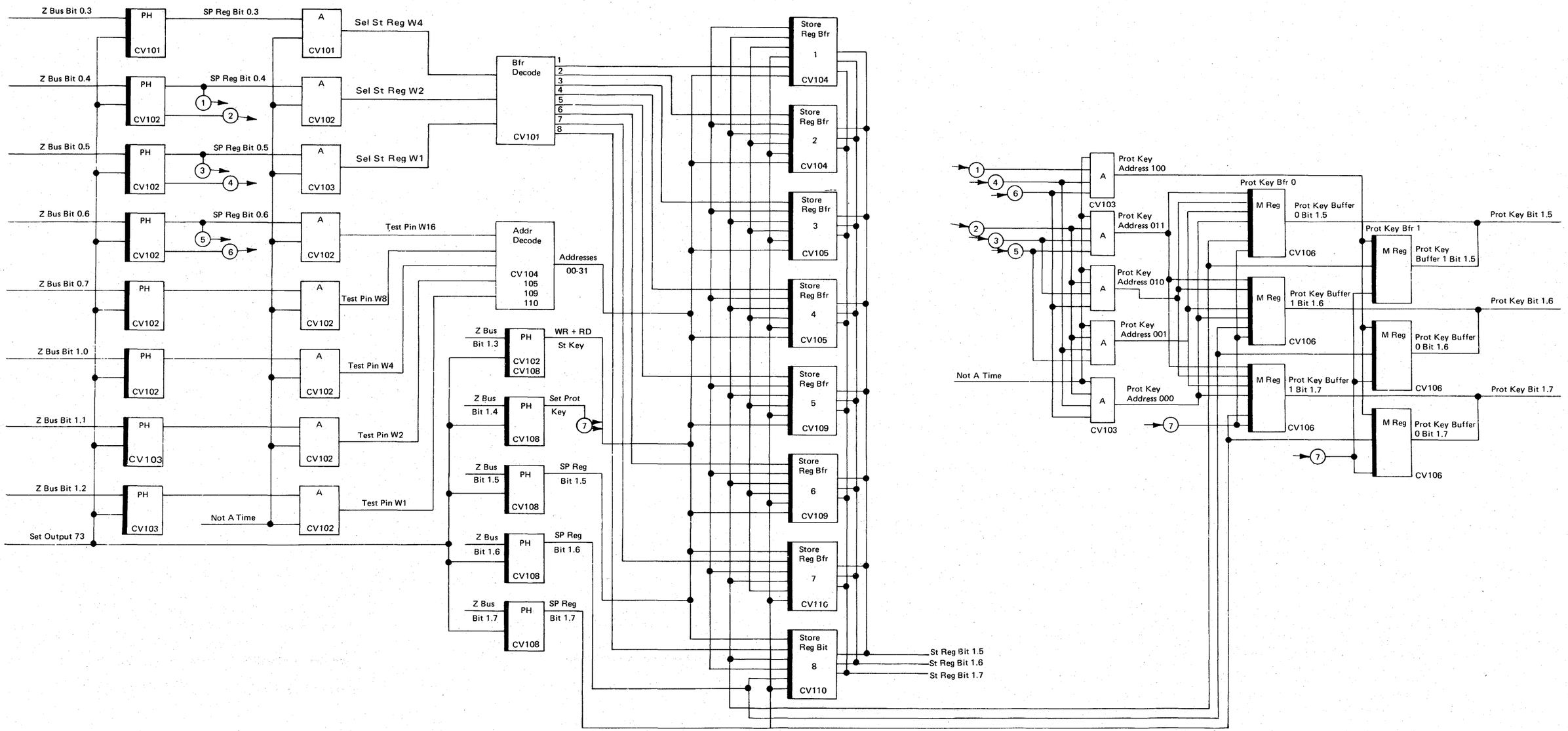


HARDWARE FUNCTION

The contents of the Z bus (contents of the general register specified by the R field) set storage protection at I1D time. Refer to the output instruction on page 6-730.



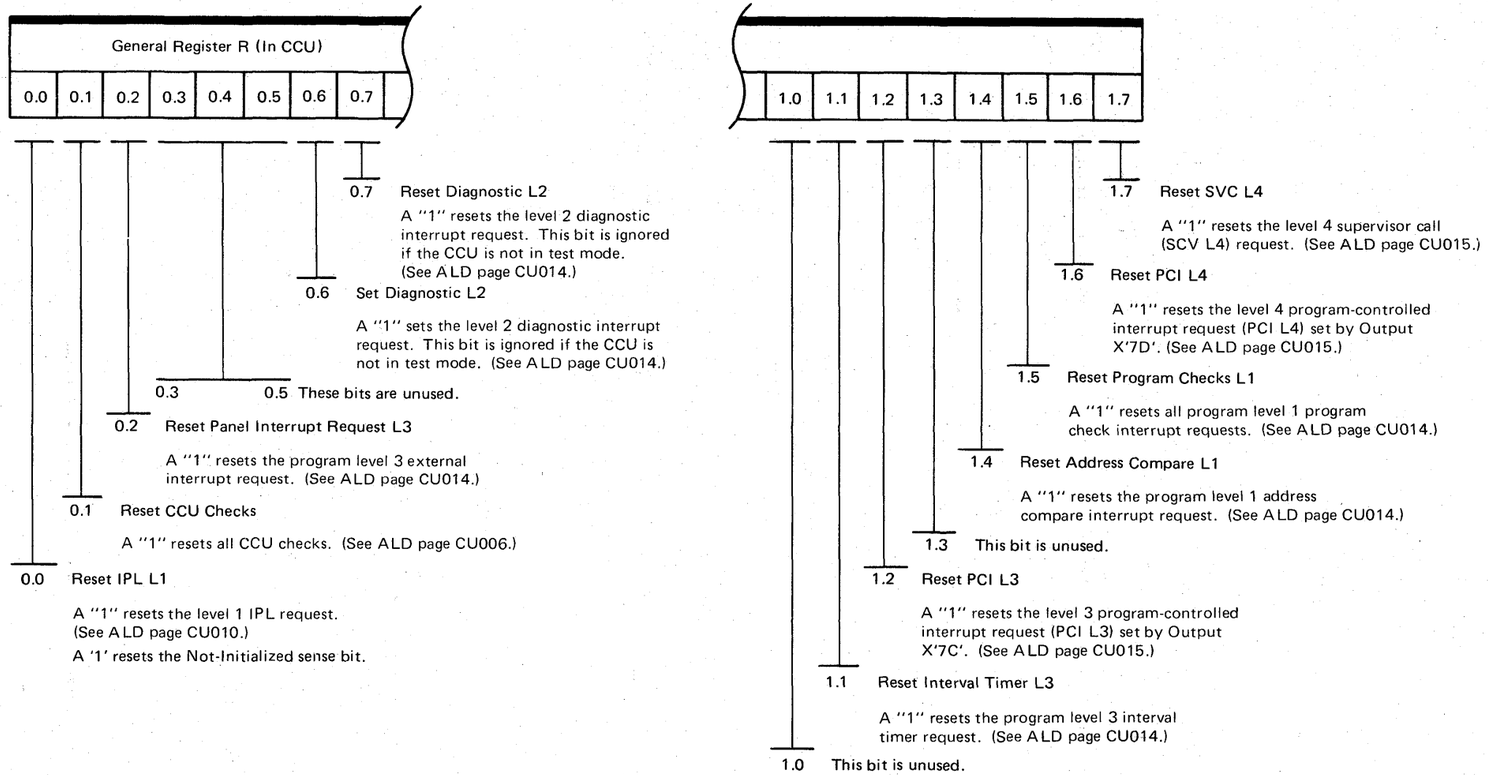
OUTPUT X'73' SET KEY — 3705s WITH OVER 256K (PART 2) (STORAGE PROTECT)



OUTPUT X'77' MISCELLANEOUS CONTROLS

Output X'77' contains controls used to set or reset various interrupt requests.

GENERAL REGISTER BIT DEFINITIONS



HARDWARE FUNCTION

At I1D time, the contents of the Z bus (contents of the general register specified by the R field) set the controls shown on this page. Refer to the output instruction on page 6-730.

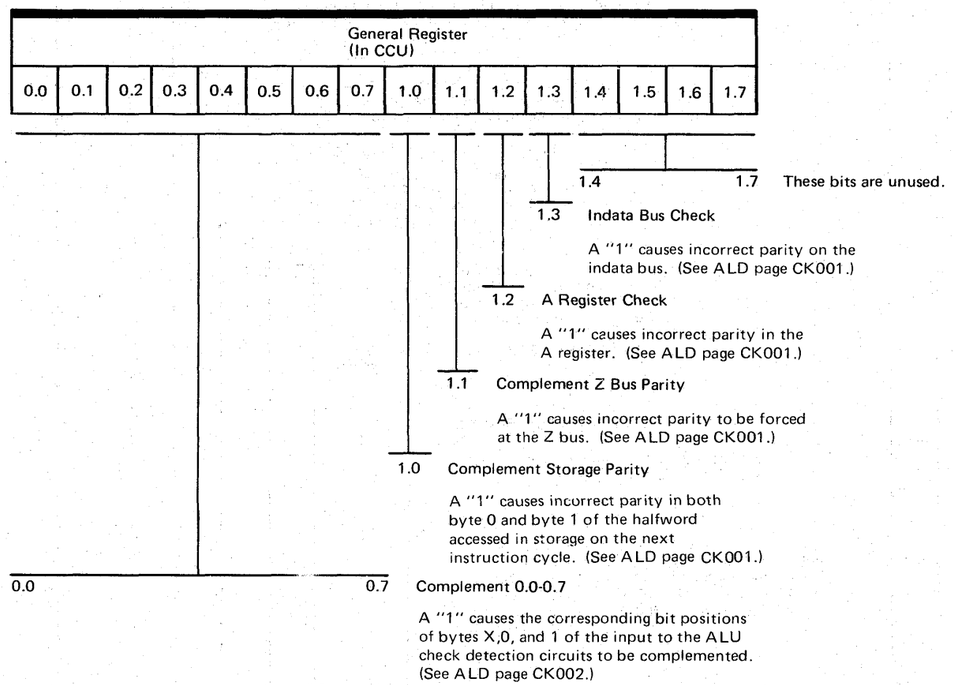
If a Remote Programer Loader is installed on a 3705-II, the ROS bootstrap program executes an Output X'77', after the load module has been successfully transferred, that resets the 'program initiated IPL' latch (GE102) if it was set.

OUTPUT X'78' FORCE CC CHECKS

Output X'78' provides a means for testing the CC check circuits under diagnostic control by forcing checks in the CCU data flow. This output is ignored if the CCU is not in test mode.

Note: You may have to take corrective action after using this output and store data with the correct parity in the affected register or storage location.

GENERAL REGISTER BIT DEFINITIONS



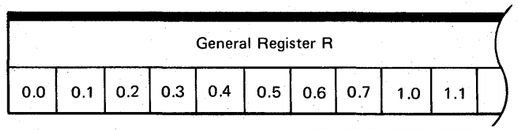
HARDWARE FUNCTION

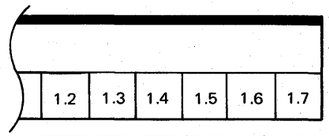
At I1D time, the contents of the Z bus (contents of the general register specified by the R field) cause the functions shown on this page. Refer to the output instruction on page 6-730.

OUTPUT X'79' UTILITY

Output X'79' sets or resets various CCU latches.

GENERAL REGISTER BIT DEFINITIONS





1.1 Reset Load Indicator

A "1" sets the 'load' latch that resets the LOAD light on the control panel to indicate that IPL is completed. The 'load' latch is reset and the LOAD light is turned on during IPL. (See ALD page CU006.)

1.0 Reset Check Stop Mode

A "1" resets 'ck stop mode' set during IPL phase 1 and allows the setting of 'mach ck set IPL'.
(See page 6-960 and ALD page CU006).

0.7 Program Level 5, Z Condition

If bit 0.5 of this output is "0", the 'Z condition' latch for program level 5 is set according to the state of this bit. (See ALD page CZ004.)

0.6 Program Level 5, C Condition

If bit 0.5 of this output is "0", the 'C condition' latch for program level 5 is set according to the state of this bit. (See ALD page CZ005.)

0.5 Inhibit Program Level 5, C and Z Replacement

If this bit is "0", the program level 5 'C and Z condition' latches are set according to bits 0.6 and 0.7. If this bit is "1", no action is taken (See ALD page CZ004.)

0.4 Remote Power Off

If the 3705 has the Remote Power Off feature (available only on a remote 3705), then Output X'79' with bit 0.4 on will power down the remote 3705.

0.3 Set FET Storage Diagnostic Mode

A "1" sets the 'allow set memory diag reg' latch. At the next 'store new' pulse, store bits for bytes 0 and 1 are set into the FET storage diagnostic registers. (See Page 7-240 for this sequence of operations.)

0.2 Set IPL

A "1" initiates an IPL. (See ALD page CU010.) A "1" also selects the ROS to be used as specified by output X'6B' and bit 0.4 if a Remote Program Loader is installed.

0.0 **0.1** These bits are unused.

1.7 Scope Sync Pulse 2

A "1" generates scope sync pulse 2. This is an oscilloscope synchronization pulse of 100 nsec that is used for maintenance purposes. (See ALD page CU015.)

1.6 Scope Sync Pulse 1

A "1" generates scope sync pulse 1. This is a scope synchronization pulse of 100 nsec that is used for maintenance purposes. (See ALD page CU015.)

1.5 Reset Bypass CCU Check Stop Mode

A "1" resets the bypass CCU check stop. This bit should not be on if bit 1.4 of this output is "1". It is ignored if the CCU is not in test mode. (See ALD page CU005.)

1.4 Set Bypass CCU Check Stop Mode

A "1" sets bypass CCU check stop. When this bit is set, operation is the same as if the DIAGNOSTIC CONTROL switch were in the BYPASS CCU CHECK STOP position. This bit should not be on if bit 1.5 of this output is "1". It is ignored if the CCU is not in test mode. (See ALD page CU005.)

1.3 Reset Test Mode

A "1" resets test mode. The TEST light of the control panel is turned off if the MODE SELECT and the DIAGNOSTIC CONTROL switches are in PROCESS. Any test functions allowed by test mode are also reset. This bit should not be on if bit 1.2 of this output is "1". (See ALD page CU005.)

1.2 Set Test Mode

A "1" places the CCU in test mode. This bit turns on the TEST light on the control panel and allows the following diagnostic functions to be performed:
a. Output X'78' Force CCU Checks
b. Set and reset diagnostic level 2.
c. Set and reset bypass CCU check stop.
d. Set and reset adapter level 1 interrupt request mask.

Note: Although the emulation program does not use X '79' bit 1.0, the Network Control Program does and will re-IPL and check point restart on a machine check.

HARDWARE FUNCTION

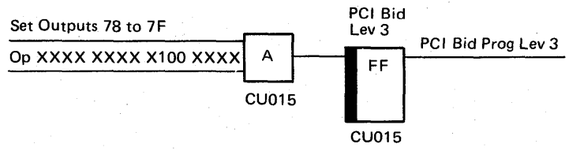
At I1D time, the contents of the Z bus (contents of the general register specified by the B register) cause the functions shown on this page. Refer to the output instruction of page 6-730.

OUTPUT X'7A' CYCLE UTILIZATION COUNTER RESET

When this instruction is issued, the bits in the Cycle Utilization Counter Register are reset to zero. The general register bits of the Output X'7A' instruction are ignored.

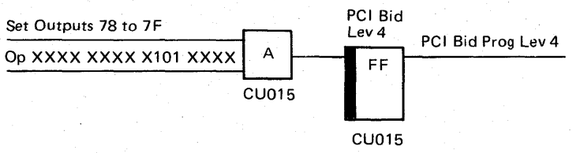
OUTPUT X'7C' SET PCI L3

Output X'7C' sets the program controlled interrupt request for level 3. Since this instruction performs a function, the bit settings of the register are ignored.



OUTPUT X'7D' SET PCI L4

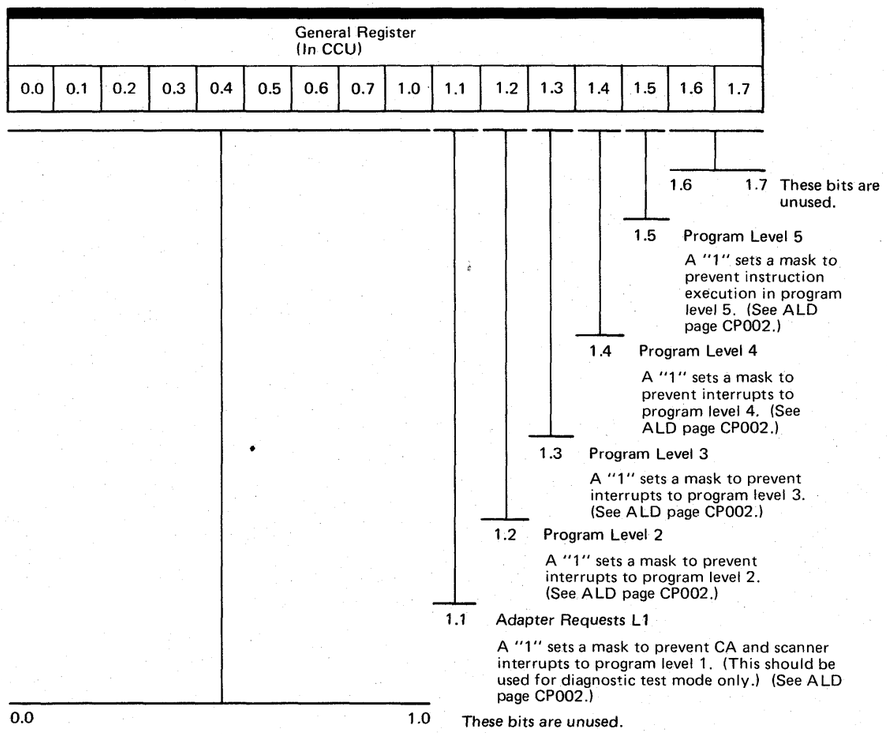
Output X'7D' sets the program controlled interrupt request for level 4. Since this instruction performs a function, the bit settings of the register are ignored.



OUTPUT X'7E' SET MASK BITS

Output X'7E' is used to set mask bits to prevent interrupts to certain program levels while processing.

GENERAL REGISTER BIT DEFINITIONS



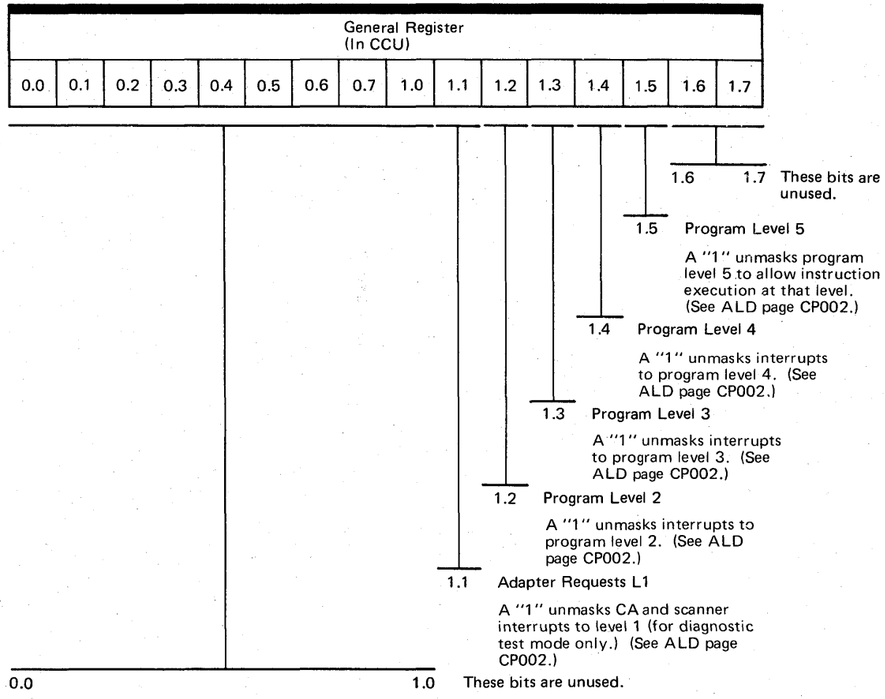
HARDWARE FUNCTION

At I1D time, the contents of the Z bus (contents of the general register specified by the R Field) cause the functions shown on this page. Refer to the output instruction on page 6-730.

OUTPUT X'7F' RESET MASK BITS

Output X'7F' is used to reset the mask bits for program level interrupts.

GENERAL REGISTER BIT DEFINITIONS



HARDWARE FUNCTION

At I1D time, the contents of the Z bus (contents of the general register specified by the R field) cause the functions shown on this page. Refer to the output instruction on page 6-730.

IPL

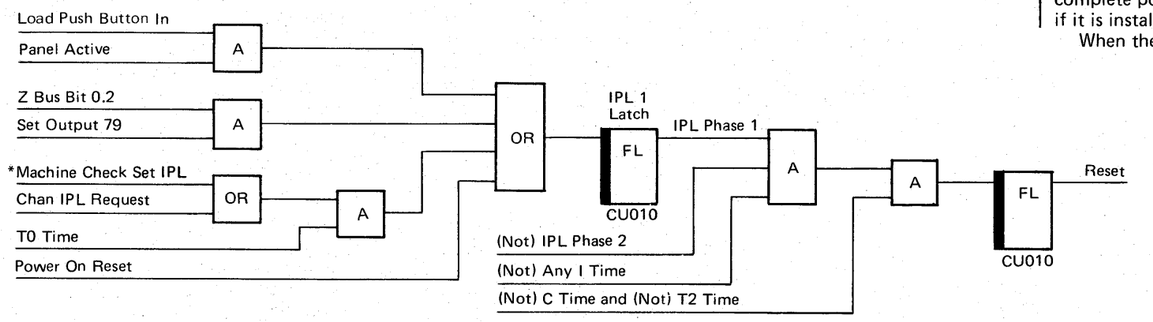
Initial program load (IPL) controls the loading of an initial program into the 3705.

Initializing an IPL operation causes a general reset of the 3705, automatic loading of a bootstrap program into storage from a read-only-storage (ROS) array, and finally passing of control to the bootstrap program. The bootstrap program (1) controls channel operations until the first load module from the host is successfully transferred into storage under a channel I/O Write IPL command or (2) controls remote-program-loader operations until the first load module from the host is successfully transferred into storage via the communication facility. After successful transfer of the first program segment into the 3705, the bootstrap program passes control to the loaded program segment which then controls the loading of whatever additional load modules are required to complete the 3705 control program load.

IPL is accomplished by successfully completing the three phases of the IPL operation.

Two lights in display B on the control panel indicate the three phases of IPL. The LOAD light on the control panel is turned on when the IPL is initiated, and is not turned off until phase three is completed, and the control program executes an Output X'79' with bit 1.1 on in the CCU general register designated by the R field.

IPL INITIALIZATION



*Refer to Output X '79' Bit 1.0 Page 6-930.

IPL PHASE 1

During IPL phase 1, the LOAD light turns on, and a general reset occurs in the 3705. The duration of the reset depends upon the duration of the action initiating the IPL. For example, if the LOAD push button is held in, the reset lasts until the push button is released.

The general reset:

1. Sets mask bits for program levels 2-5 and adapter level 1 requests.
2. Resets all interrupt entered latches.
3. Resets all CCU interrupt requests.
4. Resets PROGRAM STOP and HARD STOP.
5. Discontinues instruction execution.
6. Disables storage protection.
7. Turns on the control panel TEST light.

Minimal reset occurs in the channel adapters unless the IPL is the result of a power-on-reset. The RESET switch completely resets the channel adapters and makes an IPL necessary. A complete power-on-reset occurs in the remote program loader if it is installed.

When the phase 1 reset ends, phase 2 begins.

Summary of IPL Phase 1 Resets.

Logic Page	Card Location	Function
CC004	B3Q2	Inhibit I Cycles
CL005	B3K2	Condition LS Write
CM001	B4C2	Inhibit Storage Operations
CP001	B3T4	Inhibit Allow Instructions
CP002	B3M2	Mask Interrupt Levels
CP003	B3M2	Reset Interrupt Entered Latches
CS002	B3F2	Conditions Set SDR byte X, 0, and 1 Inhibit Set Bad Addr
CS003	B3F2	Condition TAR Set
CS004	B3F2	Gate CCU Indata to Y bus Gate TAR to Y bus
CS007	B3F2	Set Op Reg
CU004	B3P2	Reset Address Compare Reset Program Stop
CU005	B3L2	Set Test Mode Reset BP Ck Stp Mode
CU007	B3P2	Reset Clock Step Reset Start, Display,Store
CU014	B3L2	Reset PCI Bid Lev 2 Reset Addr Exception Reset Allow Irpt Reset Interrupt Key
CU015	B3M2	Reset PCI Bid Lev 3 Reset PCI Bid Lev 4 Reset Svc Bid Lev 4
CV061	B4D2	Inhibit Storage Protection
CX002	B3D2	Priority Register Occupied Latches

IPL (PART 2)

IPL PHASE 2

During IPL phase 2, the ROS bootstrap program is automatically loaded into storage sequentially from location X '00000'. Different ROS arrays are installed in the 3705 depending upon which type channel adapter is installed or, in the case of the remote 3705-II, whether the remote program loader is installed with or without channel adapters. (See 2-000 for all ROS arrays types.) In any case the CA1, CA2, Dual CA, N CA, RPL for 3705-I ROS array is mounted on an MST card and is plugged into the socket at 01A-B4F2 (see logic page CW011 and CW012) while the Remote Program Loader II, ROS array card is plugged into the socket at 01A-B4F4 (see logic page CW001).

The bootstrap program code is unique to the particular type ROS, and a listing of the code is contained in the logic pages beginning on ALD CW101.

Note: See page 1-200 for a procedure to clock step thru IPL phase 2.

PHASE 2 DATA FLOW

At the beginning of IPL phase 2, SAR and TAR contain all 0s. Cycle steal cycles are used to load the ROS bootstrap program into storage.

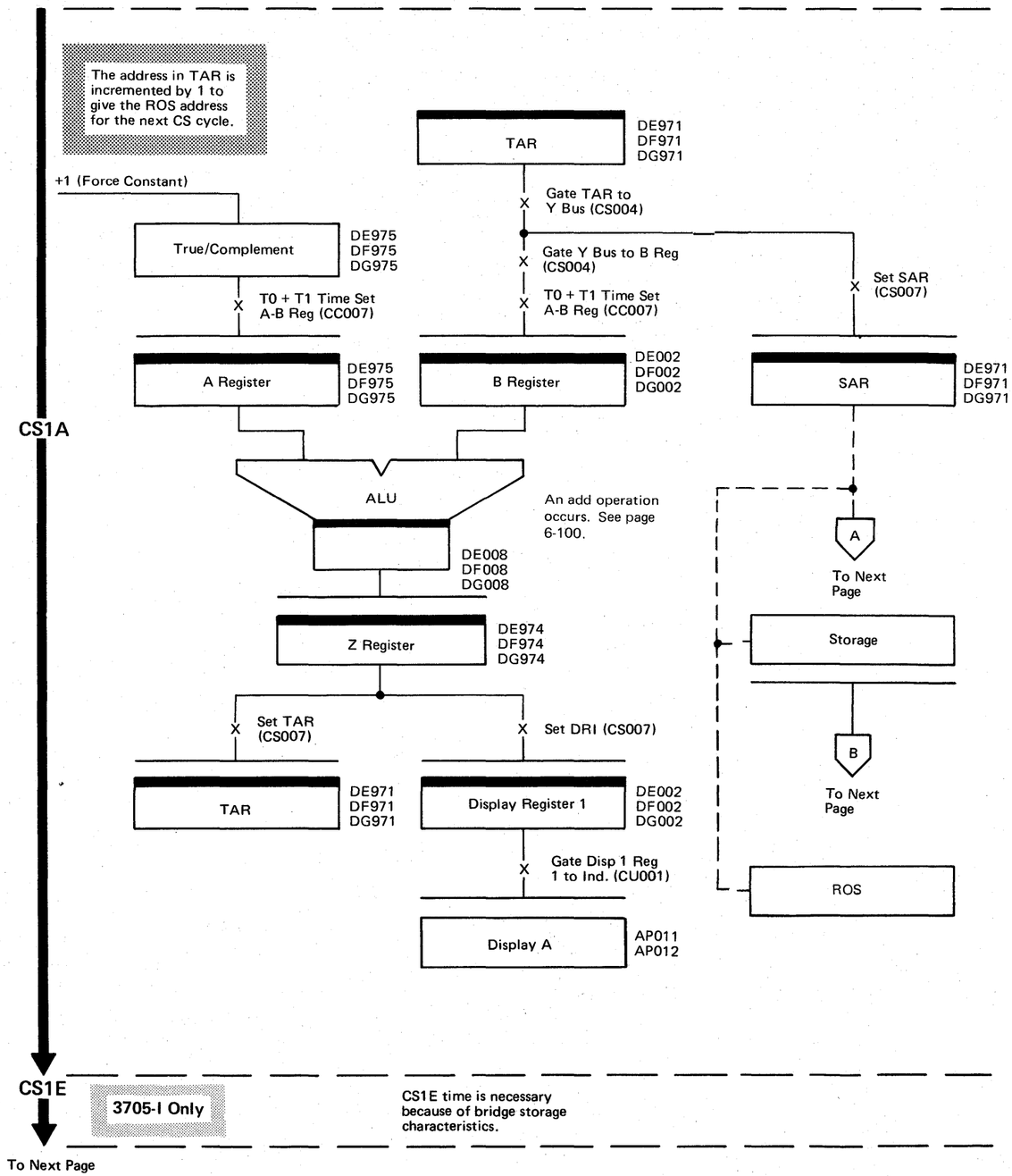
SAR addresses both storage and ROS. ROS is addressed on a byte level. During each cycle steal cycle, the ROS data is placed in byte 1 of the 'indata' bus.

The first cycle steal cycle in IPL phase 2 stores the first byte of ROS data in byte 0 of the first storage location. (A 'cross lo to hi' operation places the ROS data in both bytes 0 and 1. Because SAR bit 1.7 is 0, 'ROS byte 0' and zeros in byte 1 are gated to SDR and loaded into storage.)

The second cycle steal cycle stores the second byte of ROS data in byte 1 of the first storage location. (Because SAR bit 1.7 is 1, 'ROS byte 0, from the store read cycle, and 'ROS byte 1' are gated to SDR and loaded into storage.)

The cycle steal operations continue until all of the ROS bootstrap program is loaded. The following data flow charts and pages 6-963 or 6-964 show the ROS bootstrap cycle steal operations.

Note: Refer to page CW000 for a list of ROS program code, simulation run, and ROS flow charts.



From Preceding Page

During the read portion of the storage cycle, storage sends the data from the storage location addressed by SAR to the CCU. SAR bit 1.7 determines whether byte 0 or byte 1 is gated to the SDR. The byte of ROS data in the ROS location addressed by SAR is gated to 'indata bus' byte 1. The ROS data is duplicated in both bytes of the Z register by the ALU. SAR bit 1.7 determines whether byte 0 or byte 1 is gated to SDR. The contents of SDR are then stored in the storage location addressed by SAR.

CS1B

ROS

X Gate CCU Indata to Y Bus (CS004)

X Gate Y Bus to B Reg (CS004)

X T0 + T1 Time Set A-B Reg (CC007)

Byte 1

B Register — DE002 DF002 DG002

Byte 1

ALU — DE008 DF008 DG008

A "cross lo to hi" operation occurs. See page 6-100.

From Preceding Page B

Z Register — DE974 DF974 DG974

X If SAR 1.7 = 0: Gate Byte 1 to M Bus (CS005) If SAR 1.7 = 1: Gate Byte 0 to M Bus (CS005)

X If SAR 1.7 = 0: Gate Z Bus Byte 0 to M Bus (CS005) If SAR 1.7 = 1: Gate Z Bus Byte 1 to M Bus (CS005)

X Set SDR Byte (CS007)

From Preceding Page A

SDR — DN001

1

Storage

The byte of ROS data is only seen in Display B during a clock step operation.

X Set DR 2 (CS007)

Display Register 2 — DE003 DF003 DG003

X Gate Displ Reg 2 to ind. (CU001)

Display B — AP011 AP012

CS1F

3705-I Only

CS1F time is necessary because of bridge storage characteristics.

To Next Column

CS1C

No Action

CS1D

The contents of SDR are displayed in display B.

1

X Gate SDR Bits to A Bus (CF003)

True/Complement — DE975 DF975 DG975

X T0 + T1 Time Set A-B Regs (CC007)

A Register — DE975 DF975 DG975

ALU — DE008 DF008 DG008

An A register direct operation occurs. See page 6-100.

Z Register — DE974 DF974 DG974

X Set DR 2 (CS007)

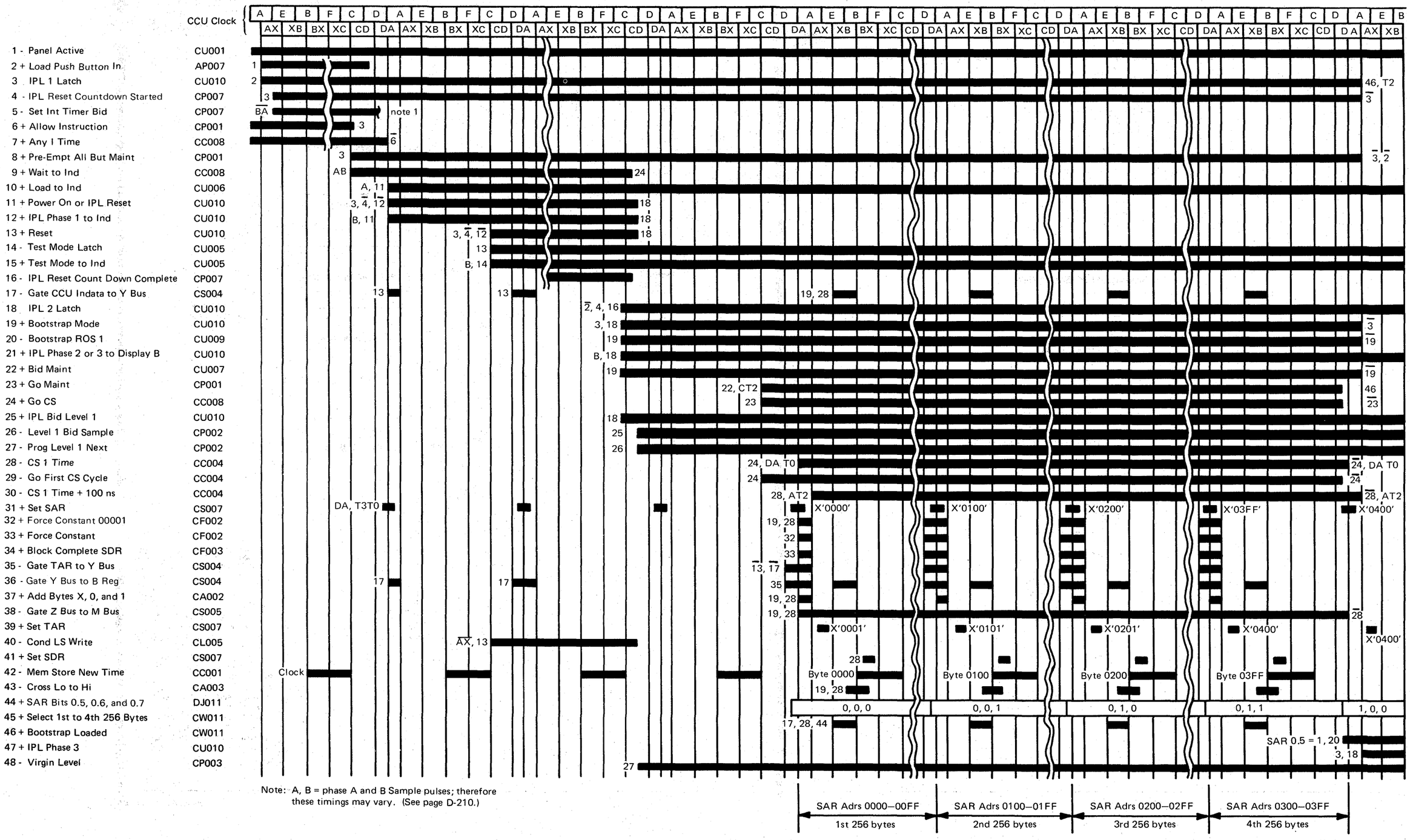
Display Register 2 — DE003 DF003 DG003

X Gate Displ Reg 2 to Ind. (CU001)

Display B — AP011 AP012

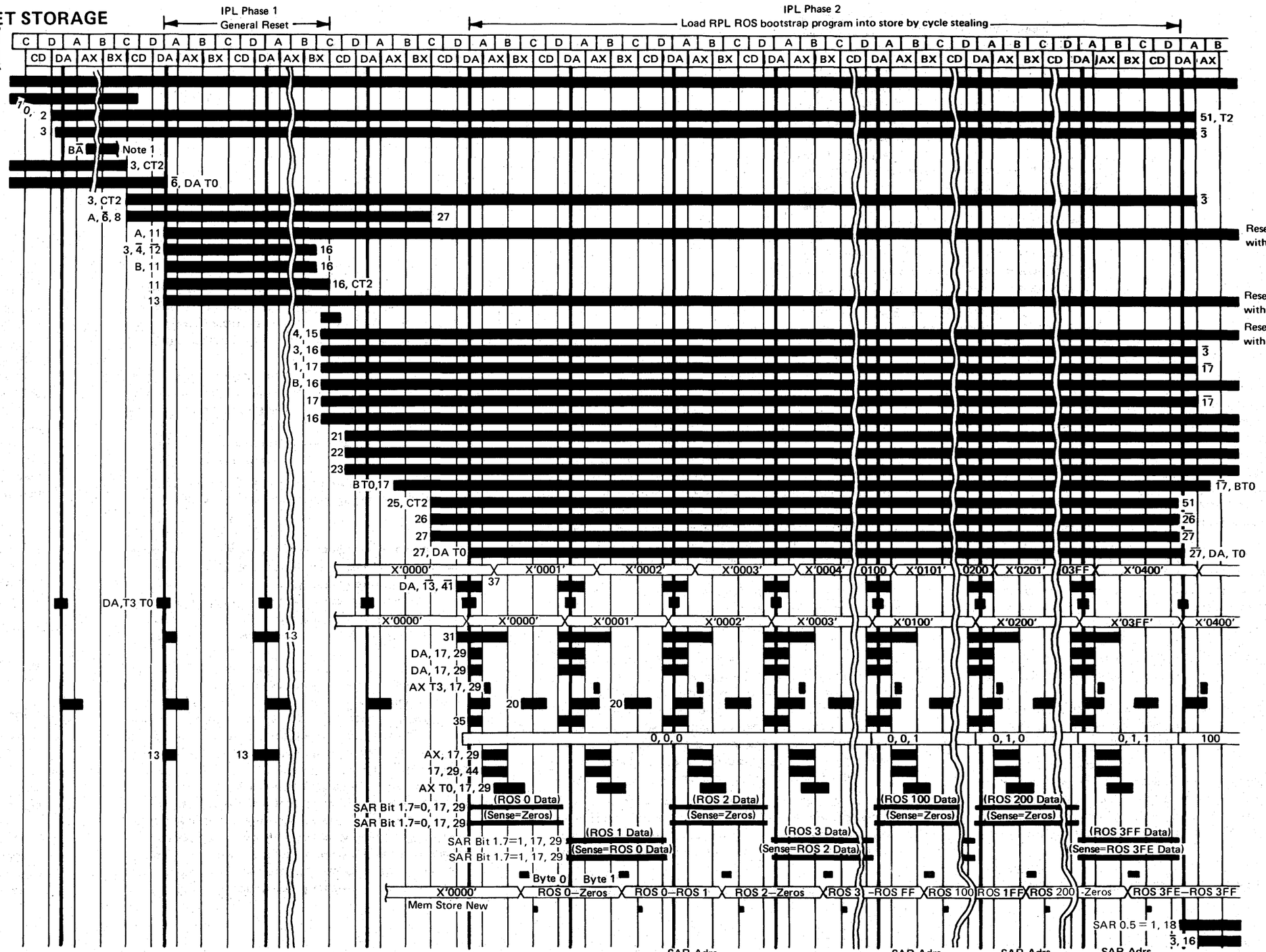
The CCU takes CS cycles until all of ROS is placed in storage.

IPL PHASE 1 AND 2 TIMING — BRIDGE STORAGE



Note: A, B = phase A and B Sample pulses; therefore these timings may vary. (See page D-210.)

IPL PHASE 1 AND 2 TIMING — FET STORAGE



Notes: 1. A B = Phase A and B Sample pulses; therefore these timings may vary. (See page D-210.)

2. The IPL 1 latch can also be set by the conditions shown in the second-level diagram on page 6-961.

3. See Page 1-200 for a procedure to clock step thru IPL phase 2.

IPL PHASE 3

ROS bootstrap program execution begins with an interrupt to program level 1, and the program is executed entirely at this level. The instruction at storage location X'00010' is the first instruction to be executed. (The branch to storage address X'00010' is hardware forced at the start of IPL phase 3.) Refer to logic page CW000 for the listing of the ROS bootstrap program, ROS flow charts, ROS code, and simulation run.

The first section of the program:

1. Saves the general registers for group 0 starting in location X'00780'.
2. Verifies the operation of the 3705 instructions needed by the second part of the bootstrap program; see 2-000, 2-040, 2-080, or 2-120.
3. Tests to determine whether to continue or branch to the ROS bootstrap escape address X'06FC'.
4. If the branch is not taken, saves external registers X'76', X'7D', and X'7E' starting at storage location X'00702'.

The TEST light turns off on the control panel after the first part of the test is complete.

The second part of the ROS bootstrap program controls channel adapter or remote program loader operations until the first program load module is successfully transferred from the host. If there is no command pending for completion or final status in the CA, the ROS bootstrap program has the CA generate an asynchronous status of Device End (DE) and Unit Check (UC). If a command other than a Write IPL is pending completion, the CA generates a final status of Device End, Unit Check, and Channel End (CE) if CE has not already been generated. In either case, Not Initialized (sense bit 6) is made available for a subsequent channel Sense command. A Write IPL normally follows the channel Sense command. See the *3704 and 3705 Communications Controllers Remote Program Loader Theory—Maintenance,* SY27-0135, for a description of the remote program loader IPL.

The Write IPL command allows the transfer of the first load module from the host CPU into the 3705. Under the Write IPL command, the load module is stored in sequential storage locations starting at location X'00400'. The maximum size of this load module cannot exceed 768 bytes. When this transfer is successfully completed, the ROS bootstrap program executes an Output X'77', with bit 0.0 on in the general register, to reset the IPL 2 latch, the IPL level 1 interrupt request, and the IPL PHASE lights. The ROS bootstrap program turns control over to the program module just loaded by branching to location X'00404'. The first two halfwords transferred in the load module must contain the IPL source identification and the total number of bytes in the load module in that order:

The IPL operation is complete when the IPL level 1 interrupt request is reset and the IPL PHASE lights turn off. However, the LOAD and TEST lights remain on until an Output X'79' resets them with bits 1.1 and 1.3 on respectively in the general register. When the 3705 is completely loaded, the loaded program should execute this instruction.

The IPL completion point in the ROS boostrap program may not be reached because of one of the following:

1. A CC check hardstop
2. Improper instruction test operation
3. Program continuity check
4. Channel adapter disabled
5. Channel adapter malfunction
6. IPL count transfer check

In this case, the ROS bootstrap program either hard-stops or loops and executes a program display function to try to identify the IPL status. See *ROS Testing,* 2-000, 2-040, 2-080, or 2-120.

IPL PHASE 3 WITH TYPE 1 OR TYPE 4 CHANNEL ADAPTER

Unless the IPL sequence is started by a power on sequence, the state of the type 1 or type 4 CA is not affected by the reset performed in IPL phase 1. Therefore, the ROS bootstrap program must handle the following conditions:

1. Channel Interface disabled. The bootstrap program executes Output X'67' with bit 1.4 on in the CCU general register to allow the interface to become enabled. The program loops until the interface becomes enabled.
2. Channel interface enabled. The bootstrap program tests to determine whether or not the native subchannel (NSC) is active with a channel command. Then one of the following actions occurs:
   a. If no command is in progress, the bootstrap program signals the type 1 or type 4 CA to send DE, UC status. When this status transfer is complete, the CA program loops, waiting for an initial selection level 3 interrupt request. When the interrupt request is detected, the bootstrap program responds as described in the type 1 channel adapter section of this manual; see 8-140.
   b. If a command is in progress, the bootstrap program signals the CA to end the command with CE, DE, UC status. When this status is successfully transferred, the bootstrap program loops waiting for a type 1 or type 4 CA initial selection level 3 interrupt request. The bootstrap program responds to the interrupt request as described in the type 1 channel adapter section of this manual; see 8-140.

IPL PHASE 3 WITH TYPE 2 OR TYPE 3 CHANNEL ADAPTER

Unless the IPL sequence is initiated as a result of a power on sequence, the state of the type 2 or type 3 CA is not affected by the reset performed in IPL phase 1. Therefore, the type 2 or type 3 CA bootstrap program must be capable of performing the following:

1. The bootstrap program requests a level 3 interrupt and loops until the interrupt occurs.
2. The bootstrap program loops until the interface becomes enabled.
3. If the channel interface is enabled and no command is in progress, the bootstrap program determines that no command was in progress when the level 3 interrupt occurred and signals the CA to send DE and UC status to the host CPU. Not initialized is set in the sense register and made available to a subsequent channel Sense command. The bootstrap program loops until a level 3 interrupt from the CA signals that a Write IPL command has been received.
4. If the channel interface is enabled and a command is in progress, the bootstrap program signals the CA to end the command with CE, DE, and UC status if the command is not a channel Write IPL command. If the command is a channel Write IPL, a level 3 interrupt is requested to signal the bootstrap program that the command is a Write IPL. The bootstrap program responds as described in the *Type 2 Channel Adapter* Section of this manual; see 9-310.

SPECIAL STATUS CONDITIONS TO HANDLE DUAL CHANNEL IPL CONTENTION:

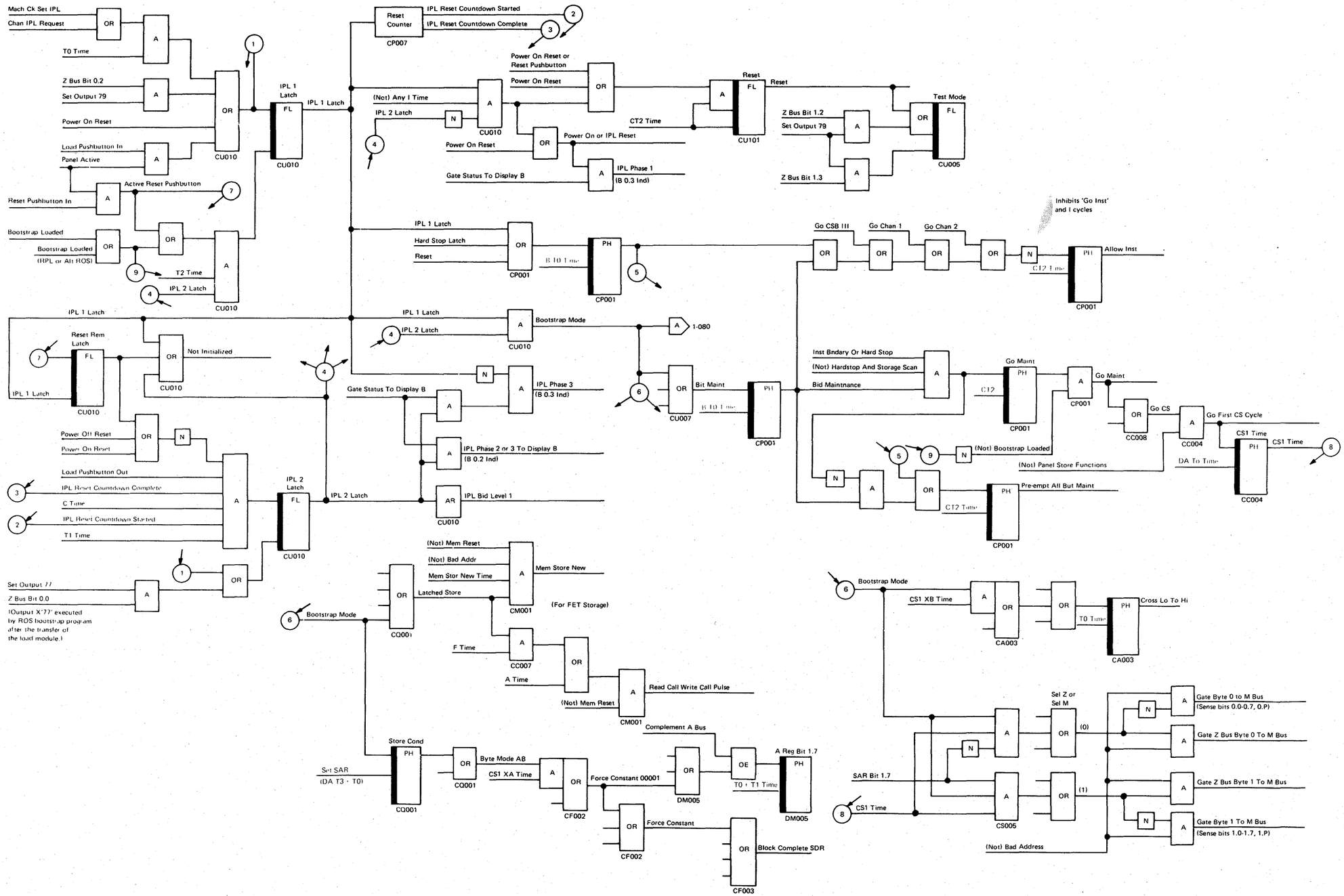
When an IPL has been started on one channel, a sense command issued by the other channel will receive an initial status of Unit Exception from a type 2 or type 3 CA.

With Dual-ROS and a type 1 or 4 CA, two status sequences are possible for a Sense command:
(1) With Models J-L or Models A-H with E.C. 319139, a CA 1 or 4 will present a sense byte and give final status of CE, DE, and UE.
(2) With 3705 Models A-H without E.C. 319139, the CA 1 or 4 will present final status of CE, DE, and UE without presenting the sense byte.

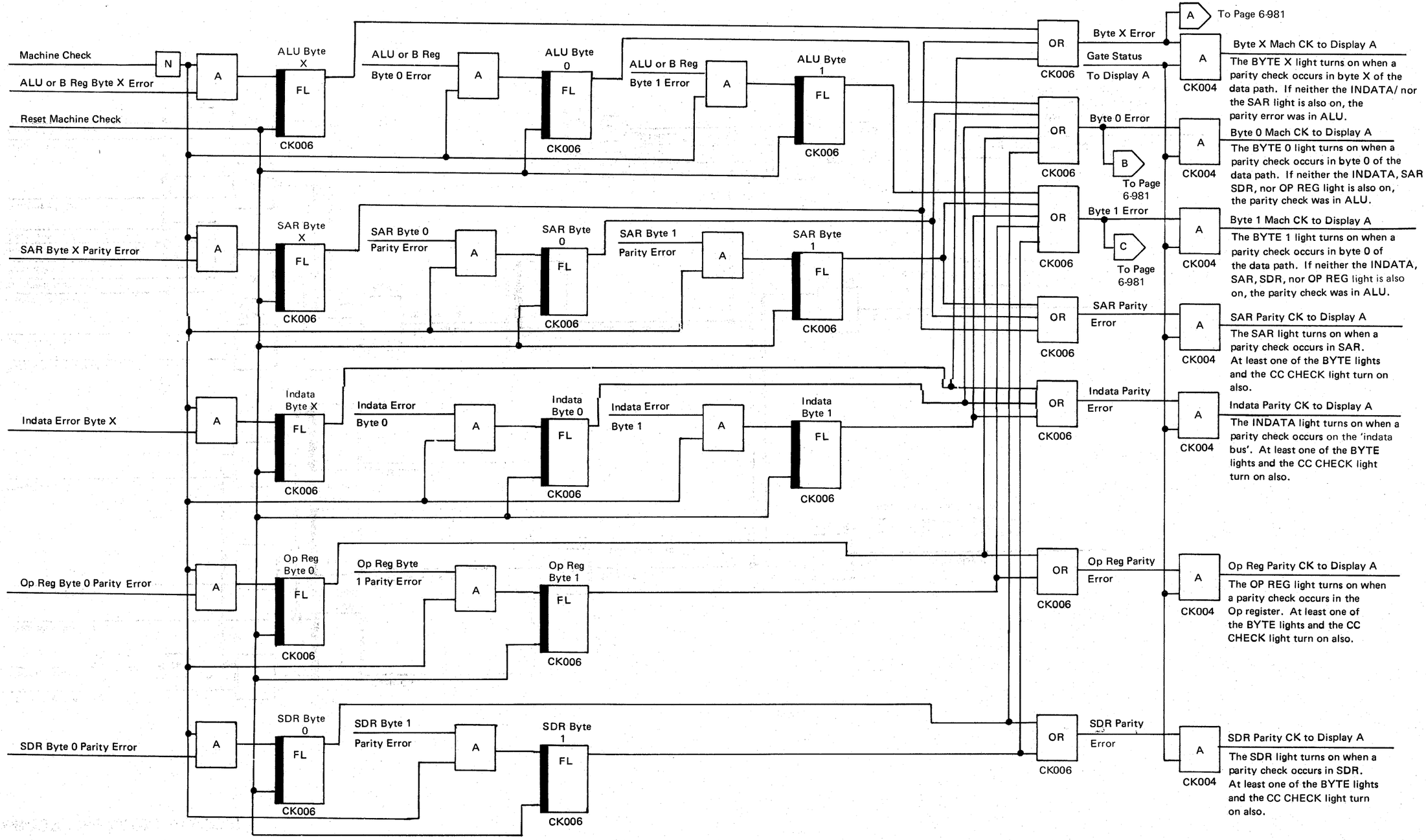
Note: With N-ROS, a Type 4 CA presents a sense byte followed by a final status of CE, DE, and UE.

An IPL on one channel will end with Channel End, Device End and Unit Check when overridden by an IPL on the other channel.

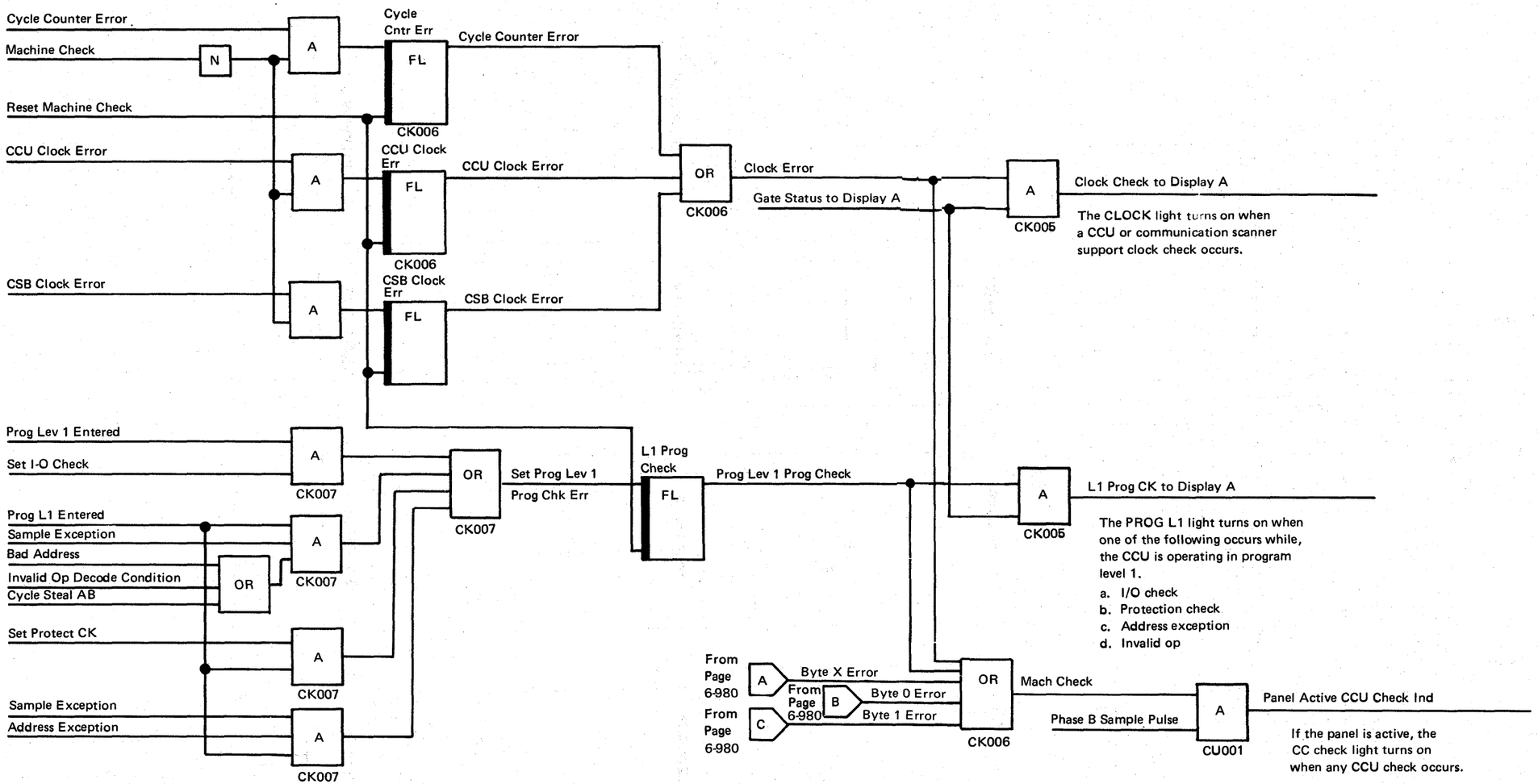
IPL DATA FLOW



ERROR CHECKING



ERROR CHECKING (PART 2)



BRIDGE STORAGE MODULE

3705-I BRIDGE STORAGE

The Bridge Storage Module (BSM) is a ferrite core storage unit. The 3705 uses a 16K (8K-18 bits addressing scheme) BSM as the basic storage unit. A 32K (16K-18 bits addressing scheme) BSM can be chained to the 16K BSM to make a total of 48K in the first frame. An additional 64K can be installed in 32K increments in each expansion module for a total storage capacity of 240K.

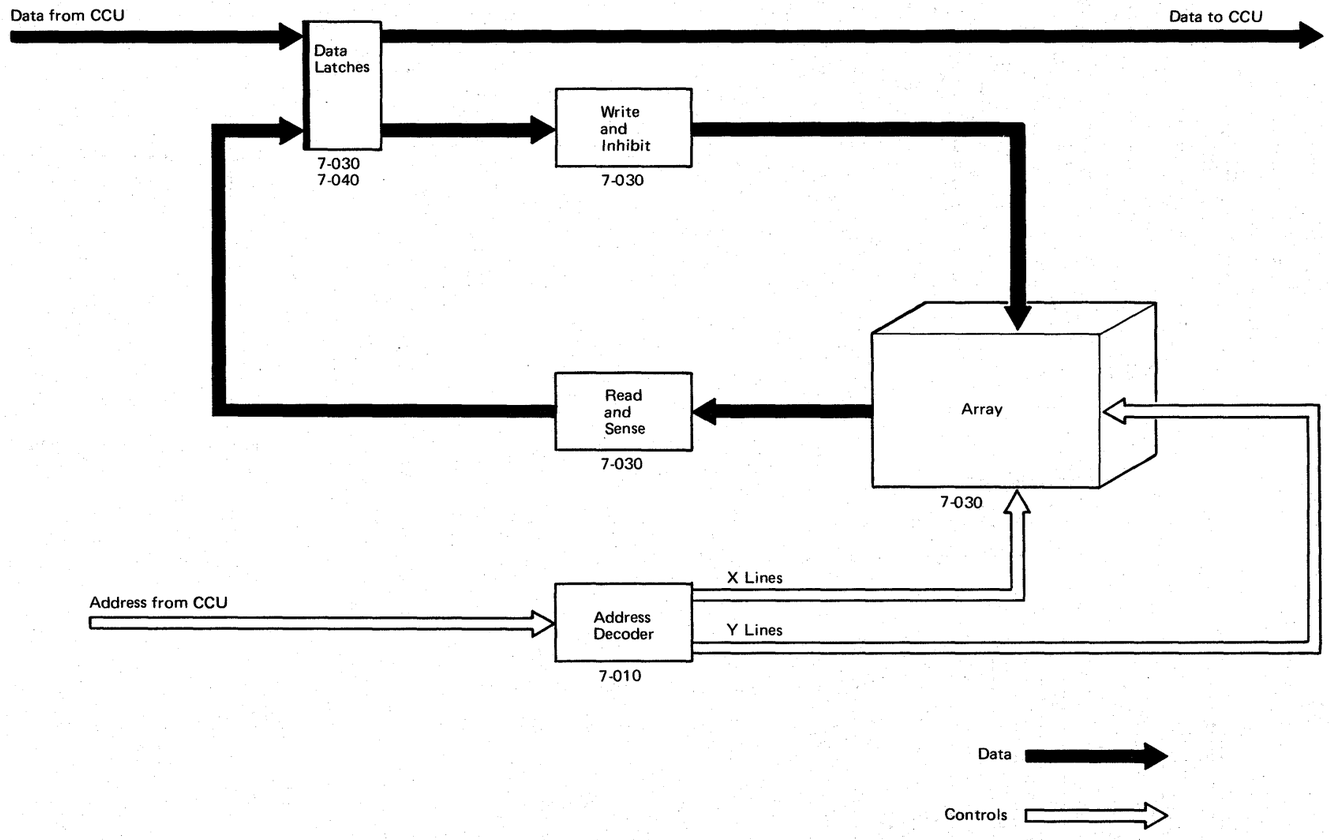
To chain two BSMs, cables are added between the BSMs, and the terminators are moved to the last BSM. The outputs of the data latches in the high-order BSM are DOT-ORed to the outputs of the low-order BSM data latches.

The BSM is a separately packaged unit that mounts in the space provided for an MST-1 board. It contains the core array, timing and control circuits, a drive system, a sense/inhibit system, and a set of data latches. The BSM does not contain a 'storage address' register (SAR).

Note: The CCU reads and writes even parity to and from storage but uses odd parity checking in the CCU when transfering data.

The central control unit (CCU) communicates with the BSM through interface lines that transfer addresses, data, and control signals. Interface signals are compatible with MST-1 circuit technology, but the BSM uses some SLT circuits internally.

Each storage cycle takes a minimum of 1200 nsec and contains a read cycle and a write cycle. (Storage has a destructive readout.) During the write cycle, either the old data is regenerated or new data is stored.



ADDRESSING

3705-I BRIDGE STORAGE

Each address selects 16 data bits and two parity bits (two cores in each of the 9 planes).

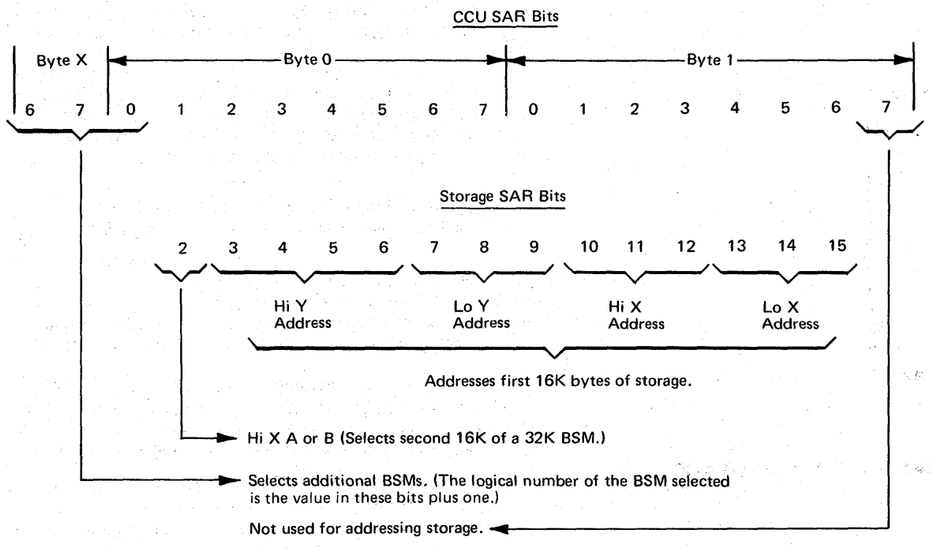
The direction of the currents in the crossing X drive, Y drive, and sense lines determines whether a '0' or a '1' is read from, or written into a core.

The SAR bits control the current in the X and Y lines.

Note: In any storage configuration, the 16K BSM is always the last logical BSM.

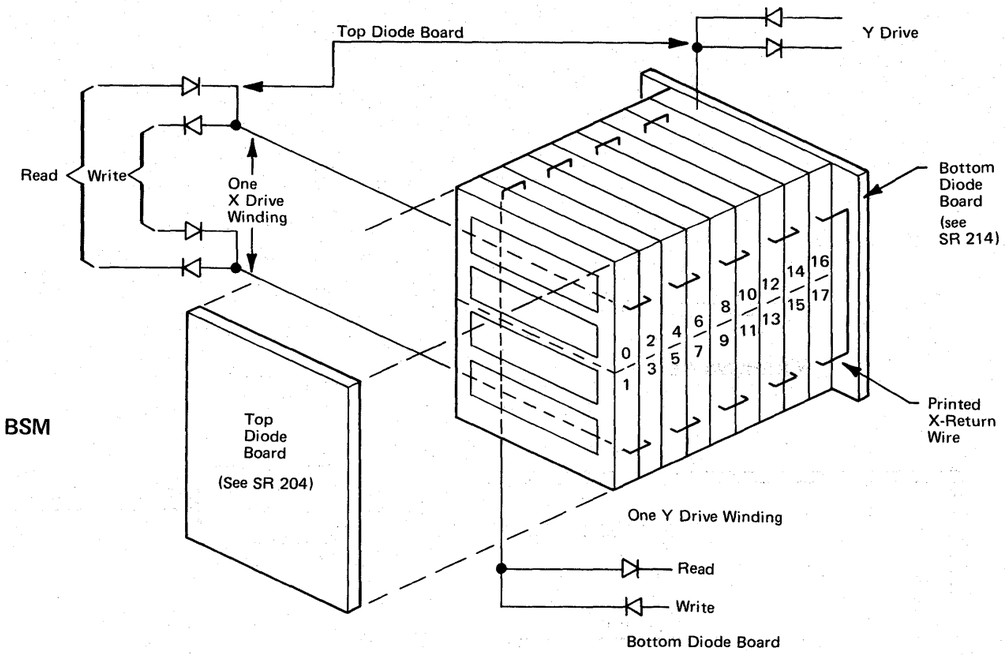
With a 16K BSM, the cards at W1D2 and W1E2 control all the X lines. The cards at W1F2, W1G2, and W1H2 control all the Y lines. These cards can be swapped to isolate problems.

With a 32K BSM, the cards at W1D2, W1E2, and W1F2 control all the X lines. The cards at W1G2, W1H2, and W1J2 control all the Y lines. These cards can be swapped to isolate problems.

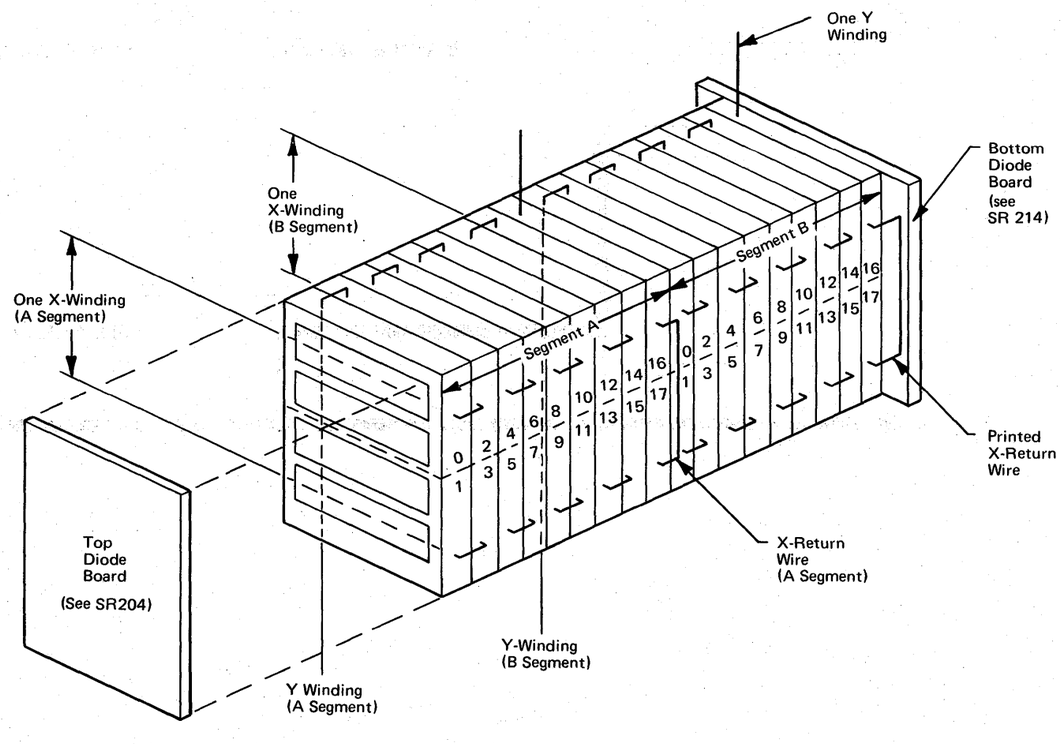


Part of Address	Cards	
	32K BSM	16K BSM
Lo X	W1D2	W1D2
Hi X	W1E2, W1F2	W1E2
Lo Y	W1G2	W1F2
Hi Y	W1H2, W1J2	W1G2

16K BSM



32K BSM



X AND Y DRIVE SYSTEM AND TIMING FOR ADDRESSING

3705-I BRIDGE STORAGE

The X and Y drive system uses:

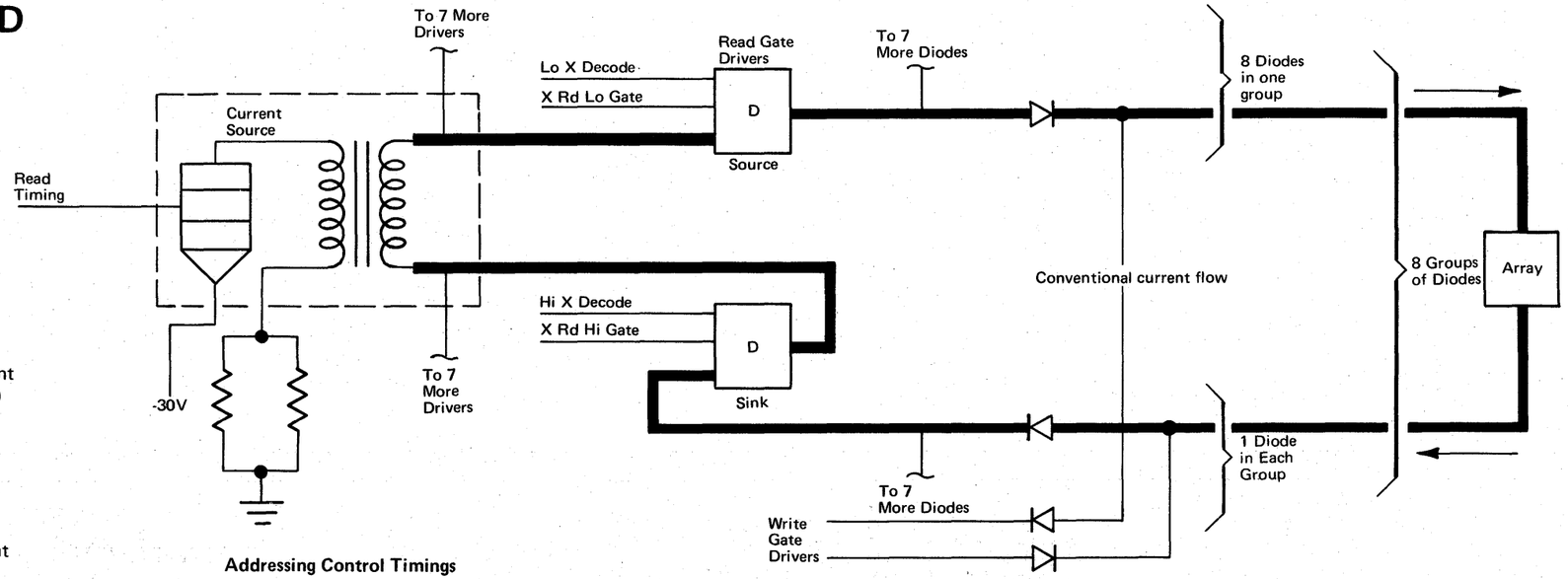
- Current sources
- A gate and selection system

Current Sources

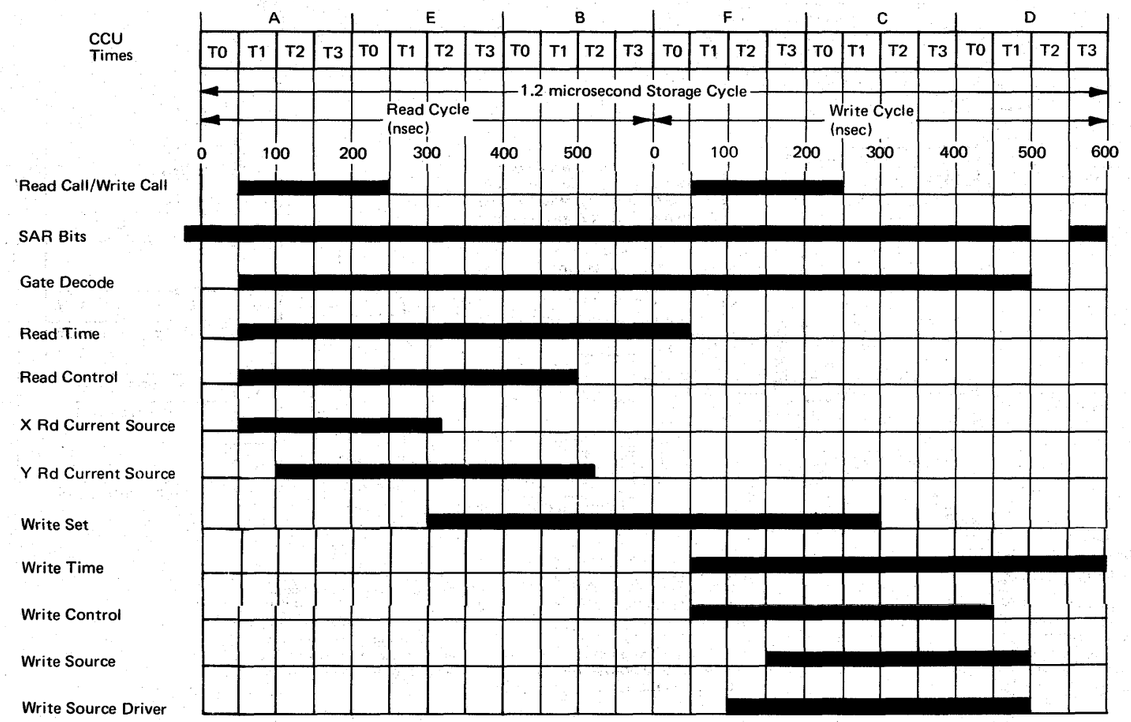
Current sources supply drive current to the X and Y windings. There are four current sources in the BSM that are packaged on the W1K2 card: X read, X write, Y read, and Y write. Each current source consists of a transformer secondary, the primary of which is driven by a transistor controlled by cycle timing. The transformer secondary is also the sink for the drive current.

Gate and Selection System

The gate and selection system directs drive current to a single X-line and a single Y-line. The gate and selection system operates as a switch at each end of the drive lines to direct the current source drive current to a single drive line. Address decoders select a pair of 'gate drivers' for X and a pair for Y during the read cycle. During the write cycle, four different drivers are selected in addition to the X write current source and the Y write current source. These drivers, in conjunction with diodes in the drive lines to the array, direct the current in the reverse direction through the same X and Y lines.



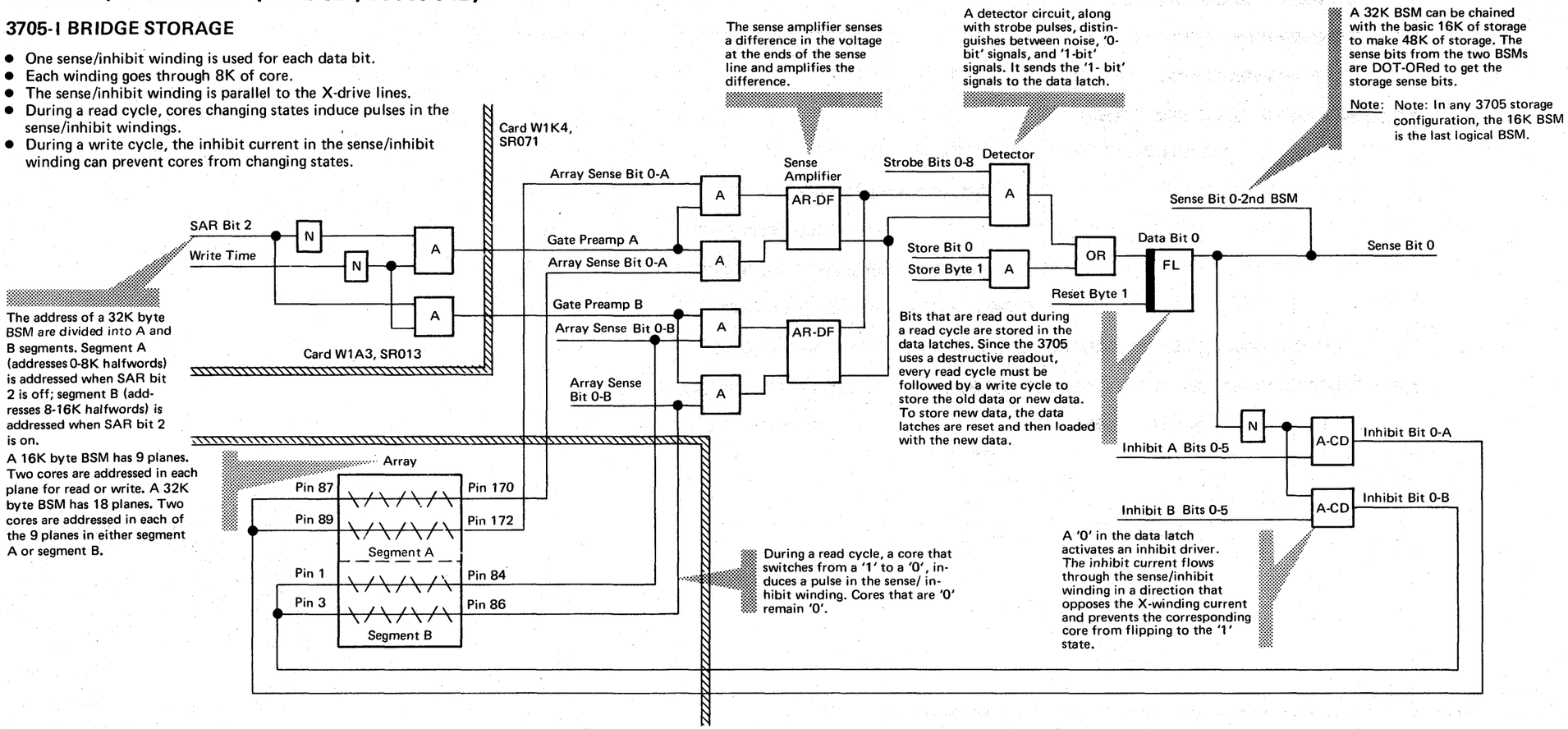
Addressing Control Timings



SENSE/INHIBIT (READ/WRITE)

3705-I BRIDGE STORAGE

- One sense/inhibit winding is used for each data bit.
- Each winding goes through 8K of core.
- The sense/inhibit winding is parallel to the X-drive lines.
- During a read cycle, cores changing states induce pulses in the sense/inhibit windings.
- During a write cycle, the inhibit current in the sense/inhibit winding can prevent cores from changing states.



SENSE/INHIBIT (READ/WRITE) 16K

3705-I BRIDGE STORAGE

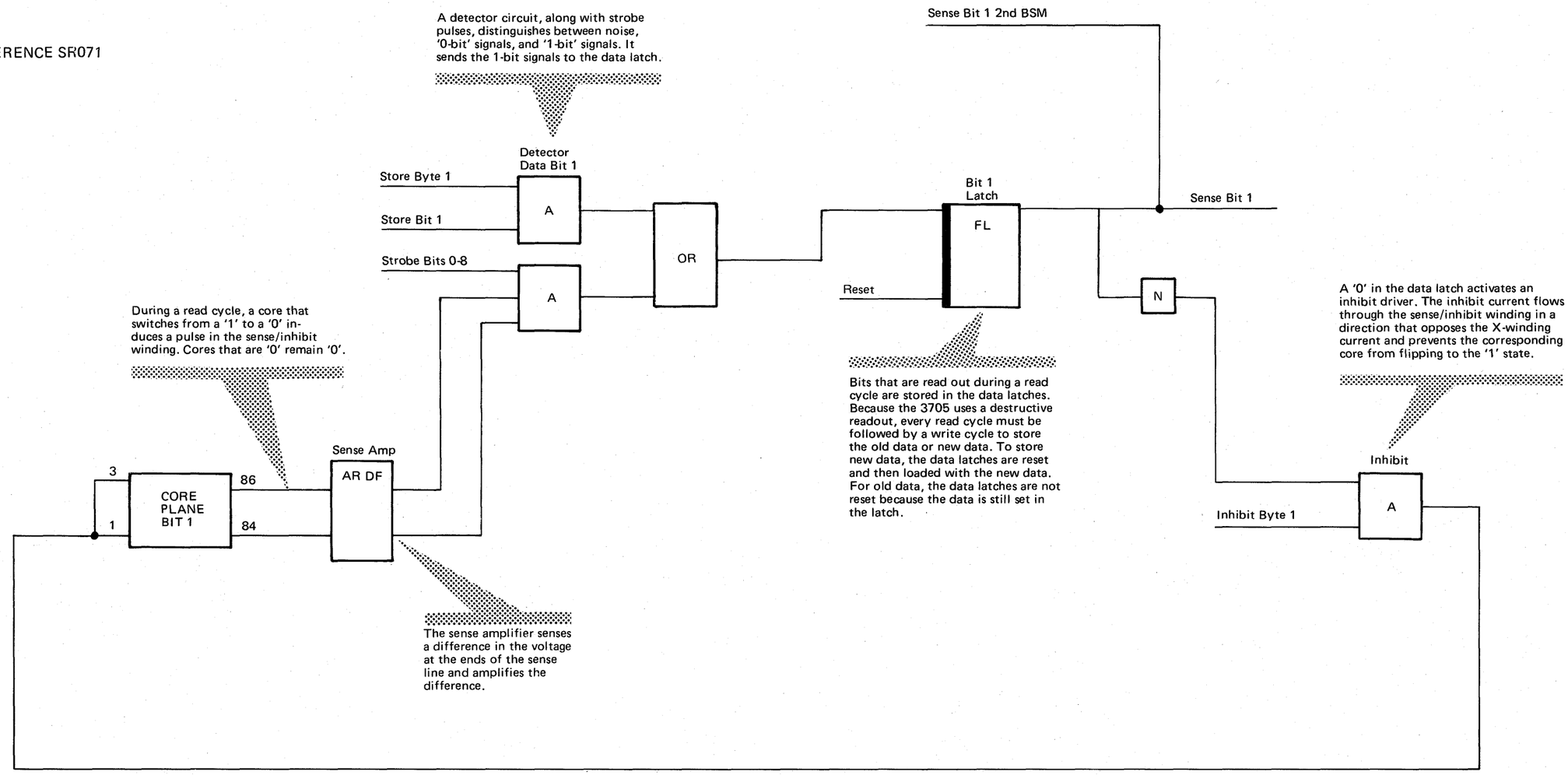
- One sense/inhibit winding is used for each data bit position, and goes through 8K of storage addresses.
- The sense/inhibit winding is parallel to the X-drive lines.
- During a read cycle, cores changing states induce pulses in the sense/inhibit windings.
- During a write cycle, the inhibit current in the sense/inhibit winding can prevent cores from changing states.

5 LOGIC REFERENCE SR071

A 32K BSM can be chained with the basic 16K of storage to make 48K of storage. The sense bits from the two BSMs are DOT-ORed to get the storage sense bits.

Note: In any storage configuration, the 16K BSM is the last logical BSM.

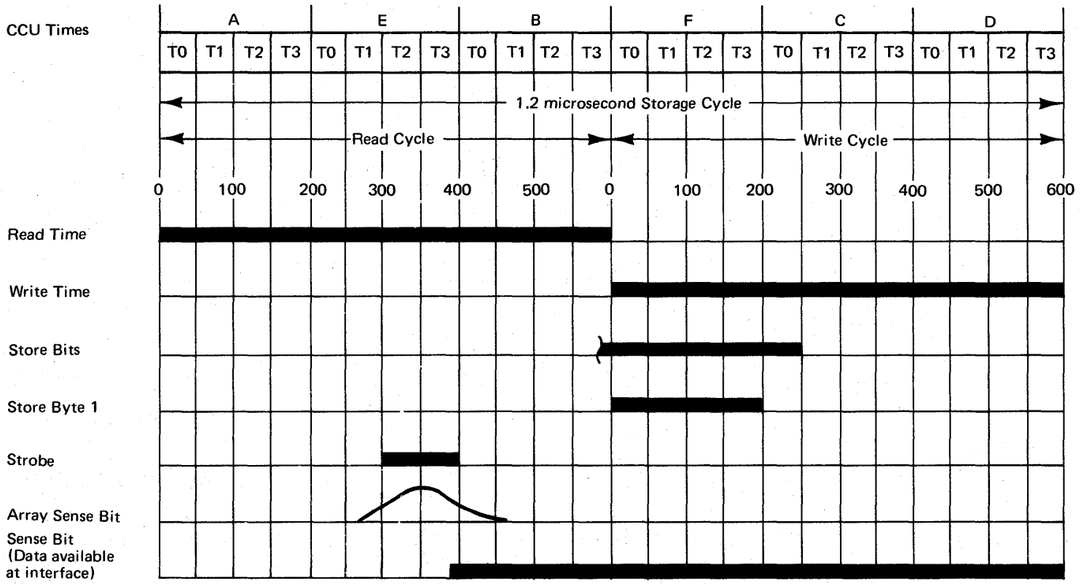
A detector circuit, along with strobe pulses, distinguishes between noise, '0-bit' signals, and '1-bit' signals. It sends the 1-bit signals to the data latch.



STO

READ/WRITE TIMING

3705-I BRIDGE STORAGE



SDR SENSE BITS

If a consistent error occurs in an SDR bit for data coming from storage, use the following chart to determine what card to replace.

Storage Sense Bit	SDR Bits Failing	Suspected Card to Replace	
		16K	32K
0	0.0	W1J4	W1K4
1	0.1	W1J4	W1K4
2	0.2	W1J4	W1J4
3	0.3	W1H4	W1J4
4	0.4	W1H4	W1H4
5	0.5	W1H4	W1H4
6	0.6	W1G4	W1G4
7	0.7	W1G4	W1G4
8	Pty Byte 0	W1G4	W1F4
9	1.0	W1F4	W1F4
10	1.1	W1F4	W1E4
11	1.2	W1F4	W1E4
12	1.3	W1E4	W1D4
13	1.4	W1E4	W1D4
14	1.5	W1E4	W1C4
15	1.6	W1D4	W1C4
16	1.7	W1D4	W1B4
17	Pty Byte 1	W1D4	W1B4

SENSE/INHIBIT SCOPING PROCEDURES

3705-I BRIDGE STORAGE

Use 1X probes when scoping the array. When large signal levels occur, the input amplifiers of the scope may saturate and distort the wave shape. High noise spikes also occur when the BSM writes bits in positions other than the one being scoped. This is not an error condition.

Because of the small signal level and the high noise level, ground each probe with a short lead (preferable 6 inches or less) when you display array sense bits. Keep the leads away from the XYZ resistors while scoping because the leads can pick up noise from these resistors.

SENSE BIT SCOPING OF ALL ADDRESSES

A Set up the scope:

1. Use: '-strobe bits 0-8' as a sync point for 16K, bits 0-8.
   '-strobe bits 9-17' as a sync point for 16K, bits 9-17.
   '-gate preamp A', K4J10 (SR071) as a sync point for 32K, bits 0-8.
   '-gate preamp B', K4J02 (SR071) as a sync point for 32K, bits 8-16.
2. Display 'strobe' on channel A, and note the position for reference.
3. Display the sense bits:

   Channel A probe to one sense line.
   Channel B probe to the other end of the sense line.
   Channel B inverted.
   Channels A and B added.
   Channels A and B at the same gain setting.
   Time Scale: 100 ns/cm

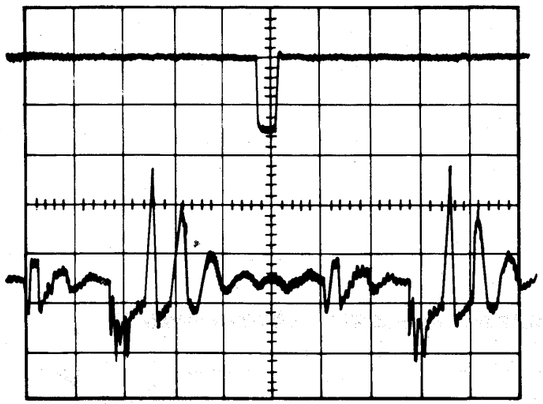
This gives a differential display on the scope.

Note: The sense bits are logically inverted on the interface between the CCU and the BSM. A logical '1' bit in the BSM becomes a logical '0' bit in the CCU (SR077).

The wave forms shown here are typical of a BSM, but they vary with each BSM. Be careful when interpreting the array sense bit wave forms. It may be difficult to distinguish between the actual signal and noise.

B Use either the storage scan procedure on page 1-140 or the procedure for storing a test pattern in storage on page 1-140.

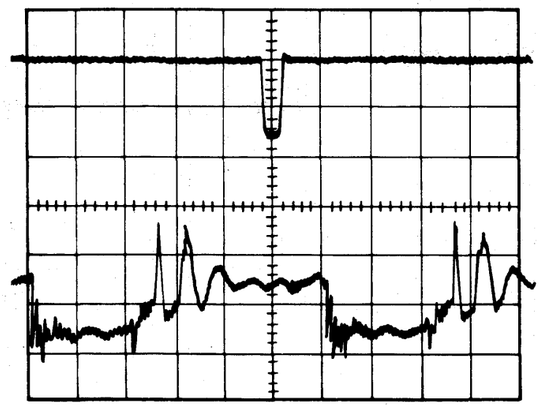
Data/Address switches set to 'FFFF'.



All Addresses
-Strobe Bits 0-8
5 V/cm
K4J12 (SR071) (32K)
J4B07 (SR071) (16K)

Array Sense Bit 0
1 V/cm
K4B02/K4D02 (SR071) (32K)
J4B02/J4D02 (SR071) (16K)

Data/Address switches set to '0000'.



All Addresses
-Strobe Bits 0-8
5 V/cm
K4J12 (SR071) (32K)
J4B07 (SR071) (16K)

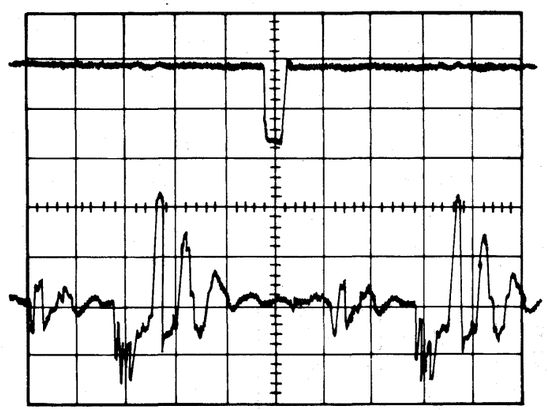
Array Sense Bit 0
1 V/cm
K4B02/K4D02 (SR071) (32K)
J4B02/J4D02 (SR071) (16K)

SENSE BIT SCOPING OF A SINGLE ADDRESS

Set up the scope as in "Sense Bit Scoping of All Addresses".

Use either the "Single Address Scan" on page 1-150 or the "Single Address Test Pattern Procedure" on page 1-150.

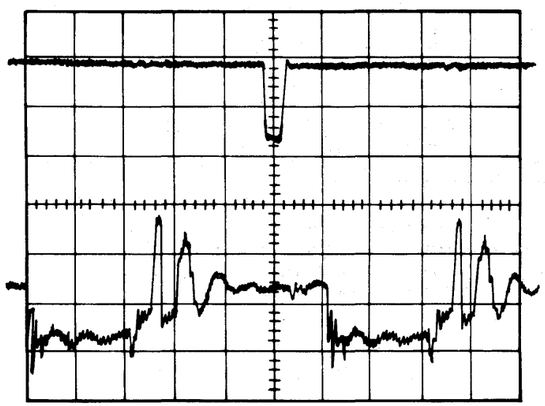
Data/Address switches set to 'FFFF'.



Single Address
-Strobe Bits 0-8
5 V/cm
K4J12 (SR071) (32K)
J4B07 (SR071) (16K)

Array Sense Bit 0
1 V/cm
K4B02/K4D02 (SR071) (32K)
J4B02/J4D02 (SR071) (16K)

Data/Address switches set to '0000'

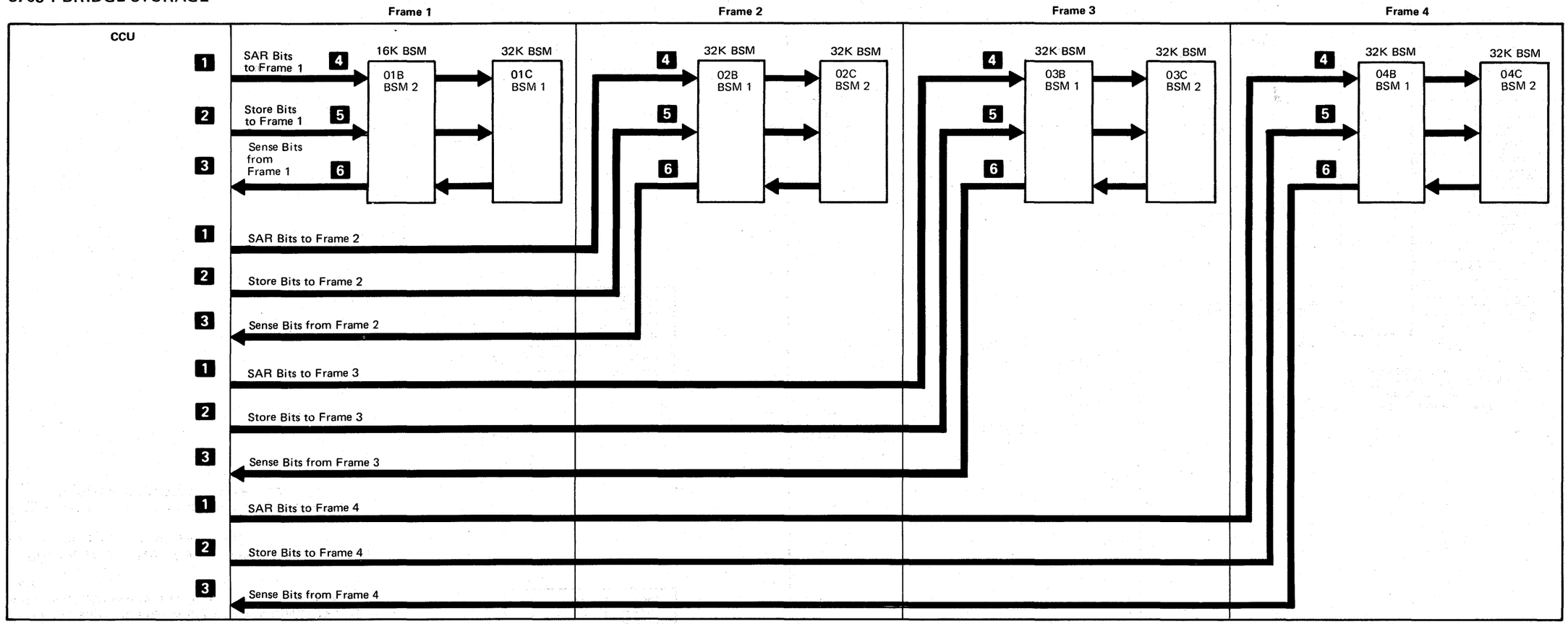


Single Address
-Strobe Bits 0-8
5 V/cm
K4J12 (SR071) (32K)
J4B07 (SR071) (16K)

Array Sense Bit 0
1 V/cm
K4B02/K4D02 (SR071) (32K)
J4B02/J4D02 (SR071) (16K)

STORAGE DATA TO CCU

3705-I BRIDGE STORAGE



Note: The 16K BSM is always the last logical BSM, but it is always in the first frame physically.

1

SAR Bits to Storage

CCU			
To Frame	Card Loc.	Card Type	ALD Page
1	B4C2	6797	AM001
2	B4C3	6797	AM101
3	B4C4	6797	AM201
4	B4C5	6797	AM301

2

Store Bits to Storage

CCU				
To Frame	Byte	Card Loc.	Card Type	ALD Page
1	0	B4B2	6799	AM002
1	1	B4A2	6799	AM002
2	0	B4B3	6799	AM102
2	1	B4A3	6799	AM102
3	0	B4B4	6799	AM202
3	1	B4A4	6799	AM202
4	0	B4B5	6799	AM302
4	1	B4A5	6799	AM302

3

Sense Bits from Storage

CCU				
To Frame	Byte	Card Loc.	Card Type	ALD Page
1	0	B4B2	6799	AM002
1	1	B4A2	6799	AM002
2	0	B4B3	6799	AM102
2	1	B4A3	6799	AM102
3	0	B4B4	6799	AM202
3	1	B4A4	6799	AM202
4	0	B4B5	6799	AM302
4	1	B4A5	6799	AM302

4

SAR Bits From CCU

First BSM in Each Frame		
Bits	Card Loc.	ALD Page
2-3	W1B1	WS001
4-7	W1C1	WS001
8	W1A1	WS001
9-11	W1B1	WS001
12-15	W1C1	WS001

5

Store Bits From CCU

First BSM in Each Frame		
Bits	Card Loc.	ALD Page
0	W1G1	WS001
1-3	W1F1	WS001
4-7	W1E1	WS001
8	W1D1	WS001
9	W1K1	WS001
10-13	W1J1	WS001
14-17	W1H1	WS001

6

Sense Bits to CCU

First BSM in Each Frame		
Bits	Card Loc.	ALD Page
0	W1G1	WS002
1-4	W1F1	WS002
5-7	W1E1	WS002
8	W1D1	WS002
9-10	W1K1	WS002
11-13	W1J1	WS002
14-17	W1H1	WS002

STO

STORAGE CONTROLS TO CCU

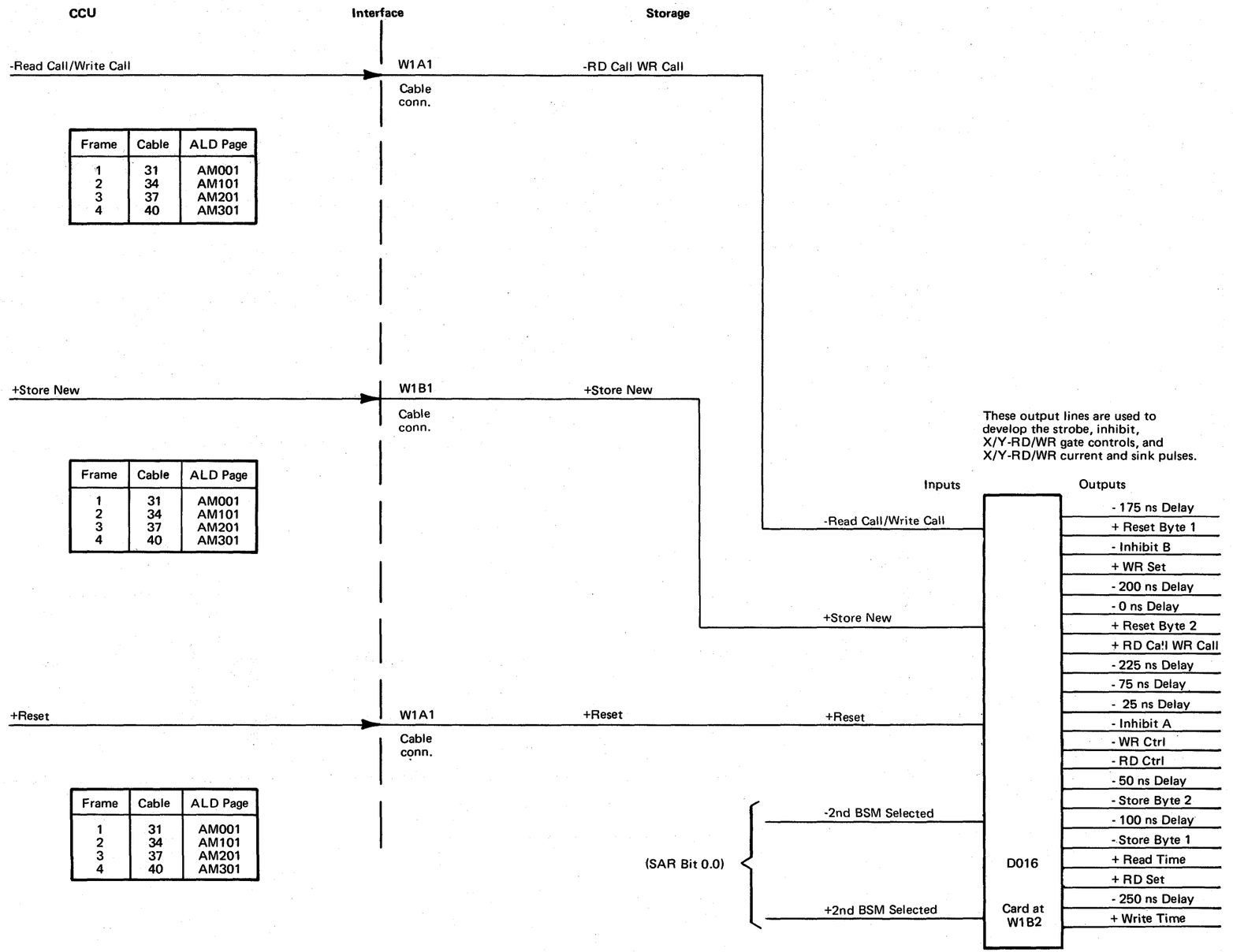
3705-I BRIDGE STORAGE

When the DIAGNOSTIC CONTROL switch is not in the CLOCK STEP position, 'read call' alternates with 'write call' every 600 ns. However, when the DIAGNOSTIC CONTROL switch is in the CLOCK STEP position, 'read call' and 'write call' alternate at a rate controlled by the operation of the START push button. 'Read call' starts the internal clock in the BSM. The BSM clock runs asynchronously through one read operation and stops. 'Write call' restarts the internal clock in the BSM, and the BSM clock runs asynchronously through one write operation and stops.

'Store new' resets the 'data' latches and puts the information on the 'store bit' lines into the 'data' latches. The data in the 'data' latches is written into storage during the write cycle.

'Reset' resets the 'data' latches and the latches controlling 'rd time', 'wr time', 'rd set', and 'wr set'.

Note: Bytes 1 and 2 in the storage correspond to bytes 0 and 1 in the remainder of the 3705.



STORAGE CYCLE TIMING

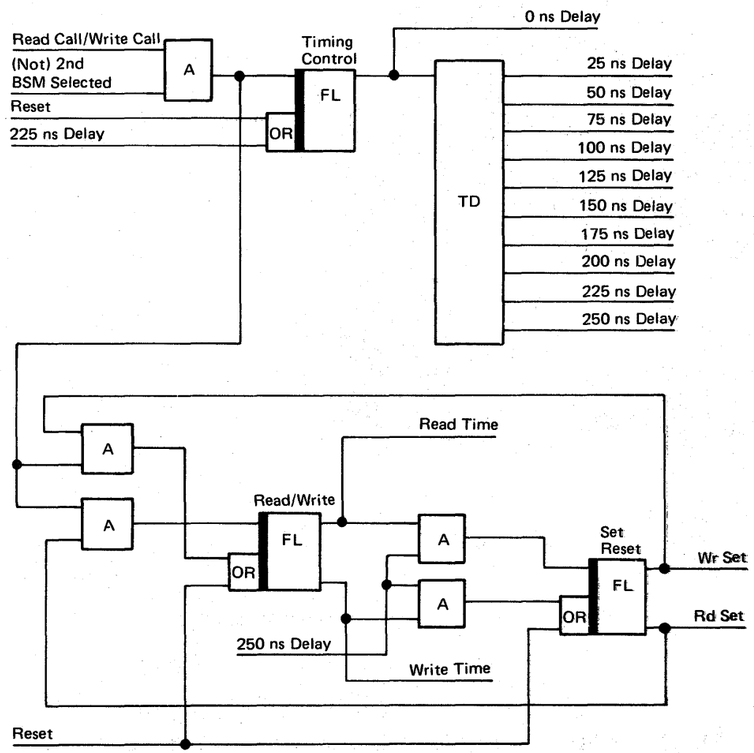
3705-I BRIDGE STORAGE

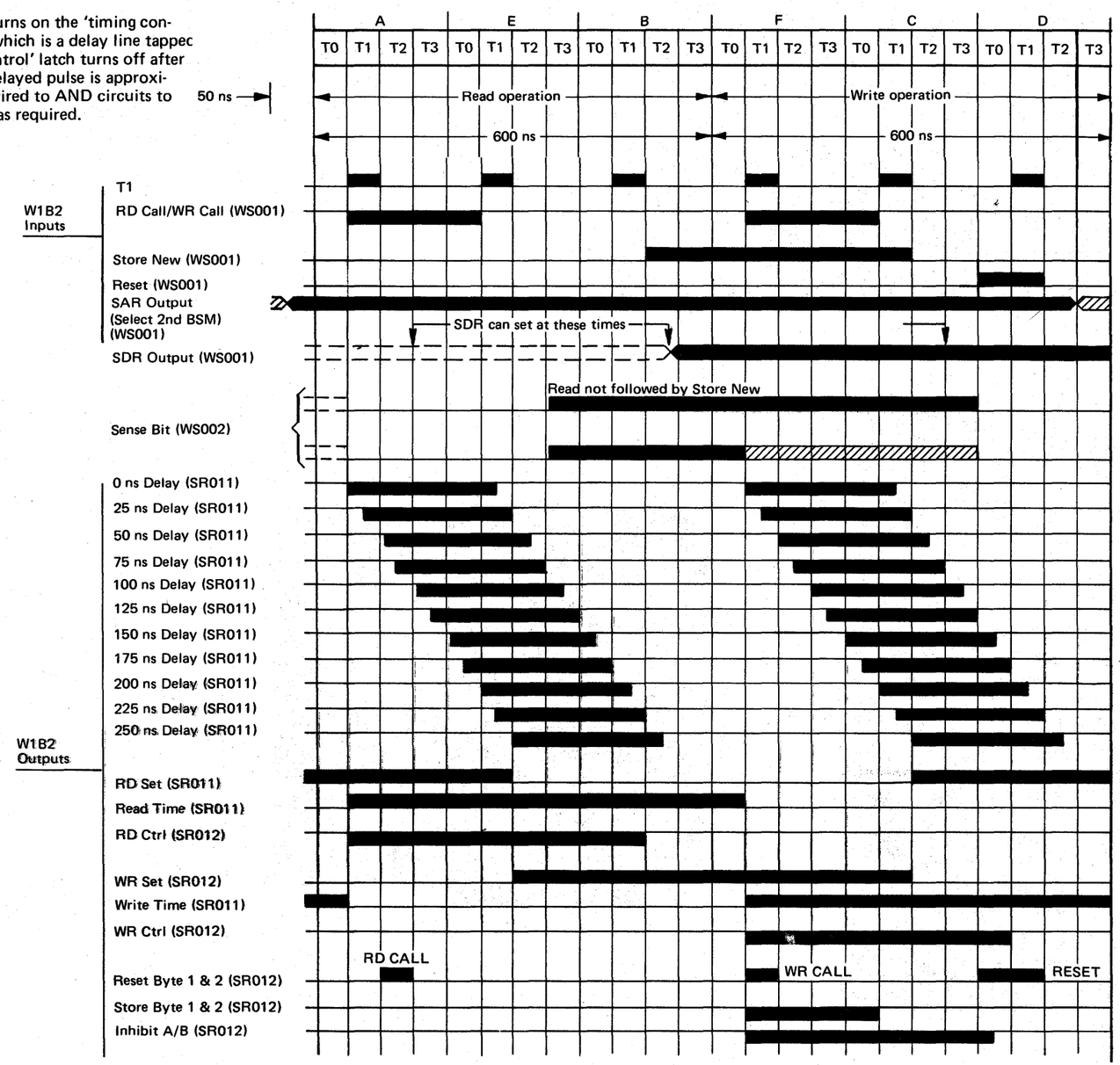
The BSM is an asynchronous unit; once started, it operates independently from the CCU. The CCU starts the storage cycle by issuing the 'read call/write call' signal. This turns on the 'timing control' latch and the 'read/write' latch. The 'read/write' latch on defines this cycle as a readout cycle. Late in the readout cycle, the 'set reset' latch is turned on, performing no function at this time but ensuring that the next 'read call/write call' will reset the 'read/write' latch. Therefore, the following cycle will be a write cycle. During the write cycle, the 'set reset' latch is turned off, forcing the next cycle to be a readout cycle.

The CCU allows 600 ns for each cycle (read or write) to be completed; it holds the storage address in SAR for both cycles.

STORAGE CLOCK

Each 'read call/write call' signal turns on the 'timing control' latch. This starts the clock, which is a delay line tappec at 25 ns intervals. The 'timing control' latch turns off after 225 ns, so the duration of each delayed pulse is approximately 225 ns. These pulses are wired to AND circuits to provide composite timing signals as required.

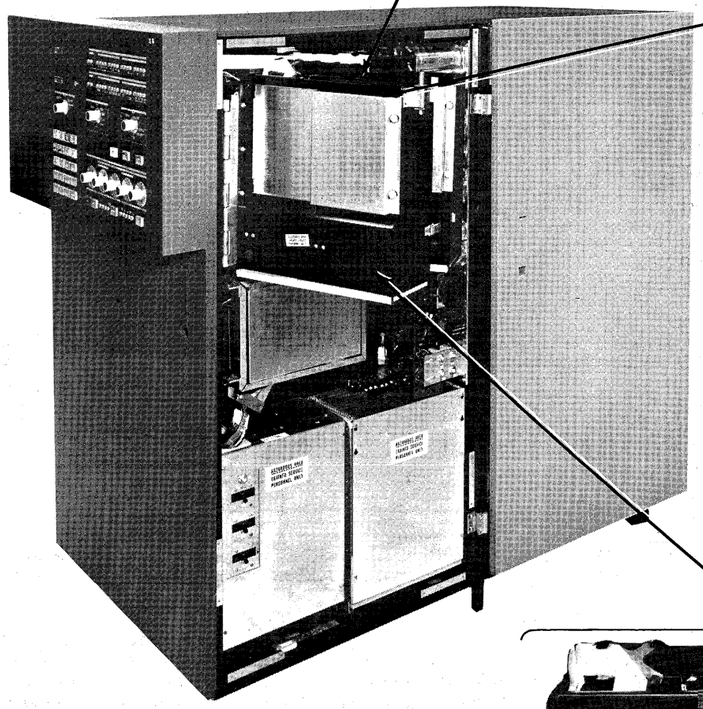


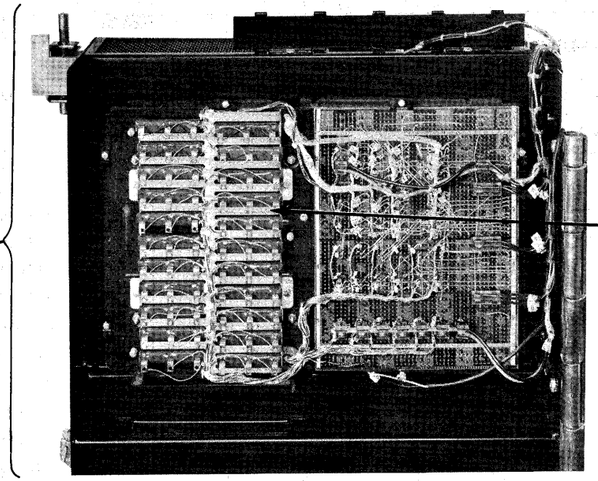


STORAGE PHYSICAL LOCATION

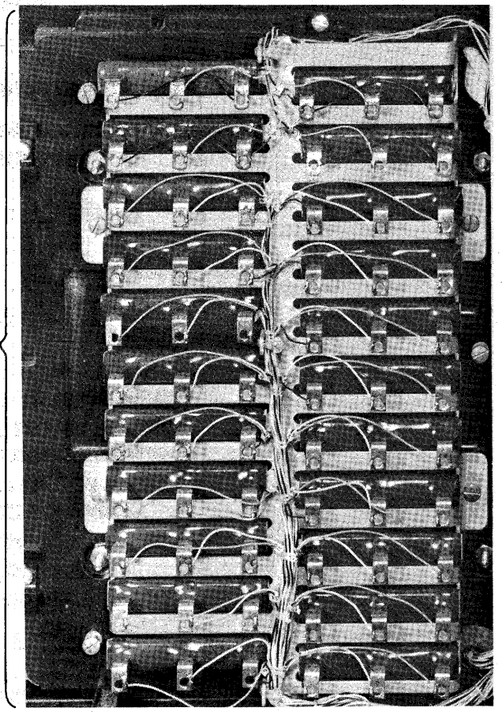
3705-I BRIDGE STORAGE

- 3705 storage is located on the B and C gates.
- The first BSM is located in the B gate of the module in which it is located.
- The B and C gates are referred to as the W1 gate in the storage ALDs.





Pin side of storage gate
B Gate

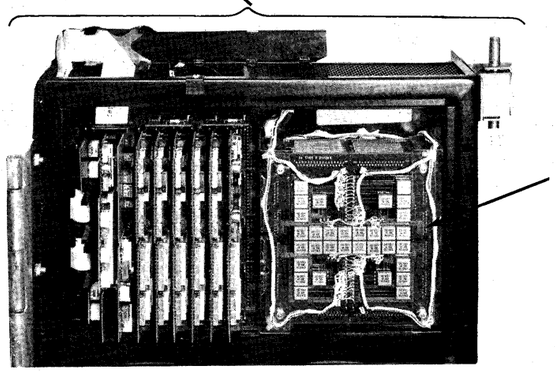


The XYZ Resistor Board covers the bottom diode board.
See SR214 for layout details of the bottom diode board.

Gate locations and storage addresses are related in the following chart.

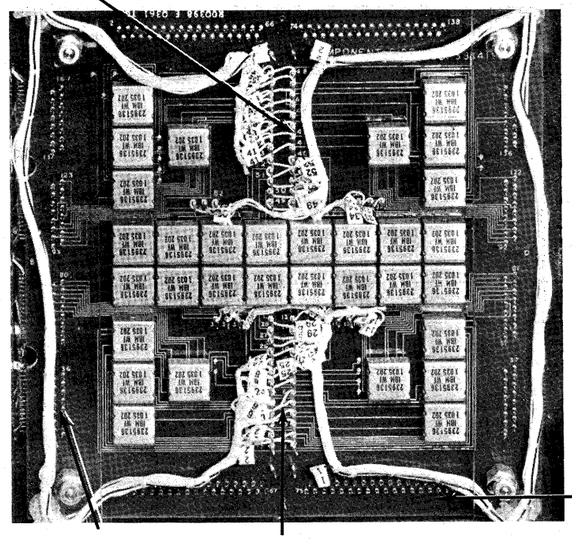
Gate	Address Found in Each Frame*			
	Frame 1	Frame 2	Frame 3	Frame 4
B	224-240K	32-64K	96-128K	160-192K
C	0-32K	64-96K	128-160K	192-224K

*Maximum configuration of the storage. In all configurations, the 16K BSM is the last logical BSM in the addressing scheme.



Card side of storage gate
B Gate

Top Diode Board Pins 33-64



Array Side B
Pins 6-167

Top Diode Board
Pins 1-32

SERVICE TECHNIQUES

3705-I BRIDGE STORAGE

BSM SERVICING

For reliable storage operation, the BSM diagnostics should run error-free with the -30 V XYZ drive voltage varied ±1.2 V from its optimum setting. (See "XYZ Drive Voltage Reoptimization" on page 7-160.) The standard CE pocket meter is sufficient for this purpose, since adjustments are relative to the optimum setting. If BSM operation is unreliable, both XYZ drive voltage reoptimization and strobe setting and -30 V reoptimization are required.

The decal on the XYZ current limiting resistor cover lists the proper -30 V and strobe settings for each BSM.

The 30 V power supply is a temperature tracking supply that adjusts by -75 mV for each degree farenheit that the temperature rises.

Card replacement, voltage and strobe adjustments, and repairs to visual shorts or opens are the only repairs that can be done by the CE. Array failures other than cabling defects, open diodes, and visual opens and shorts require BSM replacement.

FAULT LOCATION

The storage diagnostics should be run to establish a failing pattern, if it is not already evident from the reported problem. If the failure is in the first logical BSM, it may prevent loading and/or executing the storage diagnostics. Manually storing and displaying, or scanning storage may establish the failure pattern. The following procedure may also be used to check the first logical BSM.

- Set the MODE SELECT switch to INSTRUCTION STEP.
- Press the RESET then LOAD pushbuttons.
- Store the following program:

Address	*Data*	*Instruction*	
00000	3188	LR	1, 3
00002	1181	STH	1, 0 (1)
00004	9102	ARI	1 (1), 2
00006	21B8	CR	1, 2
00008	8802	BZL	X'0000C'
0000A	A80B	B	X'00002'
0000C	A102	SRI	1 (1), 2
0000E	1501	LH	5, 0 (1)
00010	15B0	CHR	5, 1
00012	8806	BZL	X'0001A'
00014	7114	OUT	1, X'71'
00016	7524	OUT	5, X'72'
00018	7004	OUT	0, X'70'
0001A	A102	SRI	1 (1), 2
0001C	13B8	CR	3, 1
0001E	8821	BZL	X'00000'
00020	A815	B	X'0000E'

- Check that memory where program is loaded is functioning correctly by displaying and checking program just loaded.
- Store X'00022' in register X'03'.
- Store X'04000' in register X'02' if this is a 16K machine. Store X'08000' otherwise.
- Store X'00000' in register X'00'.
- Set the MODE SELECT switch to PROCESS.
- Press the START pushbutton.
- The program loads each halfword with its address as data and checks that the proper value is stored. If an error occurs the program will hardstop.
- Set the DISPLAY/FUNCTION SELECT switch to a position other than STATUS or TAR and OP REGISTER.

  DISPLAY A = Address
  DISPLAY B = Data

- Pressing the START pushbutton causes the program to loop until the next failure.
- Continue until a failing pattern is established.

Most problems are associated with component failures and are in two categories:

1. Normal circuit failures such as card, loose connector, etc.

2. Array failures such as shorted lines, diodes, etc.

All BSM problems should be approached as if they are normal circuit failures. These failures can be broken into the following distinct patterns.

SINGLE BIT, MULTIPLE ADDRESS FAILURES

A sense/inhibit problem usually shows up as an extra or missing bit throughout an 8K block of storage. (Each sense/inhibit line passes through 8, 192 cores.) If the sense/inhibit card is not at fault, check the wiring to the inhibit current limiting resistor. (Refer to SR071-076 and to SR264 for locations.) See that -30V appears on pin 2 of the affected resistor. This failure could also be caused by a defective gate driver card. (See "Addressing" on page 7-010.)

A single bit failure in all addresses could be caused by the current source card, the control driver card, or a bad strobe driver card. Check also for a broken sense/inhibit wire between the array and the back panel pins on the sense amplifier. (See "Sense/Inhibit" on page 7-030.) A complete sense/inhibit winding resistance should measure approximately 14.0 ohms. An open or shorted sense/inhibit winding that is determined to be within the core plane requires a BSM replacement.

Multiple Bits, Multiple Address Failures

If this type of problem cannot be corrected by card swapping or replacement, an array failure probably exists. If the failure is related to an address pattern, it suggests an open X or Y drive line, a defective gate driver card, or a sense/inhibit card.

If the failure is related to a combination of more than one address pattern, it suggests a short between drive lines. Multiple bit failures in all addresses could be caused by the current source card, the control driver card, or a sense/inhibit card.

SHORTS BETWEEN DRIVE LINES

Shorts between drive lines usually show up as the dropping of one or more bits of two addresses. Analysis of the failing bits shows in almost all cases that they are adjacent in the array. This can be verified by a resistance check. When the two lines have been located, a resistance check should be made between the two lines, moving from one end of the array to the other. Because of the resistance of the windings, less resistance is seen as you get nearer the short.

In almost all cases, the short is caused by foreign material between the adjacent pins, or two pins are touching. A visual check with a strong light may show the shorted area. If foreign material is causing the short, it is possible that the material cannot be seen. The foreign material may be removed by passing a piece of paper between the pins at the area of the short.

DEFECTIVE CORES

A defective core position usually shows up as the dropping of a single bit in a single address. This type of problem can be caused by cracked, chipped, or broken cores losing their magnetic properties.

Vary the -30 V drive voltage and the strobe setting to see if the rate of failure changes. If the problem persists and you cannot obtain reliable operation, replace the BSM.

POOR SOLDER CONNECTIONS AND WELDS

This type of problem may be initially diagnosed as an open line due to a diode or an internal open within the array. However, before assuming that either of these are the cause, make a complete resistance check.

Open land patterns can be repaired by using number 30 wire to jumper the open.

Solder connections or welds can be resoldered satisfactorily.

BSM REPLACEMENT

When replacing a BSM, refer to reference page SR200 (32K) or SR229 (16K) for applicable jumpers.

Damage may result from improper jumpering.

CONTINUITY CHECK OF XY DRIVE LINES

3705-I BRIDGE STORAGE

The charts on ALD pages SR174 and SR184 (16K) (SR234 and SR244 for 32K) describe all X and Y drive lines and contain all the points (terminals) for performing a continuity check. An example of how to perform a continuity check for a 16K BSM follows. The same procedure is used for a 32K BSM.

Example: This example is for a failing X address of 000110. X-read current is shown from the left to the right through the array X-winding. X-write current is shown from right to left through the same array X-winding.

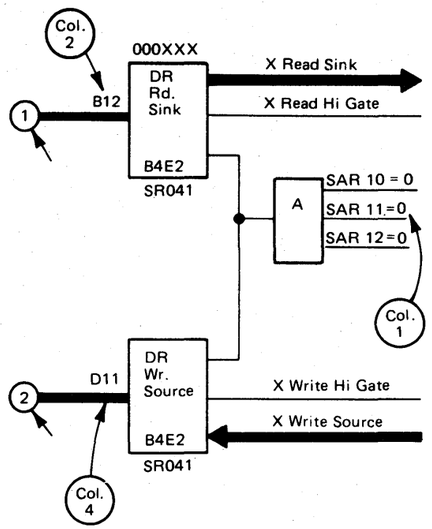
Note: This example uses conventional current flow theory, which is in the opposite direction from electron flow.

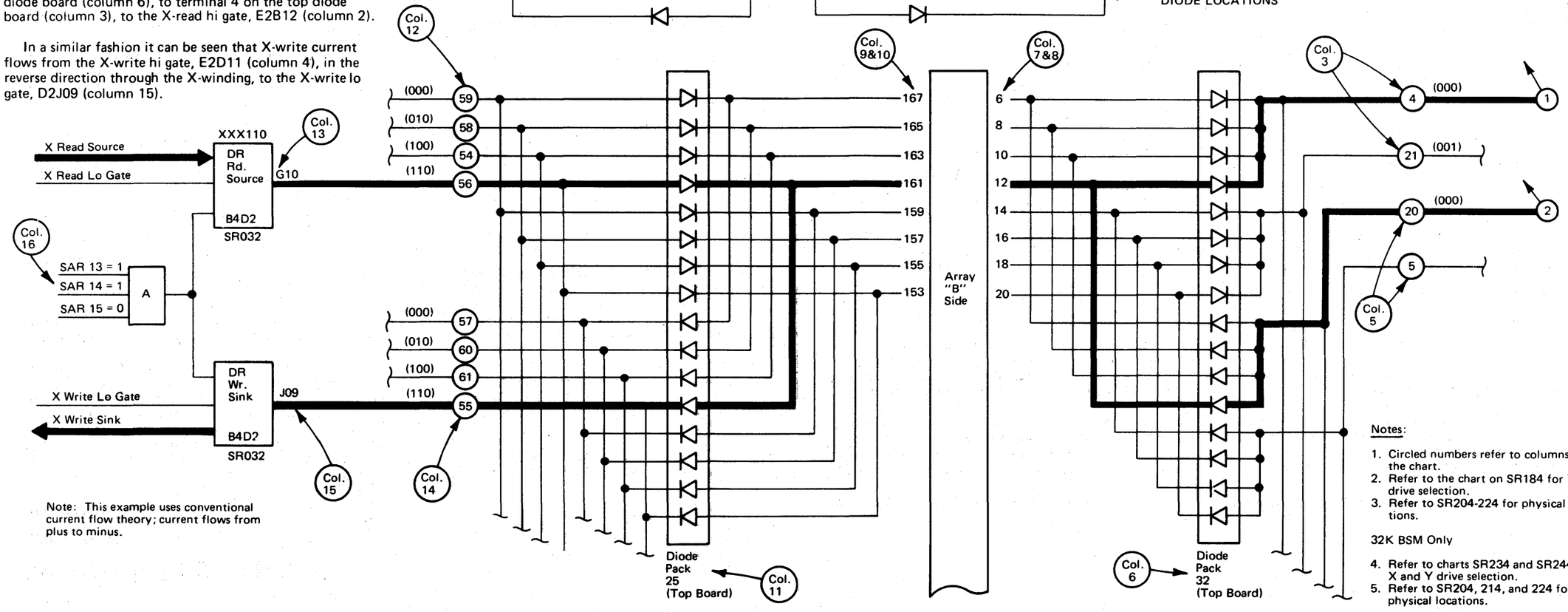
In this discussion column numbers refer to the chart on SR174.

Starting from the X-read lo gate, D2G10 (column 13), current flows to terminal 56 on the top diode board (column 11), to pin 161 on the top diode board (column 9), through the X-winding to pin 12 on the top diode board (column 7), through a diode in diode pack 32 on the top diode board (column 6), to terminal 4 on the top diode board (column 3), to the X-read hi gate, E2B12 (column 2).

In a similar fashion it can be seen that X-write current flows from the X-write hi gate, E2D11 (column 4), in the reverse direction through the X-winding, to the X-write lo gate, D2J09 (column 15).

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
HI ORDER								LOW ORDER							
HI ORDER ADDRESS	DRIVE LINE PINS				DIODE PACK HI ORDER TOP BOARD	CORE LINE GOING				DIODE PACK LOW ORDER TOP BOARD	DRIVE LINE PINS				LOW ORDER ADDRESS
	READ SINK		WRITE SOURCE			FROM		TO			READ SOURCE		WRITE SINK		
SAR BITS 10 11 12	LARGE BOARD	TOP DIODE BOARD	LARGE BOARD	TOP DIODE BOARD	PACK NO.	PIN NO.	ARRAY SIDE	PIN NO.	ARRAY SIDE	PACK NO.	TOP DIODE BOARD	LARGE BOARD	TOP DIODE BOARD	LARGE BOARD	SAR BITS 13 14 15
0 0 0	E2B12	4	E2D11	20	32	6	B	167	B	25	59	D2D11	57	D2B12	0 0 0
					8	7	D	166			45	D2B10	47	D2D09	0 0 1
					32	8	B	165		SR174	58	D2D04	60	D2B07	0 1 0
					8	9	D	164			44	D2B05	46	D2B04	0 1 1
					32	10	B	163		25	54	D2G04	61	D2G03	1 0 0
					8	11	D	162		1	42	D2G05	43	D2B12	1 0 1
0 0 0	E2B12	4	E2D11	20	32	12	B	161	B	25	56	D2G10	55	D2J09	1 1 0
					8	13	D	160	D	1	48	D2G12	41	D2J13	1 1 1
		5	32 8	14							59 45	D2D11 D2B10	57	D2B12	0 0 0 0 0 1





Note: This example uses conventional current flow theory; current flows from plus to minus.

Notes:

1. Circled numbers refer to columns on the chart.
2. Refer to the chart on SR184 for Y drive selection.
3. Refer to SR204-224 for physical locations.

32K BSM Only

4. Refer to charts SR234 and SR244 for X and Y drive selection.
5. Refer to SR204, 214, and 224 for physical locations.

LOCATING AN OPEN OR SHORTED DIODE

3705-I BRIDGE STORAGE

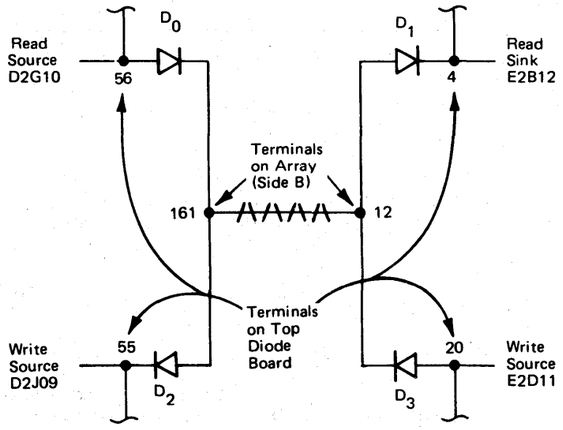
Because of the complex connection of the isolation diodes, many parallel paths exist and hinder a simple continuity check. A suggested method of locating a bad diode follows. This example is for the same failing X address (000110) as described in CONTINUITY CHECK on page 7-110.

1. Turn off the power.
2. Remove X gate cards W1D2 and W1E2 (W1D2, W1E2, and W1F2 for 32K).
3. Probe the points shown with an ohmmeter. Be careful to observe the polarity of the meter as indicated by the + or -. Expected meter readings are infinity (∞) or some resistance R (unpredictable because of meter and circuit variations). An infinite reading indicates an open diode. A zero reading indicates a shorted diode.

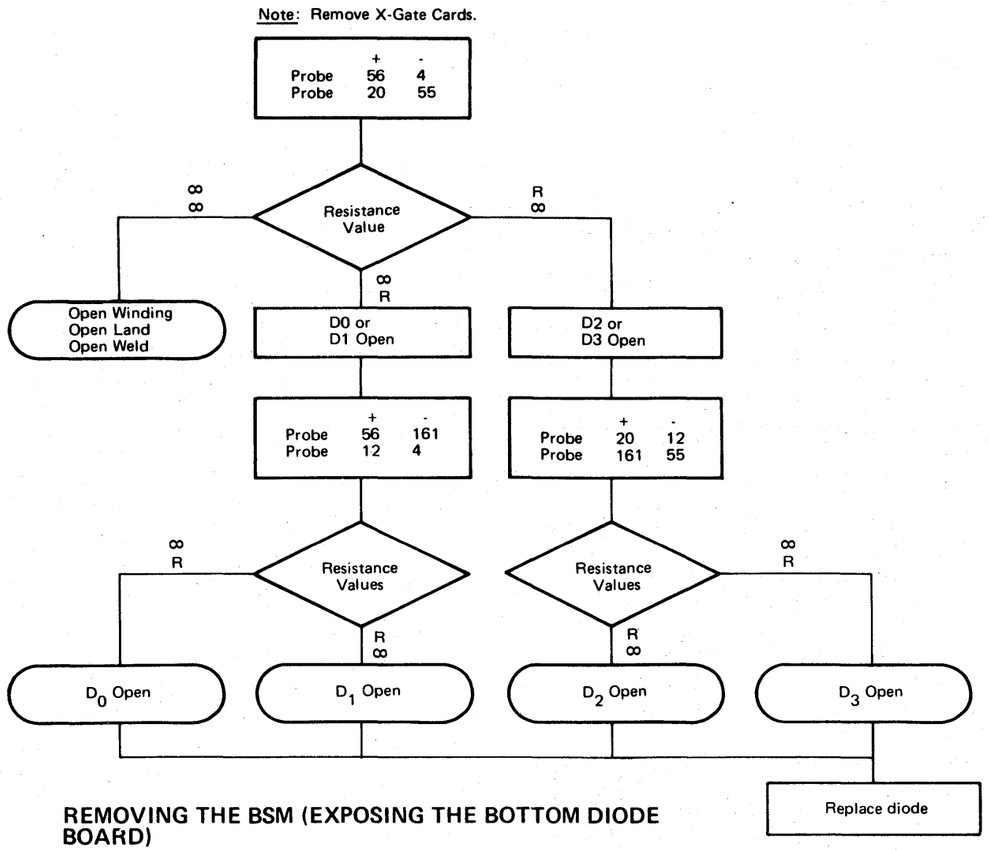
An open drive line may also be verified by scoping the source driver load resistor on the resistor panel. See 7-150 for the wave form of the Y-read current source with and without an open diode (see SR264). This method identifies an open array drive line if both Y-read and Y-write appear open. If either appears to be correct, an open diode is likely. A continuity check is required to determine which diode of the two in the line is open.

Once it has been determined that an open diode does exist, the charts on SR174 and SR184 (SR234 and SR244 for 32K) indicate the polarity of the diode to be replaced.

Probing points on the botton diode board requires removal of the BSM. See "Removing the BSM" on this page.



Note: Remove X-Gate Cards.



REMOVING THE BSM (EXPOSING THE BOTTOM DIODE BOARD)

If an open Y-line exists and the fault cannot be located on the top diode board, the BSM must be removed to expose the bottom diode board:

1. Disconnect all cables to the BSM.
2. Remove all the cards.
3. Remove the BSM and lay the unit with the card side down on a table.
4. Loosen the four nuts that hold the array on the board. The board is now connected by only the drive and sense/inhibit lines.
5. You can now expose the bottom diode board by the following method.

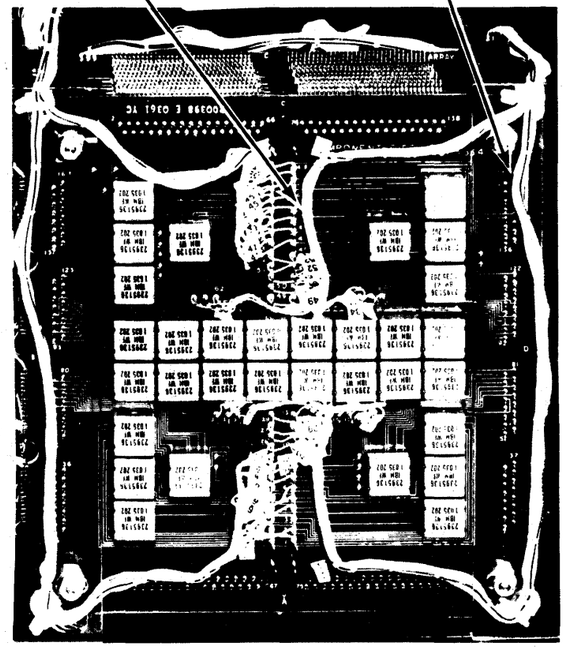
   Turn the unit over. Be careful to support the array since it is now connected only by wiring. Pull the array out vertically and turn it over so that it is laying top-side-down on the card socket. Reverse this procedure for installation.

REPLACING AN OPEN DIODE

An individual diode cannot be removed because it is a part of a module containing 16 diodes. Replacing an open diode requires soldering an individual GY diode (Part Number 2414891) over the open one. Use the following procedure.

Example: Replacing the read source diode for X address 000001.

1. Wrap one end of a yellow wire to the wrap pin on the diode board (column 3, 5, 12, or 14 on SR174 or SR184 for 16K, or SR234 or SR244 for 32K). Solder the other end of the wire to the proper end of the new diode.
2. Solder the other end of the diode to the proper terminal on the edge of the diode board (column 7 or 9 on SR174 or SR184 for 16K, or SR234 or SR244 for 32K).



Since the above procedure parallels the old diode, only open diodes can be replaced. A shorted diode requires BSM replacement.

INTERMITTENT OR RANDOM FAILURES

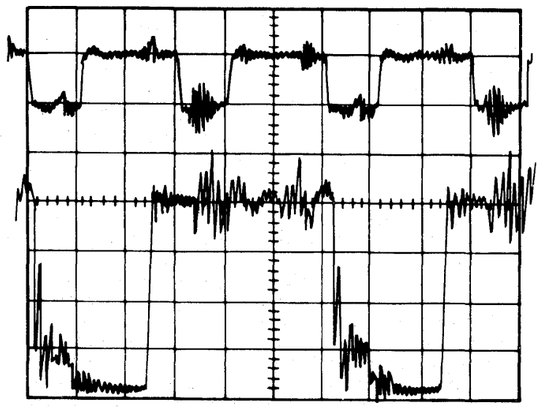
3705-I BRIDGE STORAGE

If a pattern cannot be determined and failures are of a random nature, the following areas should be checked for possible causes of the trouble.

A Use the oscilloscope to perform steps 1, 2, 3, and 4

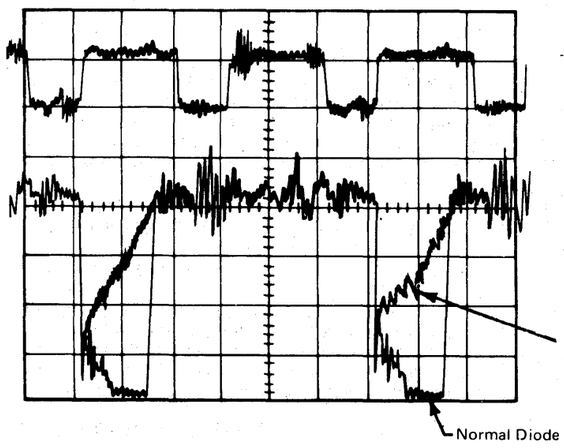
1 Probe the XY drive voltage pulses on the XY read and write current limiting resistors, and compare them with the following pictures.

Sync: -Read Call/Write Call
200 ns/cm
10X Probe



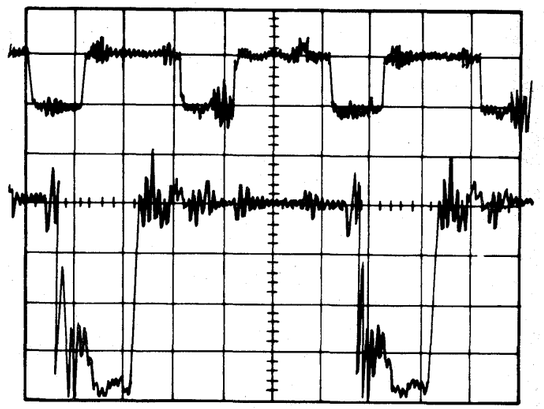
-Read Call/Write Call
1 V/cm
B2B07 (SR011) (32K)
B3B07 (SR011) (16K)

X Read Current Source Resistor
5 V/cm
Pin 2 (SR264)



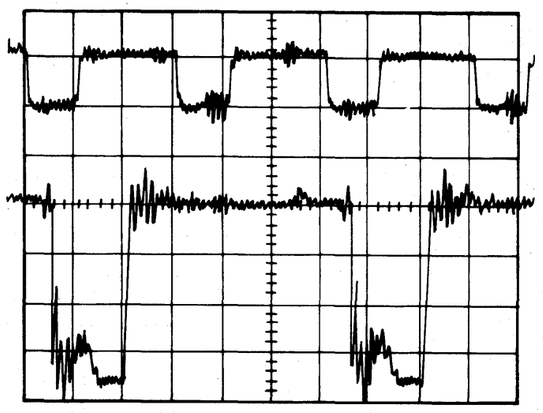
-Read Call/Write Call (Sync)
1 V/cm
B2B07 (SR011) (32K)
B3B07 (SR011) (16K)

Y Read current Source Resistor
5 V/cm
Pin 2 (SR264)



+Read Time
1 V/cm
K2J13 (SR022) (32K)
J2J13 (SR022) (16K)

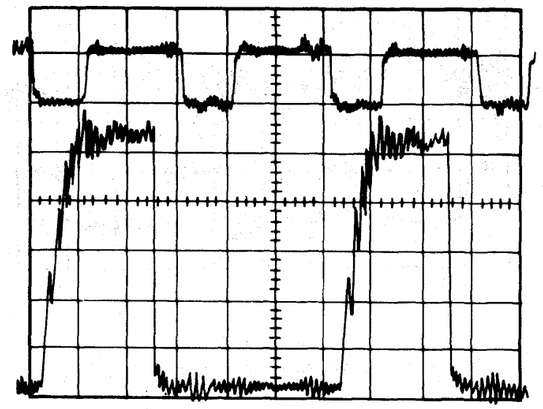
X Write Current Source Resistor
5 V/cm
Pin 2 (SR264)



+Write Time
1 V/cm
K2B03 (SR022) (32K)
J2B03 (SR022) (16K)

Y Write Current Source Resistor
5 V/cm
Pin 2 (SR264)

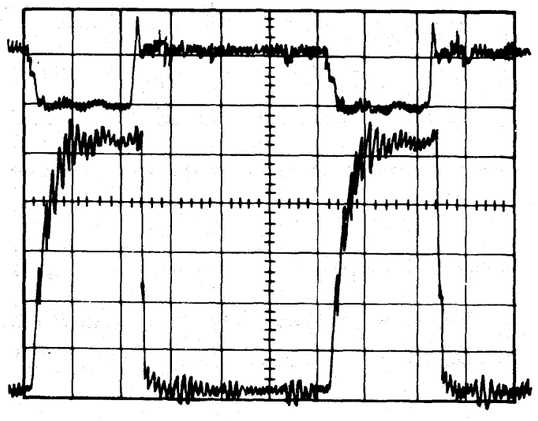
2 Probe the Z drive voltage pulses on the Z (inhibit) current limiting resistors, and compare them with the following pictures.



-Read Call/Write Call (Sync)
1 V/cm
B2B07 (SR011) (32K)
B3B07 (SR011) (16K)

Z load Bit 0 Resistor
5 V/cm
Pin 1 or 3 (SR264)

200 ns/cm
10X probe



32K
-Inhibit A bits 0-5
200 mv/cm
K4J04 (SR071)

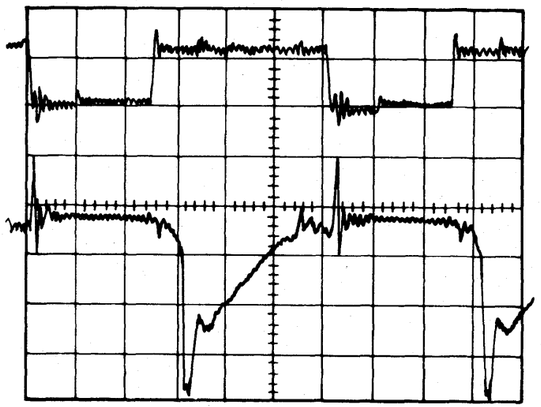
16K
-Inhibit Byte 1
J4J04

Z Load Bit 0 Resistor
5 V/cm
Pin 1 or 3 (SR264)

Note: No pulse will be observed on resistor pin 2 since it is the -30 V power supply connection. The XYZ drive voltage supply is a temperature tracking supply so the magnitude of the pulses may vary slightly if the XYZ drive voltage is not at -30 volts.

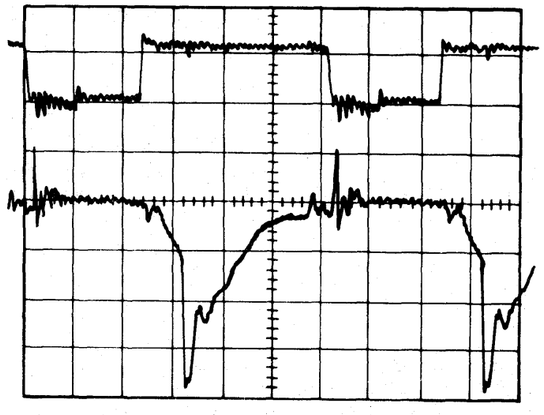
3 Probe the control driver, and compare the scope with the following pictures.

Sync (-Read Call/Write Call)
200 ns/cm
10X Probe



-Read Control
1 V/cm
C2B03 (SR021) (32K)
B2B03 (SR021) (16K)

X Rd Lo Gate Control
5 V/cm
C2D10 (SR021) (32K)
B2D10 (SR021) (16K)



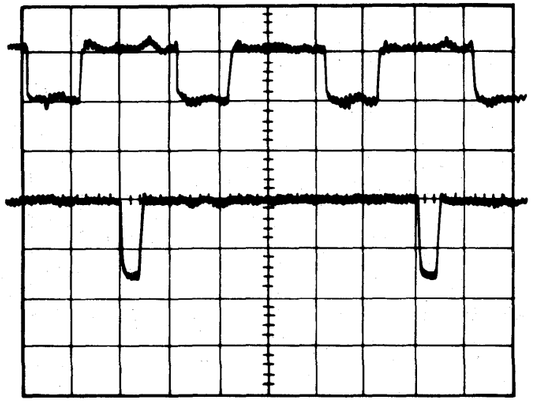
-Write Control
1 V/cm
C2B04 (SR021) (32K)
B2B04 (SR021) (16K)

X Wr Lo Gate Control
5 V/cm
C2D06 (SR021) (32K)
B2D06 (SR021) (16K)

STO

4 Probe the strobe driver, and compare the scope with the following picture.

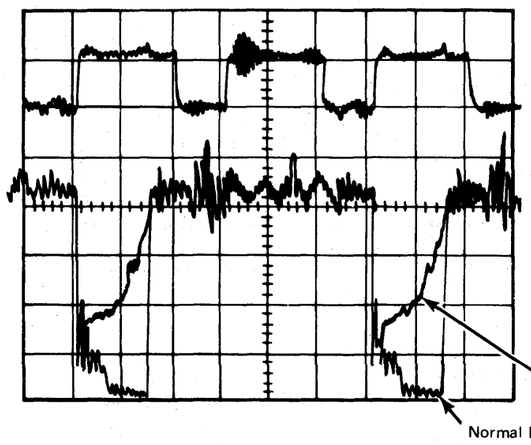
Sync (-Read Call/Write Call)
200 ns/cm
10X probe



-Read Call/Write Call
1 V/cm
B2B07 (SR011) (32K)
B3B07 (SR011) (16K)

-Strobe Bits 0-8/9-17
5 V/cm
C3D10/C3B04 (SR021) (32K)
B5D10/B5B04 (SR021) (16K)

See "Sense/Inhibit-Scoping Procedures' for instructions on cycling a single address.



-Read Call/Write Call
1 V/cm
B2B07 (SR011) (32K)
B3B07 (SR011) (16K)

Y Read Current Source Resistor
5 V/cm
Pin 2 (SR264)

Open Line or Open Diode

Normal Diode

B Check for improper setting of the -30 V, +6 V, -4 V, -14 V, and +3 V supply voltages. Use a Weston* 901 or equivalent meter to adjust these voltages. The +3 V supply should be adjusted with reference to the +6 V supply. Refer to the "Power Supply Adjustments and Checks" section.

C Check for loose voltage connectors to the large board. See SR264 for the connections.

D Check for unplugged back panel resistor assemblies. See SR264 for these connections.

* Trademark of Weston, Inc.

ADJUSTMENTS

3705-I BRIDGE STORAGE

XYZ DRIVE VOLTAGE REOPTIMIZATION

NOTE: If two BSMs are in the same frame, treat them as one BSM for voltage reoptimization. Voltage points for storage are shown on ALD page SR101.

Drive voltage marginal limits are normally reverified whenever replacing S/Z, timing, driver source, or strobe driver cards.

To reoptimize the drive voltage:

1. Loop the storage diagnostics. (Use Worse Case-Schmoo Test Routine number 09.)
2. Determine the upper drive voltage limit. Slowly decrease (approach zero) the drive voltage until an error occurs. (Measure the voltage at power control board 0XD-AIC6-E04, common 0XD-AIB6-E02. See page D-230. Adjust the drive voltage with the potentiometer on the card in position S5 of the power control board.) Record the last operating voltage as the upper limit.
3. Determine the lower drive voltage limit. Slowly increase (negative from -30 V) the drive voltage until an error occurs. Do not exceed -35 volts as the lower limit.

NOTE: The BSM should run error free for a minimum of of 30 seconds at the last operating point.

4. The optimum drive voltage is the average of the upper and lower drive voltage limits.
5. If the difference between the upper and the lower limits is less than 2.4 volts, strobe reoptimization may be necessary.

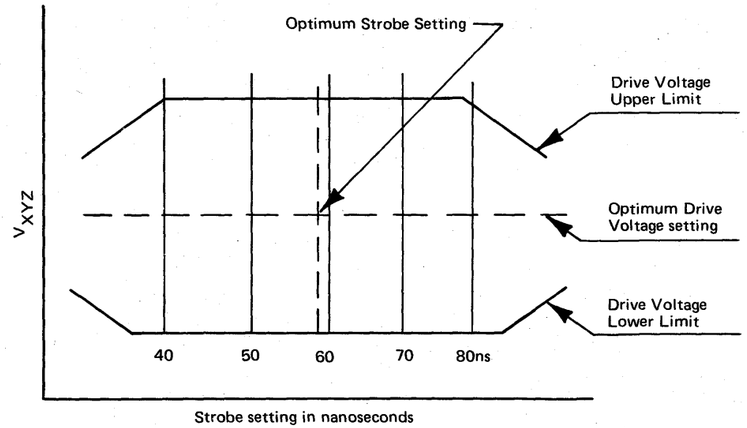
NOTE: To minimize the drive voltage power supply tracking error, reoptimize the drive voltage at a BSM ambient temperature of 68° to 86° F. It is permissible to optimize outside this temperature if necessary, but the drive voltage should be checked as soon as possible within the prescribed range.

Measure the temperature at the base of the array using a thermometer, part number 5392366, or equivalent.

STROBE SETTING REOPTIMIZATION

To reoptimize the strobe setting:

1. Loop storage diagnostics.
2. Determine and plot the upper and lower drive voltage limits for a range of strobe settings. The strobe should be set in 10 ns increments for this optimization process. Determine these limits as explained in the *XYX Drive Voltage Reoptimization* paragraphs. Make the strobe adjustments on the strobe driver card at C3 (B5 for 16K), using ALD page SR254 as a guide. A decal is provided on the XYZ current limiting resistor cover to indicate the initial setting that should be used as a reference.



3. Plot the limits recorded on the vertical axis and the strobe delay tap setting on the horizontal axis. The selected strobe setting should maximize the difference between the upper and lower drive voltage limits while centering the strobe between the earliest and latest acceptable settings.
4. The optimum drive voltage setting is the average of the upper and lower drive voltage limits at the selected strobe settings.
5. If the differences between the upper and lower voltage limits is less than 2.4 volts, a fault probably exists and must be corrected before further reoptimization is attempted.

POWER SUPPLY CHECKS AND ADJUSTMENTS

The 3705 supplies -30 V, +6 V, and -4 V to the BSM. A BSM internal +3 V and voltage sense -14 V is generated from the -6 V and -30 V respectively. The -30 V is a temperature-compensated drive voltage. (See the temperature graph on page D-230.)

In the power sequence, the -30 V is the last up and the first down.

Measure all voltages with a Weston* 901 meter or equivalent, with the temperature between 68° and 86° F.

Verify that the +6 V and -4 V are present at the power control board (0XD-AIB6-A04 for +6 V, 0XD-AIB6-E04 for -4 V, and 0XD-AIB6-E02 for common). The +3 V may be adjusted by means of a potentiometer on the upper-half of card A4 (32K) or C4 (16K).

NOTE: The +3 V is set by referencing it to the +6 V instead of ground. This results in the meter reading of -3 V.

Measure the -14 V, +0.05 V, on A4J11 (32K) or C4J11 (16K) referenced to ground. The voltage can be adjusted with a potentiometer on the lower half of the card at A4 (32K) or C4 (16K). (See ALD page SR101 for voltage measurements.)

* Trademark of Weston, Inc.

FET STORAGE MAINTENANCE PHILOSOPHY AND PHYSICAL LOCATIONS

FET STORAGE MAINTENANCE PHILOSOPHY

FET Storage Array Cards

FET storage has single-bit error correction. Therefore, FET array cards with single-bit errors are not replaced. When two errors occur at any address, a double-bit error is detected. A double-bit error can be caused by one error on each card of a card pair or by a double-bit error on one card of a card pair. The worst card should be replaced (the card with the double-bit error or the card with the most single-bit errors). See *IBM Maintenance Diagnostic Program IBM 3705 Communications Controller Internal Functional Test Symptom Indexes, D99-3705E.*

FET Storage Support Cards

When a failure occurs on one of the storage support cards, the diagnostic indicators can be used to aid in isolating the failure. Failures that cause a loss of timing signals (such as chip select timing or write pulses) may be isolated by card substitution or by the use of an oscilloscope.

Intermittent Problems

Intermittent failure of FET storage array cards should be a rare occurrance. If the IFTs do not indicate a storage problem but other indications (such as a machine check auto-IPL or hard-stop with SDR or Op Reg CC checks) point to an intermittent array problem, the following procedure should be used.

1. Determine the failing address using the maintenance procedure on Page 7-260. If this procedure does not point to the failing address, use the procedure on Page 7-290.
2. Replace the pair of array cards at the suspected address, or if feasible, try replacing one of the array cards at a time.

Intermittent problems are more likely to be caused by failures in the MST support logic.

FET STORAGE PHYSICAL LOCATIONS

The 3705-II contains FET storage while the 3705-I contains one or more bridge storage modules (core). The 3705-II comes in Models E, F, G, H. J. K, and L. The Model E has one frame, Models F and J have two frames, Models G and K have three frames, while the Models H and L have four frames. In the base frame, storage size increases in increments of 32K bytes (maximum of 256K bytes). In the first expansion frame, storage increases in increments of 64K bytes (maximum of 512K bytes).

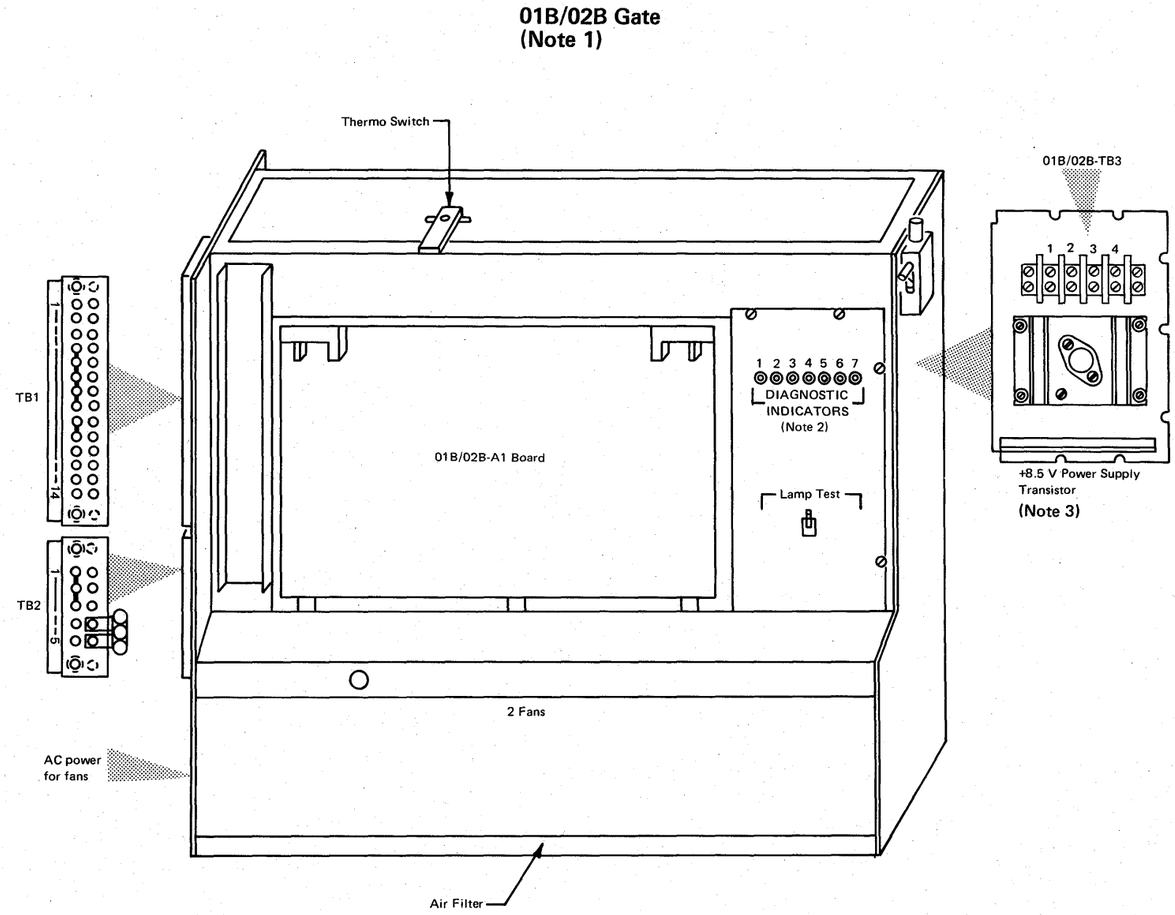
The chart below shows model and submodel designations with equivalent storage sizes.

Base Frame	First Expansion Frame	Second Expansion Frame	Third Expansion Frame	
Models	Models	Models	Models	Storage Size
E1	F1	G1	H1	32K
E2	F2	G2	H2	64K
E3	F3	G3	H3	96K
E4	F4	G4	H4	128K
E5	F5	G5	H5	160K
E6	F6	G6	H6	192K
E7	F7	G7	H7	224K
E8	F8	G8	H8	256K
–	J1	K1	L1	320K
–	J2	K2	L2	384K
–	J3	K3	L3	448K
–	J4	K4	L4	512K

All 3705-II Model E-H FET storage is located in the basic frame in gate 01B. None is located in the expansion frames. In 3705-II Models J-L, FET storage is located in both the base frame (gate 01B) and the first expansion frame (gate 02B). The FET storage cycle time is one microsecond for Models E-H and 900 nanoseconds for Models J-L. A read operation is performed every "A" cycle—even when in a stopped condition. Write operations are performed only when the CCU requires a store operation. The storage controls include automatic single-bit error correction and double-bit error detection. When a double-bit error is detected, the uncorrected bits are sent to the CCU and the parity bits for both bytes are inverted to force parity errors in the CCU. Data bits are not altered when a double-bit error is detected.

The IFTs are the primary means of servicing FET storage. A diagnostic indicator panel is located on the FET storage gate to assist you in isolating troubles when the IFTs cannot be loaded, or the trouble cannot be found using the IFTs.

The FET storage requires two special voltages: +3.4 V and +8.5 V. The transistor for the +8.5 V series regulator on a 3705-II with more than three cards in the OXD power control gate is located on the 01B gate mounted behind the diagnostic indicator panel. The +8.5 V is derived from the +12 V SCR supply (see D-330). The +3.4 V supply is located on gate 01H. The 3.4 V and 8.5 V power supplies on a 3705-II with only two or three cards in the OXD gate are located on the 01H gate (see D-500).



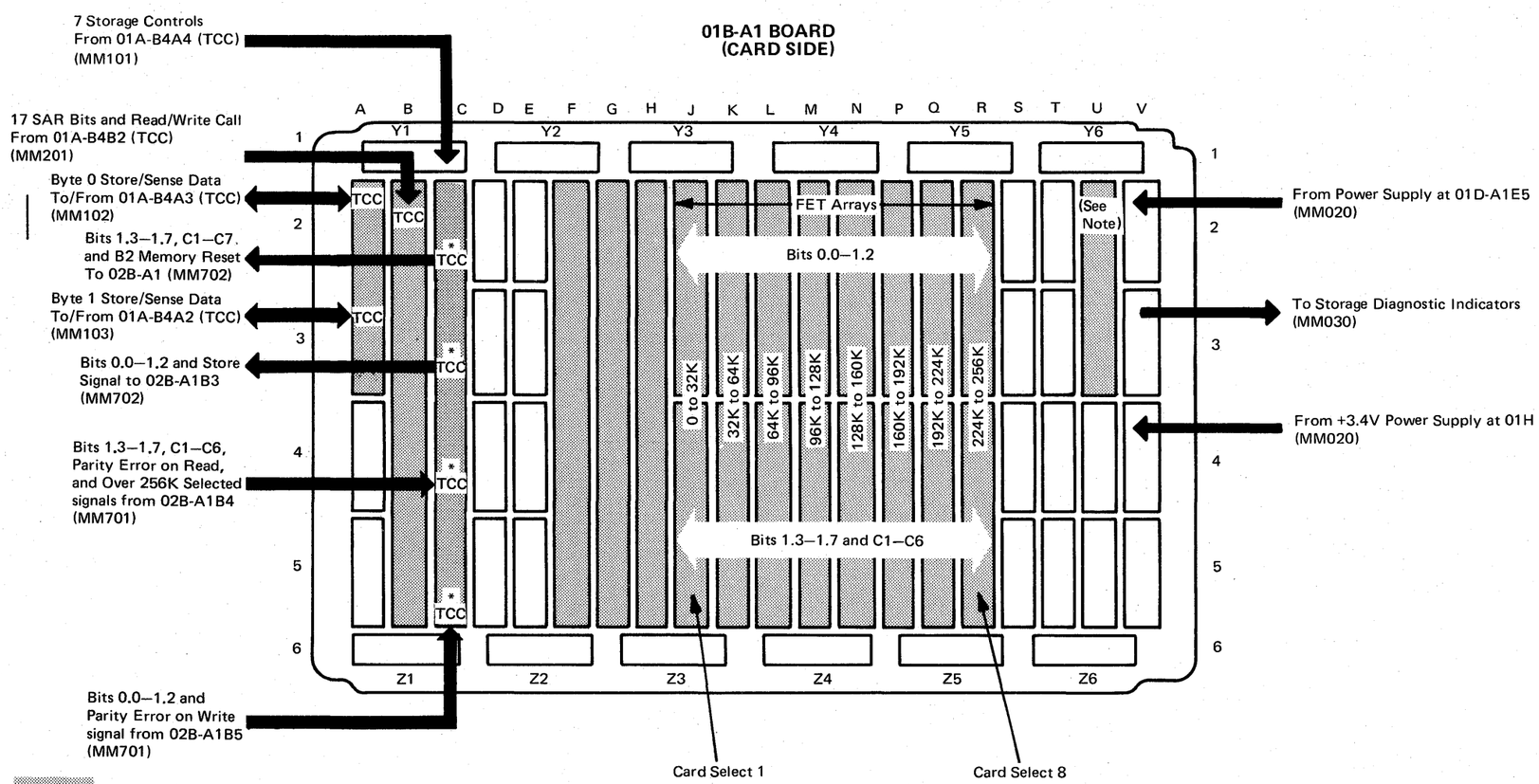
Notes:
1. The 02B gate is installed only when storage size exceeds 256K bytes.
2. The diagnostic indicators are present on the 01B gate only. The indicators can be used for storage sizes up to and including 512K bytes.
3. The illustrations shown do not apply to a 3705-II with only two or three cards in the OXD power control gate. Refer to D-500.

FET STORAGE BOARD LAYOUT (01B-A1)

(If over 256K, Models J-L only, see page 7-211 for 02B-A1 board layout.)

Card Location	ALD Page	Function
01B-A1A2	MM104	Store bit terminators (receivers)
	MM105	Sense bit drivers
	MM106	Detect sense bits parity error before CCU drivers output—LED 7
	MM107	Detect store bits parity error after CCU receivers—LED 1
01B-A1B2	MM201	SAR bit terminators
	MM202	Card select gate latch
	MM203	Card select decoding
	MM204	Write, gate CSX, and gate CSY
	MM206	Power SAR bit lines
01B-A1C2 (Installed for Models J-L only > 256K)	MM703	Redrive bits to over 256K byte mem
	MM704	Receive bits from over 256K byte mem
	MM705	Receive bits from under 256K byte mem
	MM706	Parity check on data sent to over 256K byte mem (LED 2)
	MM707	Parity check on data received from over 256K byte mem (LED 5)
01B-A1F2	MM301	Data from storage terminators
	MM302	Data registers for data bits and error corrections bits
	MM305	Detect (by bit) errors in data read from array
	MM306	Error correction for single-bit error
	MM307	Multiple-bit error detection
	MM308	Generate check bits from store data
	MM309	Generate sense bits 0.0 and 1.P
	MM310	Block error correction on multiple errors and force parity error
01B-A1G2	MM401	Generate read gate, store pulse, gate diag reg
	MM402	Diagnostic register
	MM404	Diagnostic indicator latches
	MM405	Diagnostic indicator LED drivers
	MM406	Store data storage drivers
	MM407	Store data parity checker
01B-A1H2	MM501	Data from storage isolation
	MM508	Parity check storage exit—LED 5 Parity error on read under 256K
	MM509	Check bit storage drivers
01B-A1J2	MM601	Select card 1—(0-32K) FET array (bits 0.0—1.2)
01B-A1J4	MM601	Select card 1—(0-32K) FET array (bits 1.3—1.7 and C1—C6)
01B-A1K2	MM602	Select card 2—(32K-64K) FET array (bits 0.0—1.2)
01B-A1K4	MM602	Select card 2—(32K-64K) FET array (bits 1.3—1.7 and C1—C6)
01B-A1L2	MM603	Select card 3—(64K-96K) FET array (bits 0.0—1.2)
01B-A1L4	MM603	Select card 3—(64K-96K) FET array (bits 1.3—1.7 and C1—C6)

Note: Card A1U2 is not present on a 3705-II with only two or three cards in the OXD power control gate.



*Cards in column C are present only if storage size is greater than 256K.

Card Location	ALD Page	Function
01B-A1M2	MM604	Select card 4—(96K-128K) FET array (bits 0.0—1.2)
01B-A1M4	MM604	Select card 4—(96K-128K) FET array (bits 1.3—1.7 and C1—C6)
01B-A1N2	MM605	Select card 5—(128K-160K) FET array (bits 0.0—1.2)
01B-A1N4	MM605	Select card 5—(128K-160K) FET array (bits 1.3—1.7 and C1—C6)

Card Location	ALD Page	Function
01B-A1P2	MM606	Select card 6—(160K-192K) FET array (bits 0.0—1.2)
01B-A1P4	MM606	Select card 6—(160K-192K) FET array (bits 1.3—1.7 and C1-C6)
01B-A1Q2	MM607	Select card 7—(192K-224K) FET array (bits 0.0—1.2)
01B-A1Q4	MM607	Select card 7—(192K-224K) FET array (bits 1.3—1.7 and C1—C6)

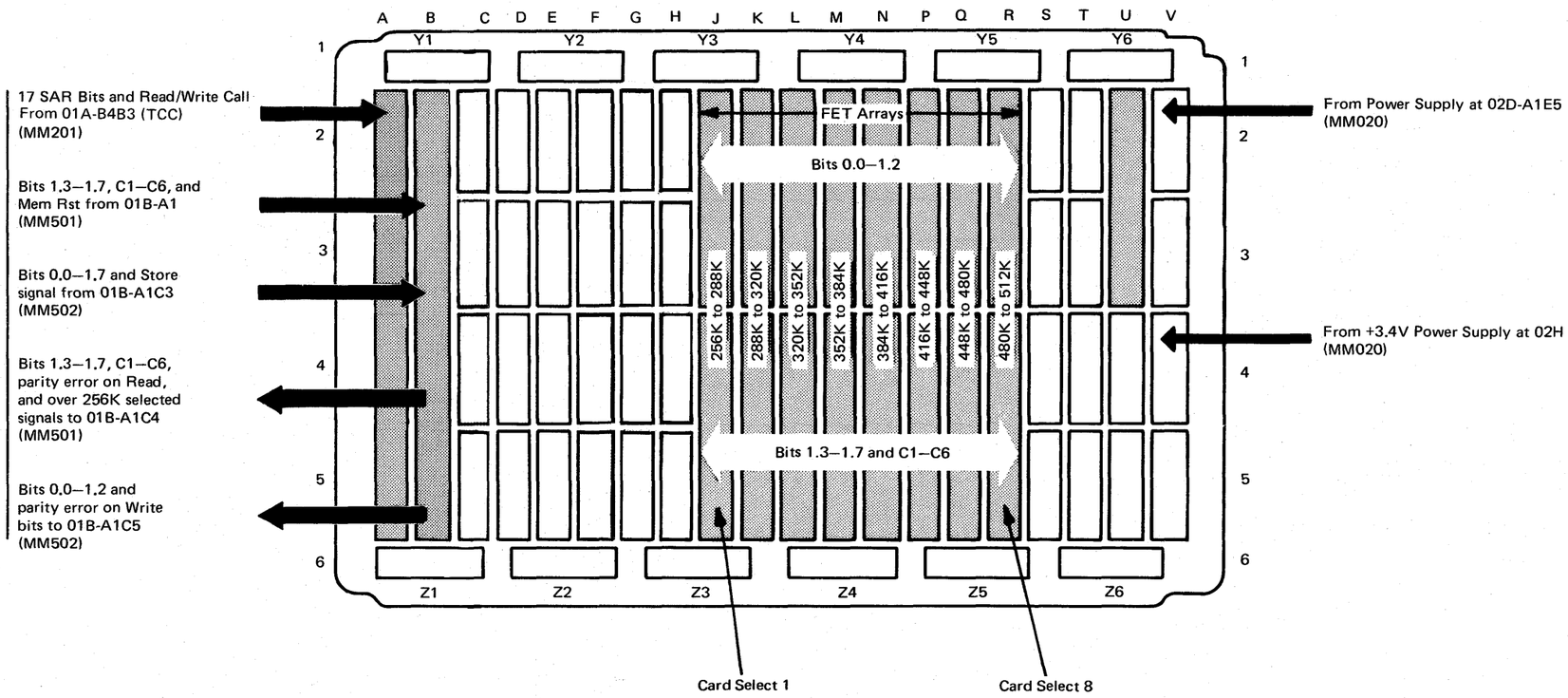
Card Location	ALD Page	Function
01B-A1R2	MM608	Select card 8—(224K-256K) FET array (bits 0.0—1.2)
01B-A1R4	MM608	Select card 8—(224K-256K) FET array (bits 1.3—1.7 and C1—C6)
01B-A1U2 (See Note)		Power supply sense and sequence

FET STORAGE BOARD LAYOUT – 02B-A1

(Installed only for 3705s with over 256K bytes of storage.)

Card Location	ALD Page	Function
02B-A1A2	MM201	SAR bit terminators
	MM202	Card select gate latch
	MM203	Card select decoding
	MM204	Write, Gate CSX, and Gate CSY
	MM206	Power SAT bit lines
02B-A1B2	MM503	Data and check bits to over 256K byte mem
	MM504	Data and check bits to over 256K byte mem
	MM505	Data and check bits from over 256K byte mem
	MM515	Data and check bits from over 256K byte mem.
	MM516	Parity check write data from first mem (LED 3)
	MM517	Parity check on over 256K read (LED 4)
02B-A1J2	MM601	Select card 1–(256-288K) FET array (bits 0.0–1.2)
02B-A1J4	MM601	Select card 1–(256-288K) FET array (bits 1.3–1.7 and C1–C6)
02B-A1K2	MM602	Select card 2–(288-320K) FET array (bits 0.0–1.2)
02B-A1K4	MM602	Select card 2–(288-320K) FET array (bits 1.3–1.7 and C1–C6)
02B-A1L2	MM603	Select card 3–(320-352K) FET array (bits 0.0–1.2)
02B-A1L4	MM603	Select card 3–(320-352K) FET array (bits 1.3–1.7 and C1–C6)
02B-A1J2	MM601	Select card 1–(256-288K) FET array (bits 0.0–1.2)
02B-A1J4	MM601	Select card 1–(256-288K) FET array (bits 1.3–1.7 and C1–C6)
02B-A1K2	MM602	Select card 2–(288-320K) FET array (bits 0.0–1.2)
02B-A1K4	MM602	Select card 2–(288-320K) FET array (bits 1.3–1.7 and C1–C6)
02B-A1L2	MM603	Select card 3–(320-352K) FET array (bits 0.0–1.2)
02B-A1L4	MM603	Select card 3–(320-352K) FET array (bits 1.3–1.7 and C1–C6)

02B-A1 BOARD (CARD SIDE)



Card Location	ALD Page	Function
02B-A1M2	MM604	Select card 4–(352-384K) FET array (bits 0.0–1.2)
02B-A1M4	MM604	Select card 4–(352-384K) FET array (bits 1.3–1.7 and C1–C6)
02B-A1N2	MM605	Select card 5–(384-416K) FET array (bits 0.0–1.2)
02B-A1N4	MM605	Select card 5–(384-416K) FET array (bits 1.3–1.7 and C1–C6)

Card Location	ALD Page	Function
02B-A1P2	MM606	Select card 6–(416-448K) FET array (bits 0.0–1.2)
02B-A1P4	MM606	Select card 6–(416-448K) FET array (bits 1.3–1.7 and C1–C6)
02B-A1Q2	MM607	Select card 7–(448-480K) FET array (bits 0.0–1.2)
02B-A1Q4	MM607	Select card 7–(448-480K) FET array (bits 1.3–1.7 and C1–C6)

Card Location	ALD Page	Function
02B-A1R2	MM608	Select card 8–(480-512K) FET array (bits 0.0–1.2)
02B-A1R4	MM608	Select card 8–(480-512K) FET array (bits 1.3–1.7 and C1–C6)
02B-A1U2		Power supply sense and sequence

FET STORAGE DATA FLOW – PART 1

Diagnostic Indicators are for CE Use When Manually Performing the "Storage Test Pattern" or "Single Address Test Pattern" Procedures

CCU
SDR
Store Bits 0.0 – 1.7
0.0
1.7
0.P
1.P
Terminators (Receivers) Parity Check
A2
7
MM104/107
Parity Check CCU Rcv
1
Gate Diag Reg
Control lines
(see 7-240)
Timings, Controls and Resets
G2
MM101

01B-A1 Board (Logic Volume 21)

Diagnostic Register
0.0
1.7
8
G2
MM402
OE for each bit
G2
MM402
Generate Check Bits
9
F2
MM308
C1
C6
AR
G2
MM404
Degate Data to Memory

Data 0.0–1.7 to Mem
AR
C2
MM703
Error Memory Entry (Note 2)
10
PC
H2
MM509
Parity Check on Write-over 256K
C Bits to Mem
C Bits to over 256K Mem
AR
C2
MM703
All bits except C6 are inverted to provide odd parity for checking purposes.

Stored Pulse Delayed
7-230
(Note 1)
Data to over 256K Mem
PC
H2
C2
MM706
OR
Reset Memory

Parity Check Data to over 256K Mem (LED 2)
Parity Check CCU Rcv (LED 1)
(LED 3)
(LED 4)
(LED 5)
ECC Active (LED 6)
Parity Err CCU Drv (LED 7)
Diagnostic Indicator Latches and Drivers
MM404
Storage Panel Diagnostic Indicator LEDs
MM404

9 Check Bit Generation

Data Bit Group	Check Bit
0 1 2 3 4 8 11 13	C1
0 1 2 5 6 7 9 14	C2
3 4 5 6 7 10 12 15	C3
0 3 5 8 9 10 11 12	C4
1 6 8 9 10 13 14 15	C5
2 4 7 11 12 13 14 15	C6

C1=1 whenever an even number of data bits in its associated group are 1s.

3 Read Call Write Call Frame 1
Generate FET Array Gates
Start Read Gate
Delay G2
MM401
Read Gate to ECC
4
Gate CSX
CCU
SAR
X.6
0.0
0.1
1.6
Decode Card Select
1
Power SAR Lines
B2
MM201/207
Card Select 8
Card Select 1
Card Select 1
SAR Bits 0.1–1.6
Address Selection
2
J2/J4
MM601
0-32k
FET Array
J2
FET Array
J4
Data to Mem
Write
11
Data to Mem
C Bits to Mem
3
1.2
1.3
1.7
C1
C6

Data Out
AR
H2
MM501
C1 C Bits Out
AR
H2
MM508
Read Gate to ECC
OR
PC
H2
MM508
OR
12
13
Data from over 256K Mem
9
AR
C2
MM704
7-230
PC
C2
MM707
C Bits from over 256K Mem
11
AR
C2
MM705
7-230

Data Reg
F2
MM302
Error Detection and Single Error Correction
5
F2
MM305
Parity Check Memory Exit (under 256K
OR
14
Parity Check Data from over 256K Mem

Data Bits to CCU
PC
A2
MM106
6
Parity Err CCU Drv
16
Drivers
A2
MM105
Sense Bits 0.0–1.7, 0.P, 1.P to CCU
(To SDR, OP Reg)
Parity Bits to CCU
ECC Active
15

* To other address selection circuits selected by 'card select X'.

The FET array for addresses 0-32k (card select 1) is shown. Seven other FET arrays are possible depending on the address option selected. The data paths and write pulses are parallel to those shown above.

Notes:
1. Errors are inhibited if over 256K is not selected (Volume A21, MM202).
2. For 3705 Models J–L, this line is called "Parity Check on Write to any Mem."

FET STORAGE DATA FLOW—PART 2

Addressing

1 SAR bits X.4, X.5, X.6, X.7, and 0.0 decode into 'card select 1' through 'card select 8'. Each card-select line selects a pair of FET array cards that contain 32k of storage as shown below. With the X.5 bit off, the signal 'read call write call frame 1' is active and selects FET storage located in the base frame. When the X.5 bit turns on, the signal 'read call write call frame 2' selects the FET storage located in the first expansion frame.

SAR Bits X.4	X.5	X.6	X.7	0.0	FET Array Cards Selected	Address Bit Range
0	0	0	0	0	01B-A1 J2/J4	00000 – 07FFF
0	0	0	0	1	01B-A1 K2/K4	08000 – 0FFFF
0	0	0	1	0	01B-A1 L2/L4	10000 – 17FFF
0	0	0	1	1	01B-A1 M2/M4	18000 – 1FFFF
0	0	1	0	0	01B-A1 N2/N4	20000 – 27FFF
0	0	1	0	1	01B-A1 P2/P4	28000 – 2FFFF
0	0	1	1	0	01B-A1 Q2/Q4	30000 – 37FFF
0	0	1	1	1	01B-A1 R2/R4	38000 – 3FFFF
0	1	0	0	0	02B-A1 J2/J4	40000 – 47FFF
0	1	0	0	1	02B-A1 K2/K4	48000 – 4FFFF
0	1	0	1	0	02B-A1 L2/L4	50000 – 57FFF
0	1	0	1	1	02B-A1 M2/M4	58000 – 5FFFF
0	1	1	0	0	02B-A1 N2/N4	60000 – 67FFF
0	1	1	0	1	02B-A1 P2/P4	68000 – 6FFFF
0	1	1	1	0	02B-A1 Q2/Q4	70000 – 77FFF
0	1	1	1	1	02B-A1 R2/R4	78000 – 7FFFF

Note: Storage in frame 02B-A1 is added in increments of 64K bytes.

2 The address selection circuits, selected by 'card select x', decode the selected address from SAR bits 0.1-1.6.

Read Operation

3 The read call portion of the 'read call write call' line occurs during every "A" cycle. The 'read call write call' line generates the 'gate CSX' (chip select x) pulse and the read gate.

4 During a read operation the 'write' pulse is inactive. The 'read gate to ECC' pulse gates the FET array contents (data bits 0.0-1.7 and check bits C1-C6) into the ECC (error correction code) data register. This storage output has odd parity and the parity check line 'parity check memory exit' (Models E—H) turns on diagnostic indicator #5. For Models J—L, a parity check occurring on a read under 256K operation, or a parity check on a read over 256K turns on diagnostic indicator #5. Diagnostic indicator #4 also turns on if a data error is detected during a read over 256K operation. The status of this indicator is updated after each *read* operation.

5 The ECC generates six new check bits from the contents of data register bits 0.0-1.7 and compares these six new check bits with the six check bits in the data register. A syndrome bit is generated for each mismatch of check bits. A syndrome decoder determines if there is (1) no error, (2) a single-bit error, or (3) a double-bit error.

1. No error—data bits 0.0-1.7 are sent to the CCU unchanged. The 'ECC active' diagnostic indicator #6 remains off, or turns off if it was on.
2. Single-bit error—the syndrome decoder determines which data register bit position (0.0-1.7) contains the failing bit from storage and inverts that position's output to the correct level. All other data bits are sent to the CCU unchanged. The 'ECC active' diagnostic indicator # 6 turns on.
   If the failure from storage is a single check bit, no corrections are made but the 'ECC active' diagnostic indicator #6 turns on.
3. Double-bit error—in the event of a double error (either data or check bits), the syndrome decoder:
   a. Blocks error correction, thereby sending the uncorrected bad data to the CCU.
   b. Forces bad parity by inverting parity bits 0.P and 1.P for both bytes of data sent to the CCU. The 'ECC active' diagnostic indicator #6 turns on.

   All other multiple errors that do not look like single data or check bit errors also turn on diagnostic indicator #6.

The status of diagnostic indicator #6 is updated after each *read* operation.

6 Odd parity is generated for both bytes of data sent to the CCU (except in the case of a double-bit error when parity errors are forced). The parity check line 'parity error CCU drivers' turns diagnostic indicator #7 on if there is a parity check on the data to the CCU. The status of diagnostic indicator #7 is updated after each *read* operation.

Write Operation

7 The store bits from the SDR are parity checked at the input to the 01B-A1 storage board only. If bad parity is detected, the 'parity check CCU received' line:

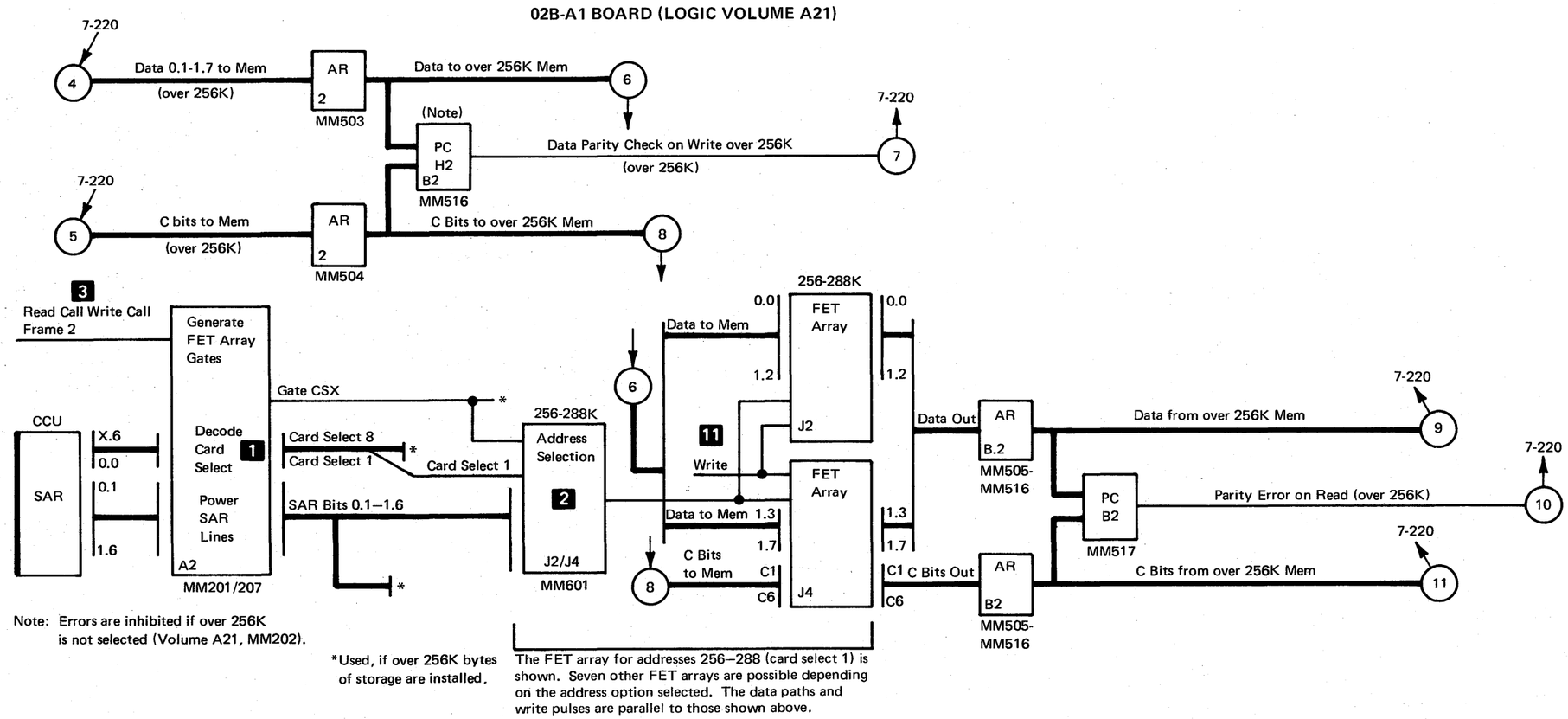
1. Turns on diagnostic indicator #1. The status of this indicator is updated on each *store* operation.
2. Degates 'data 0.0-1.7' and 'C1-C6' bits to storage thereby storing zeros in all bit positions. The syndrome decoder detects this condition as a double-bit error but will detect it only during the next read that occurs at this storage address.

8 The diagnostic register is used by the diagnostic IFTs to validate the storage and error detection/error correction circuitry and to gather statistics on storage errors. See 7-240 for a description of its operation.
When the diagnostic register is reset (all zeros), the store data passes through the exclusive ORs unchanged.

9 Six check bits (C1-C6) are generated from the store data. Bit C6 is inverted to provide odd parity to the next parity checker.

10 The data to be stored in the FET arrays contains 16 data bits and 6 check bits. If bad parity is detected, the 'error memory entry' (Models E—H) line turns on diagnostic indicator #3. For Models J—L, a parity check occurring on a write operation to any memory, or a parity check on a write over 256K operation turns on indicator #3. Diagnostic indicator #2 also turns on if a data error is detected during a write over 256K operation. The status of this indicator is updated on each *store* operation.

11 To store data in the FET arrays, the 'write' line must be active when the selected address is active. The 'store new' signal from the CCU generates the 'write' line (see 7-240).
The write call portion of the 'read call write call' line occurs during "C" cycle, but only when a store operation is required. Except for the timing, the address selection for the write operation is similar to that for the read operation.



STO

FET STORAGE DIAGNOSTIC REGISTER OPERATION

A sixteen bit diagnostic register on the control card (01B-A1G2) aids the IFTs in validating the operation of the error detection/error correcting circuitry and in gathering storage error statistics. The output of the diagnostic register is exclusive ORed with the corresponding store bits from the SDR (see 7-220). When a "test mask" (combinations of ones and zeros) is set in the diagnostic register, each one causes an inversion of the corresponding bits in the store data while zeros pass the store data unchanged.

Setting the Diagnostic Register

1 An Output X'79' with bits 0.3 and 1.2 = 1 sets the 'allow set memory diag reg' latch and 'test mode' latch respectively.

2 The test mode latch turning on removes the resets to the diagnostic register and to the 'allow set memory diag reg' latch.

3 'Allow set memory diag reg' brings up 'degate data to mem' that inhibits the store data and C bits from being written into the FET array.

4 Any store instruction may be executed to store the "test mask" data in the diagnostic register (this example uses the STH (store halfword) instruction). The data at the storage address is not changed during this operation. An installed address must be used to prevent address exception checks.

5 During the I2 cycle of the STH instruction, 'mem store new' arms the 'allow set memory diag reg' latch so that the next 'mem reset' pulse can reset the latch.

6 'Store new' brings up (1) 'gate diag reg' that sets the store data (test mask) in the diagnostic register, (2) 'write', and (3) 'gate CSX' (used for address selection).

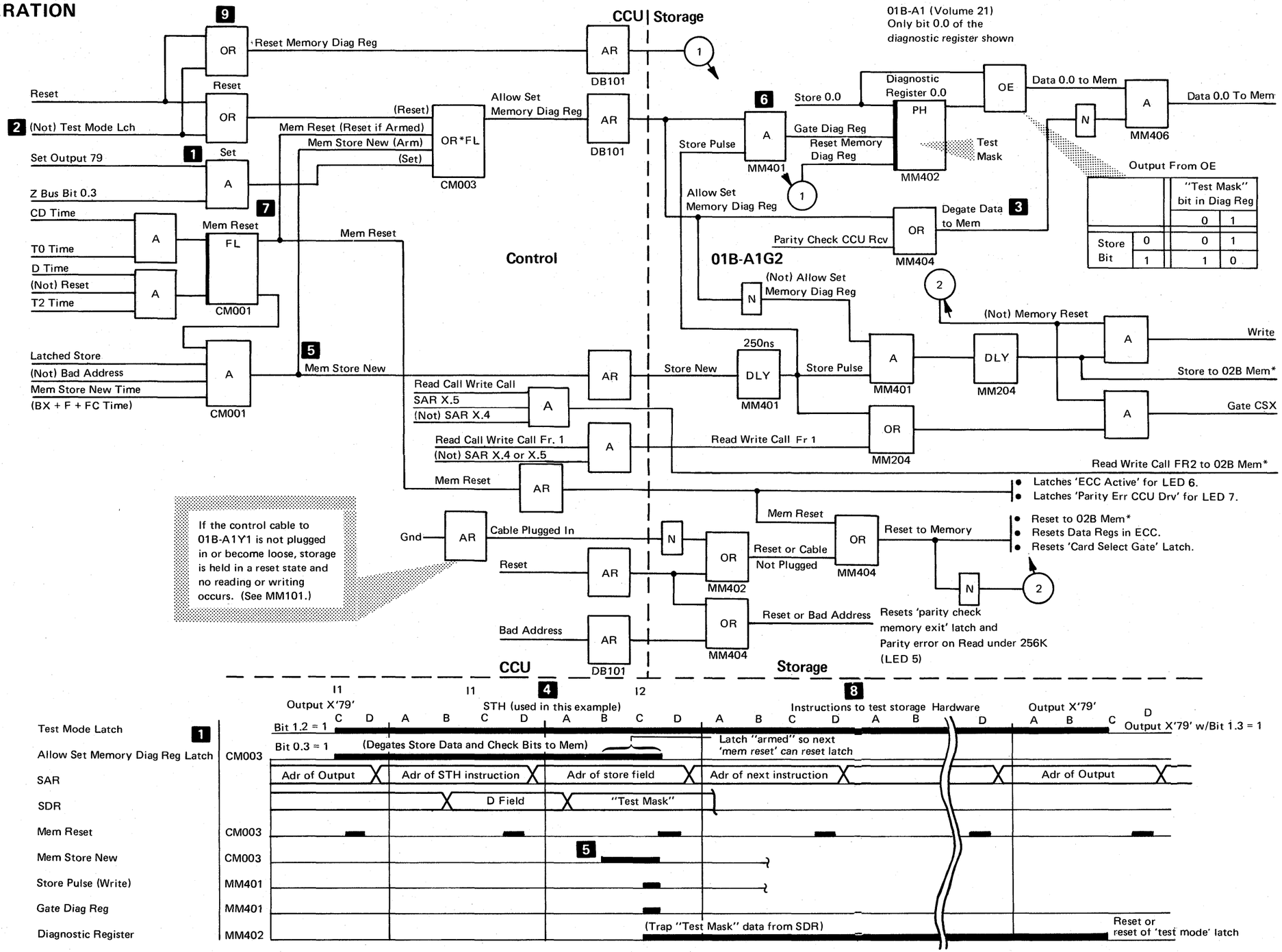
7 The next 'mem reset' pulse resets the 'allow set memory diag reg' latch.

8 The IFTs use the test mask bit pattern in the diagnostic register to force single-bit errors, double-bit errors etc. to validate the ECC (error correction code) circuitry and to gather statistics on storage errors.

Resetting the Diagnostic Register

9 The diagnostic register resets (1) on a machine reset, (2) when the test mode latch is turned off (output X'79' with bit 1.3 = 1), or (3) after being set with all zeros.

*Only when storage installed is greater than 256K bytes.



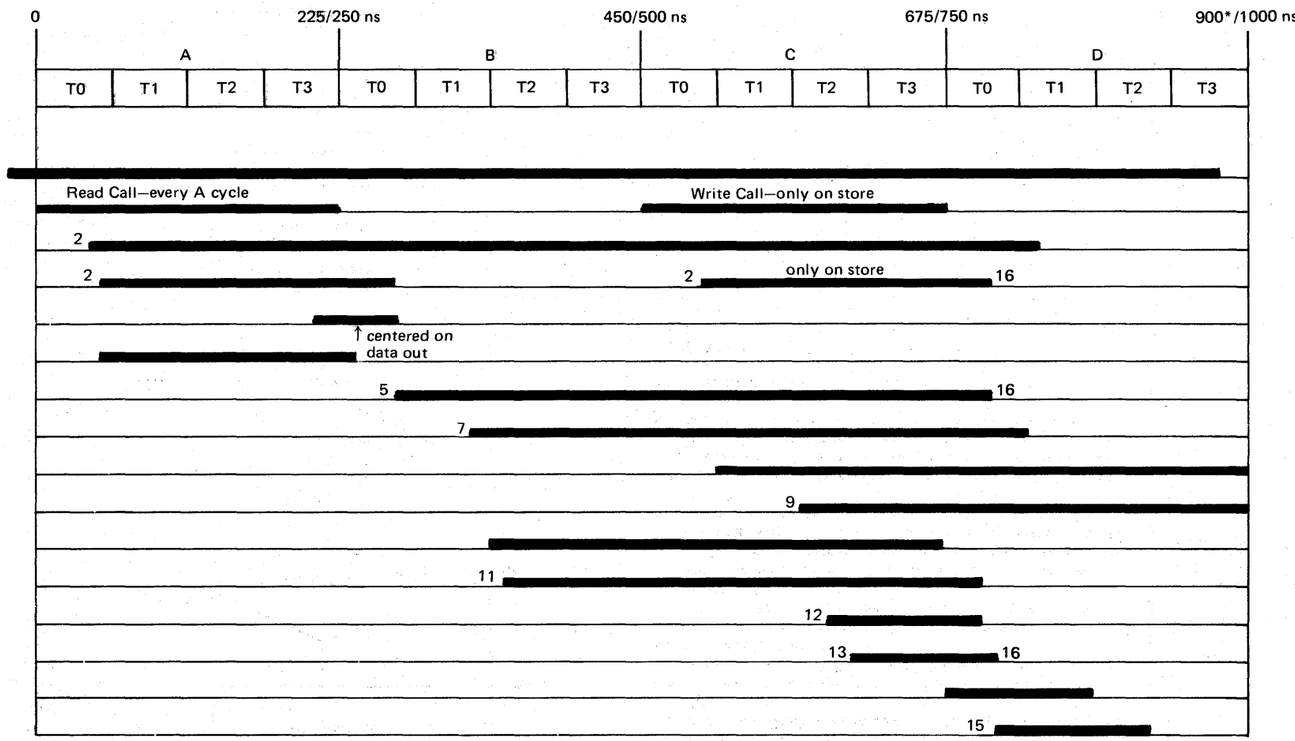
FET STORAGE TIMING CHART

Volume 21 contains FET logic for frame 01B
(Up to and including 256K).

Volume A21 contains FET logic for frame 02B
(Over 256K up to 512K).

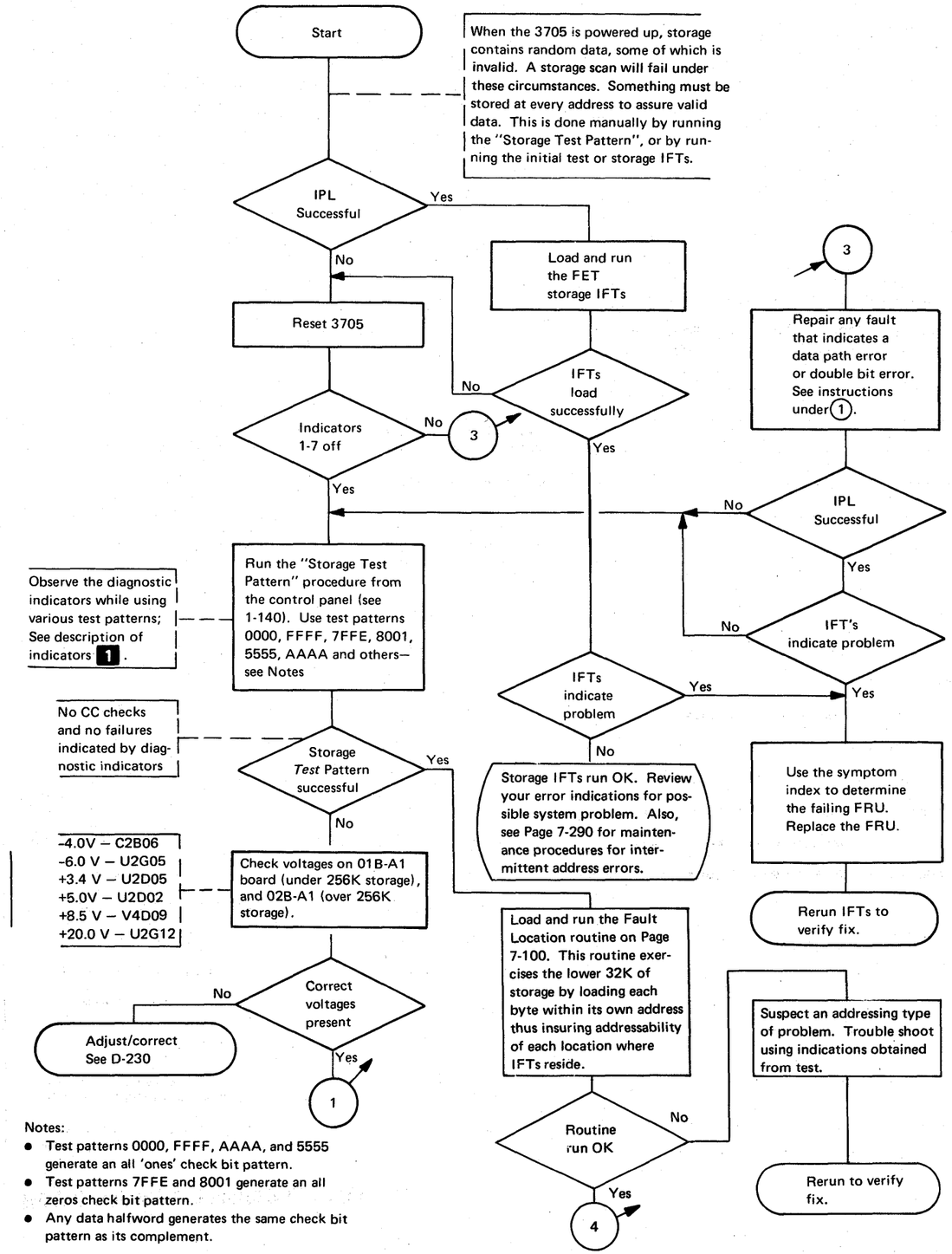
	Line Description		Logic	Pin Locations
1	SAR (Vol. 21 and A21)		MM201	Note 1
2	Read Write Call (Vol. 21 and A21)		MM201	Cannot scope
3	Card Select X (Vol. 21 and A21)		MM203	Note 1
4	Gate CSX (Vol. 21 and A21)		MM204	Note 2
5	Data Out (from FET arrays) (Vol. 21 and A21)		MM60X	Note
6	Read Gate to ECC (Vol. 21 only)		MM401	01B-A1G2G03
7	Data Register Output (Vol. 21 only)		MM302	Cannot scope
8	Sense Bits		MM103	Note
9	Store Bits		MM102	Note
10	Data to Memory (Vol. 21 and A21)		MM60X	Note
11	Memory Store New (Vol. 2)		CM001	01A-B3T4B05
12	Store New (Vol. 21 only)		MM101	01B-A1A1E11
13	Store Pulse	(Vol. 21 only)	MM401	01B-A1G2U06
		(Vol. 21 only)	MM401	01B-A1G2S07
		(Vol. A21 only)	MM504	02B-A1B2J02
14	Write (Vol. 21 and A21)		MM204	Note
15	Memory Reset (Vol. 2)		CM001	01A-B3T4D09
16	Reset to Memory	(Vol. 21 only)	MM404	01B-A1G2U05
		(Vol. 21 only)	MM404	01B-A1LU05
		(Vol. A21 only)	MM503	02B-A1B2D05

STORAGE CYCLE



Notes:
1. See the logic page for the pin location of a specific bit position.
2. See the logic page for the pin locations of this multi-output pulse.

*900 nanosecond cycle time is a standard feature only on 3705-II Models J-L.



Notes:

- Test patterns 0000, FFFF, AAAA, and 5555 generate an all 'ones' check bit pattern.
- Test patterns 7FFE and 8001 generate an all zeros check bit pattern.
- Any data halfword generates the same check bit pattern as its complement.

1

Use the following procedure to verify the operation of FET storage support circuitry.

Run the "Single Address *Test* Pattern" from the control panel (see 1-150 for procedure). Select an address in the first 32k of storage. See logic reference page MM002 for the card select addressing chart and storage data flow diagram. Use test patterns such as 0000, FFFF, 5555, AAAA, 7FFE, 8001 and observe the diagnostic indicator lights on the storage panel.

CAUTION

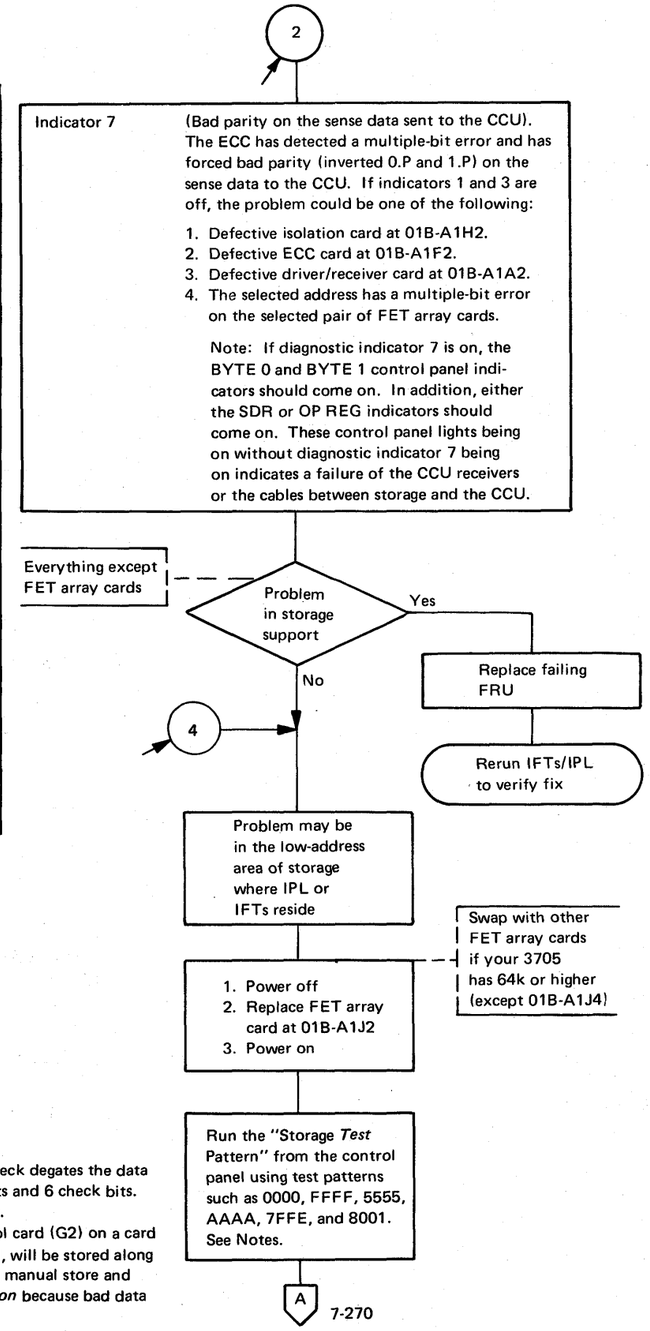
1. Indicators 1 and 3 are updated on each store operation. Indicators 5, 6, and 7 are updated on each read operation.
2. Every "A" cycle is a read cycle using whatever address is in SAR, even though stopped.
3. Store errors (indicators 1 or 3 on) do not interrupt CCU activity and the bad data is stored in the FET arrays.
4. Priority for trouble shooting should be indicators 1, 3, 5, and 7.

1

Indicator 1	(Bad parity on the data received from the CCU). This indicates that the problem is (1) in the CCU (2) in the cables between CCU and storage, or (3) a defective card at 01B-A1A2, G2 (data stored is X'0000'), or F2.
Indicator 2	Indicates bad parity on the 22 store/check bits to be stored. Only activated if over 256K storage is being accessed. Diagnostic indicator #3 also turns on.
Indicator 3	(Bad parity on the 22 store/check bits to be stored). If indicator 1 if off, the problem is a defective card(s) at 01B-A1F2, H2, G2, or A2.
Indicator 4	Indicates bad parity on the 22 data-out/check bits from the over 256K FET memory. Note: (If indicator 4 comes on while under 256K storage is being used, it indicates hot bits are present at the outputs of the over 256K arrays.) Diagnostic indicator #5 also turns on.
Indicator 5	(Bad parity on the 22 data-out/check bits from the FET arrays). If indicators 1 and 3 are off, a single-bit error on the data read from the FET arrays has occurred. If this occurs only at random addresses, this does not necessarily indicate an operational problem since single-bit errors are corrected by the ECC (error correction code) circuitry. However, if this occurs on all installed addresses, you should suspect a "hot" zero or one bit from the isolation card at 01B-A1H2.
Indicator 6	(ECC is active). The ECC has either corrected a single-bit error or has detected a double-bit error.

2

Indicator 7	(Bad parity on the sense data sent to the CCU). The ECC has detected a multiple-bit error and has forced bad parity (inverted 0.P and 1.P) on the sense data to the CCU. If indicators 1 and 3 are off, the problem could be one of the following: 1. Defective isolation card at 01B-A1H2. 2. Defective ECC card at 01B-A1F2. 3. Defective driver/receiver card at 01B-A1A2. 4. The selected address has a multiple-bit error on the selected pair of FET array cards. Note: If diagnostic indicator 7 is on, the BYTE 0 and BYTE 1 control panel indicators should come on. In addition, either the SDR or OP REG indicators should come on. These control panel lights being on without diagnostic indicator 7 being on indicates a failure of the CCU receivers or the cables between storage and the CCU.

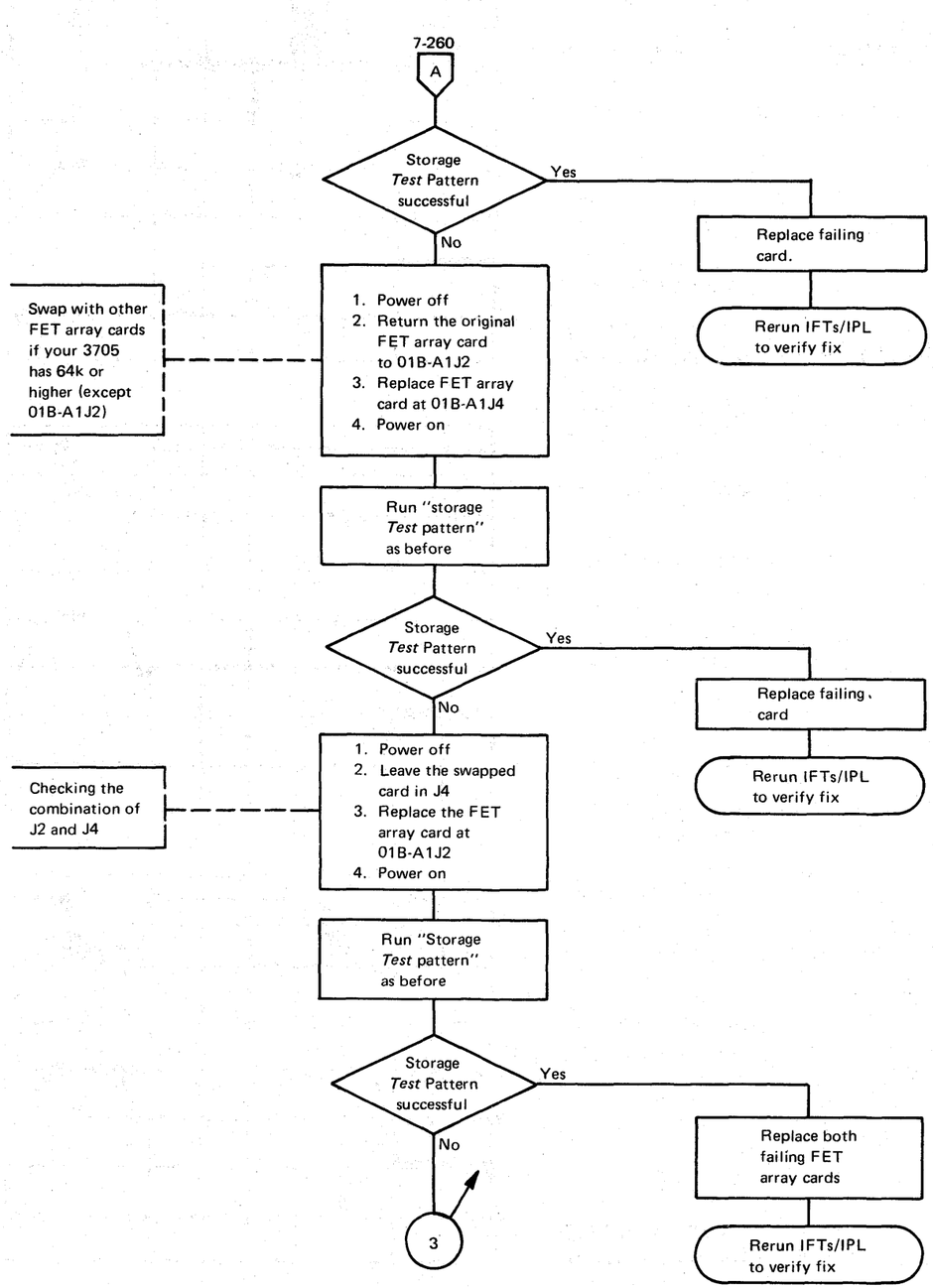


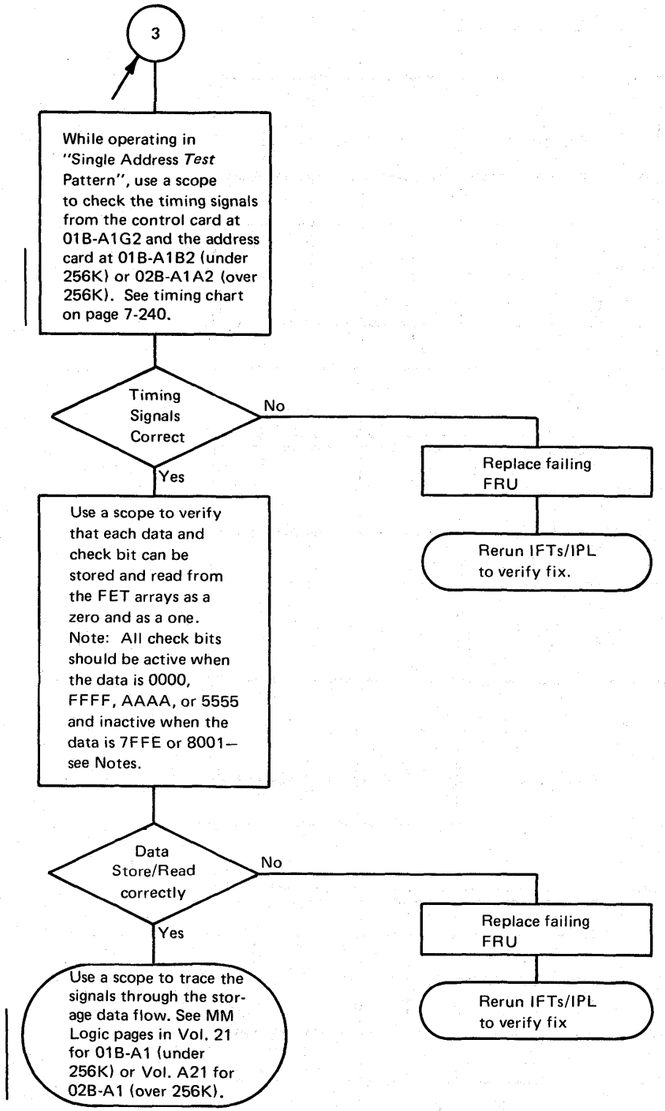
Service Aid

When FET storage detects bad parity on the data from the CCU, the parity check degates the data and check bits to storage. This forces all zeros to be stored for the 16 data bits and 6 check bits. This all zero pattern is detected as a multiple-bit error when read from storage.

To disable the degating of the data and check bits, place the storage control card (G2) on a card extender and "float" pin 01B-A1G2U02. The data, as received from the CCU, will be stored along with the generated check bits and can be observed on the display lights during manual store and display operations. This service aid *must not be used during customer operation* because bad data will have good parity generated and stored.

FET STORAGE MAINTENANCE PROCEDURE—PART 2

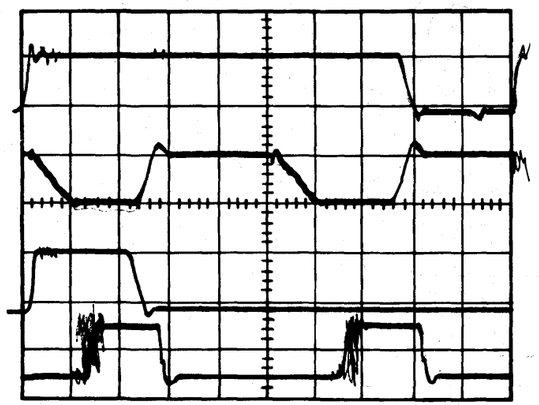




Notes:

- Test patterns 0000, FFFF, AAAA, and 5555 generate on all 'ones' check bit pattern.
- Test patterns 7FFE and 8001 generate an all zero check bit pattern.
- Any data halfword generates the same check bit pattern as its complement.

FET STORAGE TEST PATTERNS



READ/WRITE CYCLE–USING STORAGE TEST PATTERN

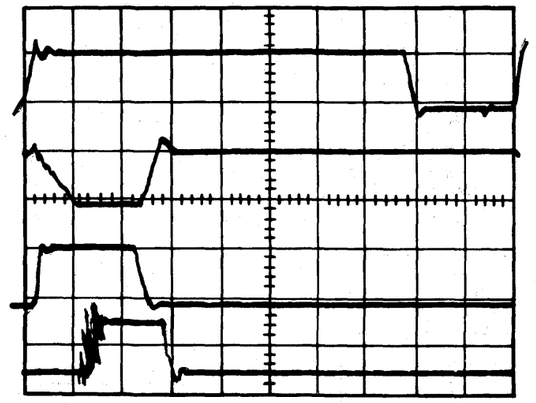
+ Gate card select (B2D13)

- Gate CSX A1 (B2S12)

+ Read gate to ECC (G2G03)

+ Bit 0.0 from memory (F2S13) (Bit 0.0 active)

Scope settings: 1 V/cm
100 nsec/cm



READ CYCLE – USING STORAGE SCAN

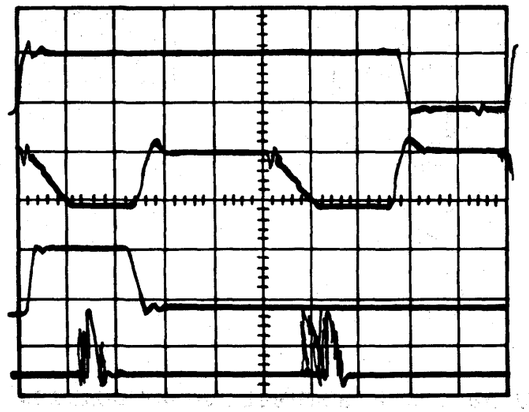
+ Gate card select (B2D13)

- Gate CSX A1 (B2S12)

+ Read gate to ECC (G2G03)

+ Bit 0.0 from memory (F2S13) (Bit 0.0 active)

Scope settings: 1 V/cm
100 nsec/cm



READ/WRITE CYCLE–USING STORAGE TEST PATTERN

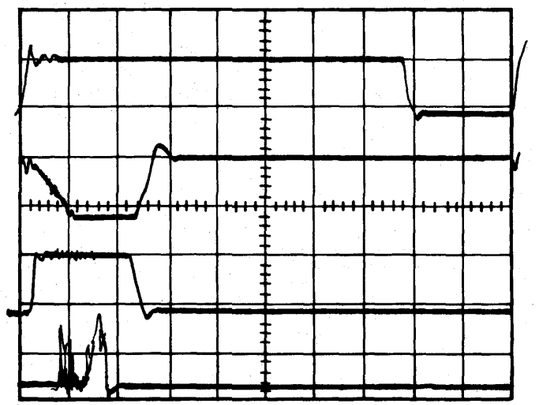
+ Gate card select (B2D13)

- Gate CSX A1 (B2S12)

+ Read gate to ECC (G2G03)

+ Bit 0.0 from memory (F2S13) (Bit 0.0 Inactive)

Scope settings: 1 V/cm
100 nsec/cm



READ CYCLE–USING STORAGE SCAN

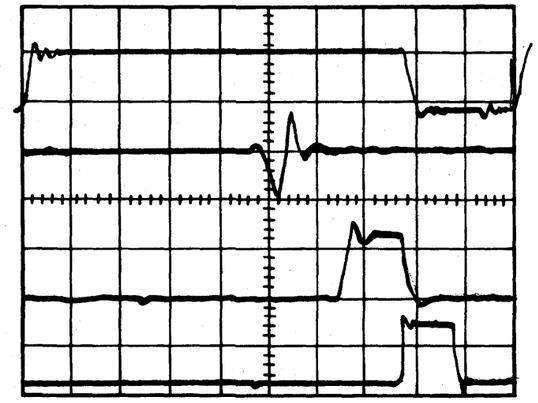
+ Gate card select (B2D13)

- Gate CSX A1 (B2S12)

+ Read Gate to ECC (G2G03)

+ Bit 0.0 from memory (F2S13) (Bit 0.0 inactive)

Scope settings: 1 V/cm
100 nsec/cm



WRITE CYCLE–USING STORAGE TEST PATTERN

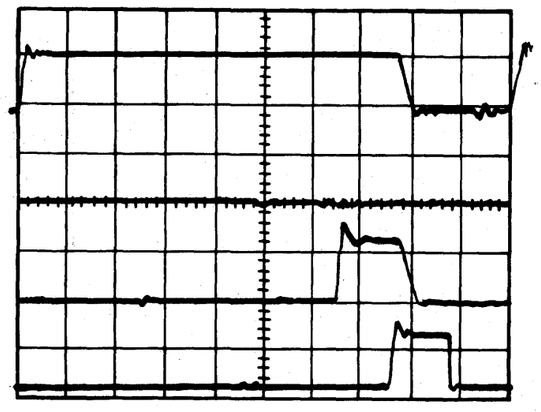
+ Gate card select (B2D13)

+ Data 0.0 to memory (J2J13) (Bit 0.0 active)

+ Write A1 (J2J10)

+ Reset to memory (G2U05)

Scope settings: 1 V/cm
100 nsec/cm



WRITE CYCLE–USING STORAGE TEST PATTERN

+ Gate card select (B2D13)

+ Data 0.0 to memory (J2J13) (Bit 0.0 inactive)

+ Write A1 (J2J10)

+ Reset to memory (G2U05)

Scope settings: 1 V/cm
100 nsec/cm

MAINTENANCE PROCEDURE — INTERMITTENT FET STORAGE ADDRESS ERRORS

Use these procedures to trap the failing storage address if the FET storage diagnostics and maintenance procedures do not indicate a problem. These procedures should be used to isolate the problem to a 32K increment of storage so it can be replaced as a last resort.

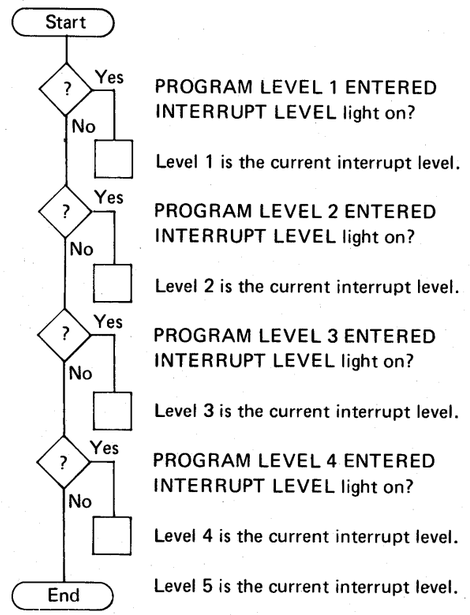
Procedure A — use this procedure if the 3705 does not have any adapters that cycle steal (that is Type 2 CA, Type 3 CA, Type 4 CA using ACF/NCP/VS or higher, or the Type 3 scanner).

Procedure B — use this procedure whenever procedure A does not apply.

PROCEDURE A

(Used when 3705 does not have adapters that cycle steal.)

1. Set the DIAGNOSTIC CONTROL switch to CC CHECK HARDSTOP.
2. Load the EP or NCP and then start the normal operation.
3. If a storage error occurs, the 3705 will hardstop from a CC check with the OP REG or SDR check light on.
4. If the SDR check light is on, go to step 6.
5. If the OP REG check light is on, the failing storage address is two less than the contents of TAR.
6. If the OP REG contains a "Load Address" or "Branch and Link" instruction, the failing storage address is two less than the contents of TAR. See Page 6-150 for instruction decoding.
7. The failing instruction will be displayed in the OP REG and should be an ICT, STCT, IC, STC, LH, L, or ST instruction. See Page 6-150 for instruction decoding.
8. If the B field of the instruction (byte 0, bits 1, 2, and 3 of the OP REG) is 000, the failing storage address is in the first 32K increment.
9. Record the displacement field from the failing instruction displayed in the OP REG.
10. Determine the current program interrupt level by using the following procedure:



11. Use the B field of the instruction (byte 0, bits 1, 2, and 3 of the OP REG) and the current interrupt level to determine, from the following chart, the register address to be used to display the contents of the Base Register.

Register Address to Display Base Number

B Field	Current Interrupt Level				
	1	2	3	4	5
001	01	01	09	11	19
010	02	02	0A	12	1A
011	03	03	0B	13	1B
100	04	04	0C	14	1C
101	05	05	0D	15	1D
110	06	06	0E	16	1E
111	07	07	0F	17	1F

Set this register address in ADDRESS/DATA switches B and D and display the base number.

12. The failing storage address is obtained by adding (hex) the displacement field (from step 9) to the base number (from step 11). For the ICT and STCT instructions, the failing storage address is one less than the calculated value. For the L instruction, the address may be two more than the calculated value.

    Note: If the R or R, N field specifies the same register as the B field, this procedure will not work. Use Procedure B if necessary.

PROCEDURE B

(Used when Procedure A does not apply.)

1. Obtain two MST-1 CE Indicator Latch Cards, P/N 5851882, and install on boards 01A-B3 or B4 (only one latch card is needed if your 3705 is not over 64K). See Page 1-201 for a description of the use of the latch cards.
2. Jumper pin Q of the latch card(s) to pin 01A-B3N2J06 (-Mach Check)—ALD page CK006. This holds the latch cards reset until a machine check occurs.
3. Jumper pin F of latches #1, #2, #3, and #4 to 01A-B3R2G10 (-CD Time)—ALD page CC001.

    Note: Latches #1,and #2 are both on latch card #1.
    Latches #3 and #4 are on latch card #2.

4. Jumper pin E of latches #1, #2, #3 and #4 to 01A-B3P2J05 (-Program Stop Latch)—ALD page CU004.
5. Jumper pin D of latch #1 to 01A-B4E2U02 (+SAR Bit 0.0)—ALD page CM002.
6. If 64K or lower, go to Step 10.
7. Jumper pin D of latch #2 to 01A-B4E2M13 (+SAR Bit X.7)—ALD page CM002.
8. Jumper pin D of latch #3 to 01A-B4E2S03 (+SAR Bit X.6)—ALD page CM 002.
9. Jumper pin D of latch #4 to 01A-B4E2J13 (+SAR Bit X.7)—ALD page CM002.
10. Reset the latch card(s) and set the DIAGNOSTIC CONTROL switch to CC CHECK HARD STOP.
11. Load the EP or NCP and then start the normal operation.
12. If a storage error occurs, the 3705 will hardstop from a CC check with the OP REG or SDR check light on.
13. Determine the failing 32K storage increment using the following chart.

Latch 4 (X.5)	Latch 3 (X.6)	Latch 2 (X.7)	Latch 1 (0.0)	Failing Storage Increment
OFF	OFF	OFF	OFF	1—32K
OFF	OFF	OFF	ON	32K—64K
OFF	OFF	ON	OFF	64K—96K
OFF	OFF	ON	ON	96K—128K
OFF	ON	OFF	OFF	128K—160K
OFF	ON	OFF	ON	160K—192K
OFF	ON	ON	OFF	192K—224K
OFF	ON	ON	ON	224K—256K
ON	OFF	OFF	OFF	256K—288K
ON	OFF	OFF	ON	288K—320K
ON	OFF	ON	OFF	320K—352K
ON	OFF	ON	ON	352K—384K
ON	ON	OFF	OFF	384K—416K
ON	ON	OFF	ON	416K—448K
ON	ON	ON	OFF	448K—480K
ON	ON	ON	ON	480K—512K

TYPE 1 CHANNEL ADAPTER

(NOT AVAILABLE FOR 3705-II MODELS J-L)

INTRODUCTION

The type 1 channel adapter (CA) handles data transfers between the 3705 and the channel with the CCU interrupt facilities. This adapter accepts a range of subchannel addresses and commands consistent with the IBM 2701, IBM 2702, and IBM 2703 transmission control units. However, the 3705 must be assigned a single subchannel address to be used when the 3705 is not emulating one of the other transmission control units.

The range of subchannel addresses and commands enables the 3705 to emulate the other IBM control units under program control.

Unlike the type 2 channel adapter, the type 1 channel adapter does not cycle steal data into storage. This adapter requires control program intervention for each inbound and outbound data transfer.

Data transfers between the channel and the channel adapter are controlled by the data/status control register. Up to four bytes can be transferred (byte count in status control register) before the control program intervenes in the operation. However, each 4 byte transfer requires control program intervention before and after the transfer.

If a type 2 channel adapter is installed in the 3705 configuration with the type 1 CA, both channel adapters can transfer data simultaneously.

CHANNEL ADAPTER MODES OF OPERATION

The type 1 channel adapter operates in either native subchannel (NSC) or emulation subchannel (ESC) mode. The 3705 control program selects the mode with an Output X'67' instruction (see 8-130). NSC mode uses a single channel address for each channel interface installed, and must be used in the initial program load. The 3705 control program handles line control and message assembly while operating in this mode.

ESC mode uses a range of addresses assigned to each communication line attached to the 3705. The host CPU is responsible for line control while operating in this mode. ESC mode is used when IBM 2701, 2702, or 2703 operation is emulated.

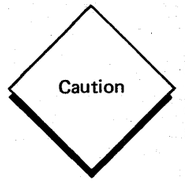
ADDRESS ASSIGNMENT

During initial selection, the channel adapter must be able to recognize the I/O device address presented on the channel bus-out if the channel interface is enabled. Since the type 1 CA can have a NSC address and a range of ESC addresses, alternate means of assigning the addresses are provided.

The NSC address is assigned on the plug card at Y4P2, RC104. The NSC address can be any address from 0 to 255. If the Two Channel Switch feature is installed, NSC addresses for interface A and B are assigned by different plug cards (A on Y4P2, B on Y4R2, RF106, Y4P2 is an address source for the control program). The 2 NSC addresses need not be identical.

ESC addresses are assigned on the plug card at Y4M2, RC302-305, and are a contiguous group of addresses. The lowest address in the group can be 0 or any multiple of 16 from 0 to 240. The highest address that can be assigned must be greater than the lowest address and 1 less than an even multiple of 4 from 3 to 255. The range of addresses can be set to include a minimum of 4 and a maximum of 256 addresses. The range of addresses must be the same for both interfaces if the Two Channel Switch feature is installed.

Refer to FEALD YZ000 pages 10-13 for I/O channel address address jumpering.

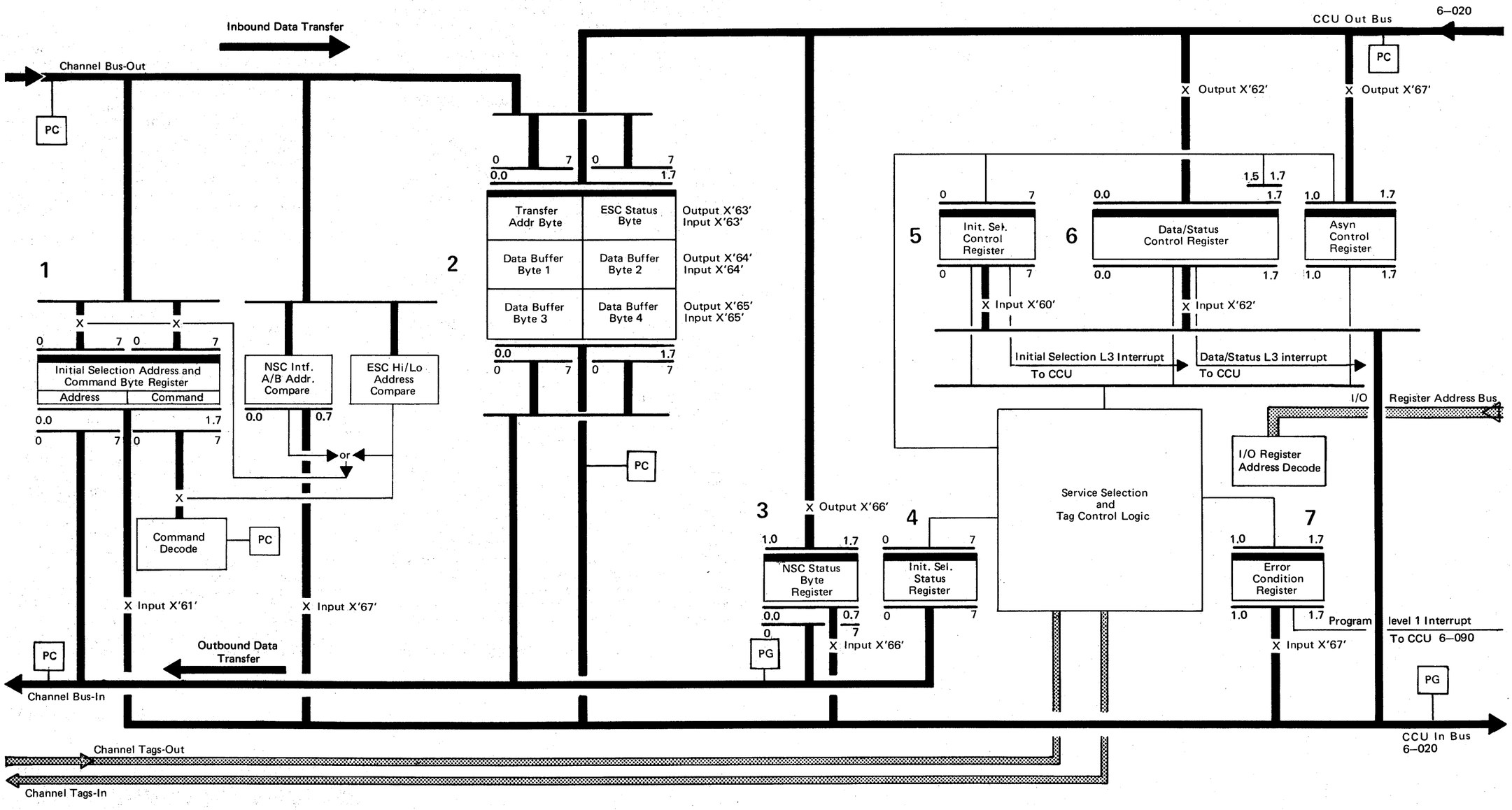


The hard stop latch disables the channel interface without extinguishing the interface enabled light. The channel adapter does not recognize its address and trap select out if the hard stop latch is set.

CHANNEL COMMANDS

The type 1 channel adapter initially accepts as a valid command any configuration from X'00' to X'FF'. The only limitation is that the command byte must be in parity on the channel. The channel adapter presents an initial status of X'00' if the parity is correct and the command is not a No-Op, an ESC Test I/O, or a Start I/O clearing NSC stacked status. The CA then requests an initial selection level 3 interrupt so that the control program can further determine if the command is valid for the subchannel address the command was issued to. If the command is not valid for that address (determined by the control program), the CA presents CE, DE, and UC status to the channel under program control.

TYPE 1 CA DATA FLOW



TYPE 1CA DATA FLOW (PART 2)

1 INITIAL SELECTION ADDRESS AND COMMAND REGISTER

This register contains the I/O device address byte and command byte presented to the channel adapter during initial selection. The register can be accessed by Input X'61' which should be executed only if the type 1 channel adapter initial or data/status level 3 interrupt request is set. See 8-070 for Input X'61' description. This register is referred to as the SIO register in the ALD's.

2 LOCAL STORE

The local store provides buffering for the I/O address byte used in all data and status transfer sequences initiated by the 3705. Buffering for up to four bytes of data for inbound and outbound data transfers is provided here also.

The control program loads or accesses the I/O device address and the emulation status byte with Output X'63' and Input X'63' respectively. The data bytes are transferred with X'64' or X'65' instructions, see chart below.

Data Byte	Data Transfer	
	Out	In
1	X'64'	X'64'
2	X'64'	X'64'
3	X'65'	X'65'
4	X'65'	X'65'

3 NSC STATUS BYTE REGISTER

The current status of the NSC is maintained in this register and gated over the channel interface during NSC status transfer sequences. The control program should set the NSC status by executing an Output X'66' instruction. The control program has access to this register with the Input X'66' instruction.

4 INITIAL SELECTION STATUS REGISTER

The status byte is generated and presented to the channel from this register during initial selection sequences except under the following conditions.

- An initial selection sequence occurs for the native mode subchannel before the NSC status byte provided by the control program has been accepted. The NSC status byte from the NSC status register is presented instead of the hardware generated status.
- An initial selection sequence occurs for an emulation address when the control program has signaled that an ESC status transfer sequence is required and has signaled that ESC Test I/O status is available. The ESC status byte provided by the program is presented instead of hardware generated status.

5 INITIAL SELECTION CONTROL REGISTER

The information in this register identifies the event causing the type 1 channel adapter initial level 3 interrupt request to be set. The register can be accessed by Input X'60', which should be executed only if the interrupt request is set.

6 DATA/STATUS CONTROL REGISTER

The information in this register controls and identifies events that cause the type 1 channel adapter data/status level 3 interrupt request to be set. The register can be accessed by Input X'62', which should be executed only if the interrupt request is set. The control program can perform various control functions by setting or resetting bits in this register with an Output X'62' instruction. The instruction should be executed only when the control program is servicing a type 1 CA level 3 interrupt request.

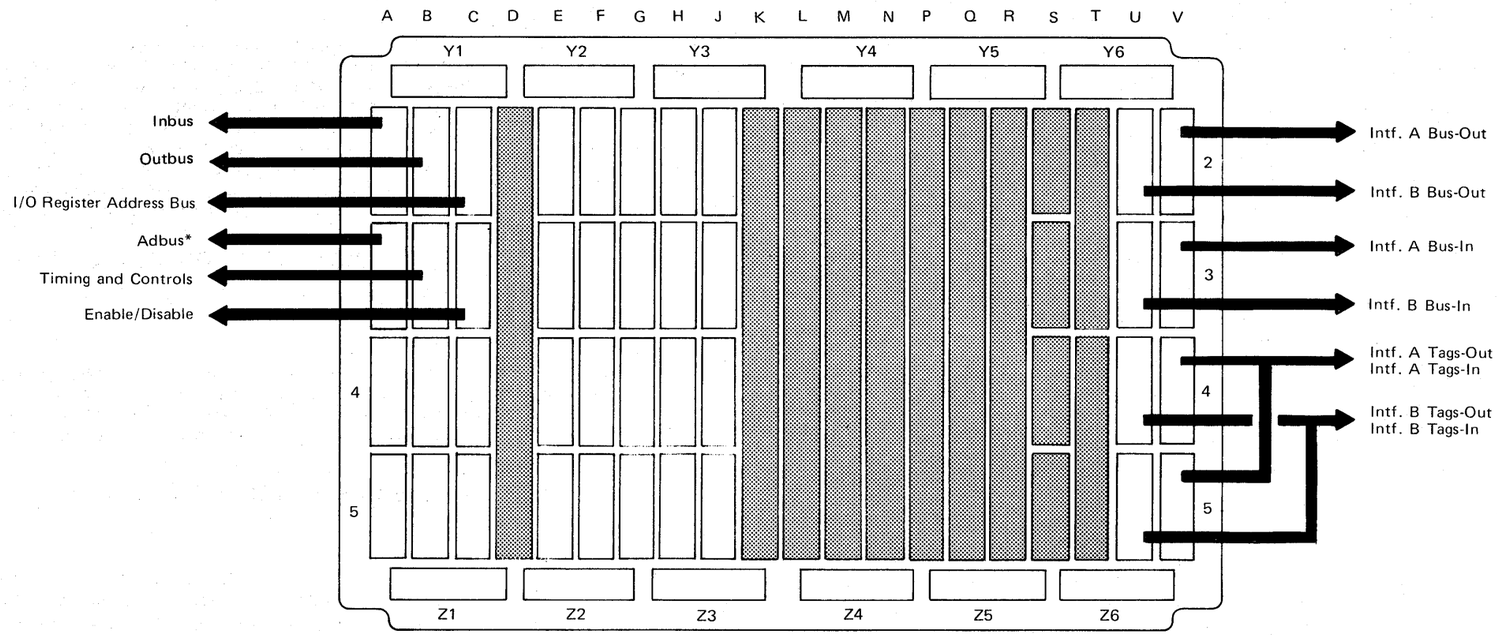
7 ERROR/CONDITION REGISTER

The error/condition register is a collection of latches that are set when the CA detects an error or an occurrence of specific asynchronous conditions. The 3705 control program has access to this register with an Input X'67' instruction, (see page 8-140). The errors indicated by the error/condition register cause type 1 CA error interrupts (see page 8-360).

CARD FUNCTIONS AND LOCATIONS

Card Loc.	ALD Page	Function
Y4D2	RA101	I/O Decodes (Type 1 Scanner and CA) I/O Feedback L1 Bid Basic Clocking **Inbus Doting** **Inbus Gating**
Y4P2	RC101	Chan. Intf. Tags and Control Chan Intf A Receivers Intf. A control **Channel Address Jumper** Channel Address Parity Check Local Store Assembler Byte 0 Local Store Byte 0 Intf B Address
Y4N2	RC201	Tag Control Clock Tag Control, Start I/O and Op-In Tag Control Tag In latches Tag Control stack chaining stop or Halt I/O Tag Control Enable and Sel. Sys Reset Tag Control Powering
Y4M2	RC301	Bus-Out Repowering Low Address Jumpering Low Address Logic High Address Jumpering High Address Logic Start I/O and Command Registers Local Store Byte 1 Command Decode **Outbus Inversion**
Y4L2	RC401	**Outbus Termination** Initial Selection Control Service Transfer Control Byte Count Initial Status Generation
YAK2	RC501	Input/Output Control Assembler and Local Store control Asynchronous Interrupt control NSC Control RN Asynchronous Information Error Latches
Y4T2	RC601	NSC Status Register Asynchronous Interrupt Control
Y4T4	RC801 RC802	Interface A Select Out Relay Interface B Select Out Relay
Y4Q2	RC701	Bus-In Drivers Intf. A Tag-In Drivers Intf. A Select Out Relay Driver and Control gates Bus-In Error Latch
Y4R2	RF101	Intf. B Receivers
Y4S2	**RF201**	**Bus-In Drivers, Intf. B** **Tag-In Drivers Intf. B** **Select Out Relay and Control Gates** **Bus In Error Latch**

This board also houses the Type 1 Communication Scanner.



01A-Y4 **Board
CARD SIDE

*The Adbus is not used with the Type 1 Channel Adapter.

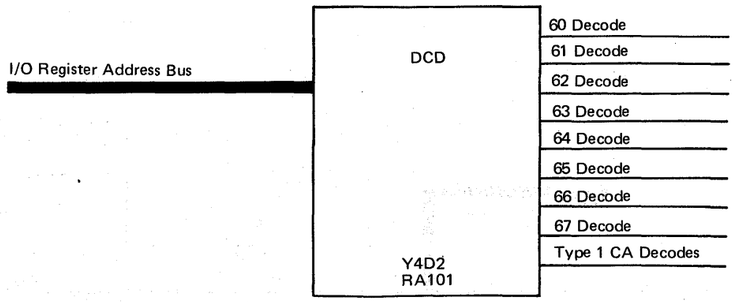
** Y4 is the psuedo board location for the Type 1 Channel Adapter. The actual board location is 01A-A4.

INPUT AND OUTPUT INSTRUCTIONS

The type 1 channel adapter relies on the 3705 control program to use input and output instructions to control data transfers. The control program initiates channel data and status transfers, and transfers data between the CA and the CCU with input and output instructions.

Each input or output instruction addresses an external register. The input instructions gate the external register to CCU general registers via the CCU Inbus. Output instructions gate CCU general registers to CA registers via the CCU Outbus. The 'I/O register address bus' is decoded in the type 1 attachment base which is shared with the type 1 communication scanner.

Executing an Input or Output X'60', X'61', X'62', X'63', X'64', X'65', or X'66' when the CA is actively handling a data or status transfer sequence causes an in/out check to occur; see 8-360.



I/O Reg Bus Bits							Decode
1	2	3	4	5	6	7	
1	1	0	0	0	0	0	60
1	1	0	0	0	0	1	61
1	1	0	0	0	1	0	62
1	1	0	0	0	1	1	63
1	1	0	0	1	0	0	64
1	1	0	0	1	0	1	65
1	1	0	0	1	1	0	66
1	1	0	0	1	1	1	67

CONTROL PANEL ACCESS TO CA REGISTERS

Type 1 CA registers X'60' through X'66' should be accessed from the control panel with Input or Output instructions only when either of the type 1 CA level 3 interrupts are pending.

To ensure that this interrupt remains pending, the 3705 should be in either Program Stop or Hard Stop mode before these instructions are executed from the control panel.

If these conditions are not met, the following occurs:

1. If the type 1 CA is in the process of a data or status transfer sequence and an Input or Output X'60' through X'66' is initiated from the control panel, the type 1 CA hardware:
   a. Causes a type 1 CA level 1 interrupt request.
   b. Sets the type 1 CA In/Out instruction accept latch.
   c. Gates X'0000' onto the CCU Inbus to be displayed in display B if the instruction is an Input.
   d. Does not recognize Output instructions.

2. If the type 1 CA is not transferring data or status and a type 1 CA level 3 interrupt request is not pending, one of the following occurs:
   a. For Input X'60', X'61', or X'66' instructions, either the instruction is executed without error or, if at the same time the instruction is being executed, the CA is being selected by the host CPU channel, the CCU may sample invalid data from the type 1 CA. The data in display B should be considered invalid.
   b. For Output X'66' instructions, either the instruction is executed without error or, if at the same time the instruction is being executed, the type 1 CA is being selected by the host CPU channel, a type 1 CA channel bus in check and a type 1 CA level 1 interrupt request may be set or a CPU data check may be detected at the host CPU.

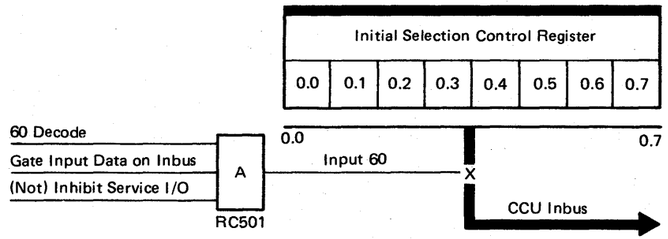
3. If the type 1 CA is in the process of presenting ESC status to a Test I/O issued to an ESC address, and an Input X'60' through X'66' or an Output X'62' through X'66' is executed, one of the following occur:
   a. The instruction executes without error.
   b. If at the same time any of these instructions are being executed, the type 1 CA is being selected by the host CPU channel, either a type 1 channel bus in check, a type 1 CA local store, a level 1 interrupt request, or a CPU data check may occur.

Input and Output X'67' can be executed from the 3705 control panel without causing an error.

INPUT X'60' INSTRUCTION

Input X'60' transfers the contents of the initial selection control register into a CCU general register. The 3705 control program uses this instruction to determine the exact cause of a type 1 CA initial selection level 3 interrupt.

An Output X'60' resets the initial selection control register and the L3 interrupt request resulting from the initial selection.



Bit	Logic Page	Function
0.0	RC402	Input Initial Selection State*
0.1	RC205	Input Initial Interface Disconnect
0.2	RC205	Input Initial Selective Reset
0.3	RC402	Input Initial Bus Out Check
0.4		0
0.5	RC402	Input Stack Initial
0.6	RC505	NSC Status Cleared
0.7	RC205	Input System Reset

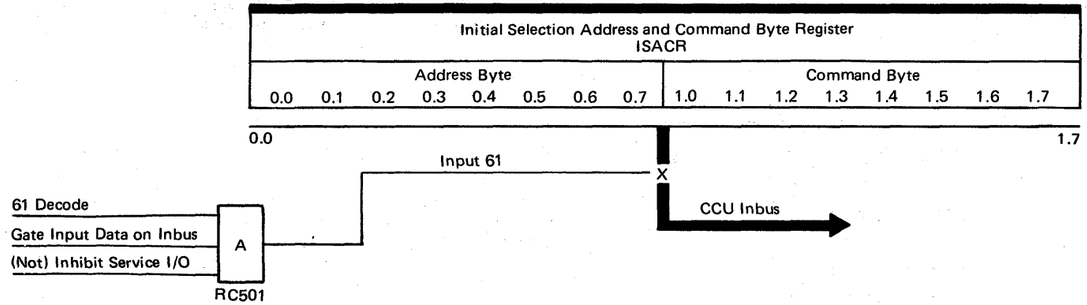
*Normal Initial Selective

INPUT X'61' INSTRUCTION

Input X'61' transfers the contents of the initial selection address and command byte register into a CCU general register. During an initial selection sequence, a type 1 CA initial selection level 3 interrupt is requested, and the 3705 control program must investigate the subchannel address and command causing the interrupt. Byte 0 is the address to which the command in byte 1 was issued.

The 3705 control program must store the address and command because the host CPU can send the CA a new command before the 3705 control program has completed the previous one when in ESC mode. The 3705 control program must also control the CA action for each command.

An Output X'61' instruction has no effect on the channel adapter.



OUTPUT X'62' INSTRUCTION

This instruction initiates inbound and outbound data transfers and status presentations. The 3705 control program uses this instruction to control CA action and to specify the number of bytes of data to transfer across the channel interface on a channel data transfer.

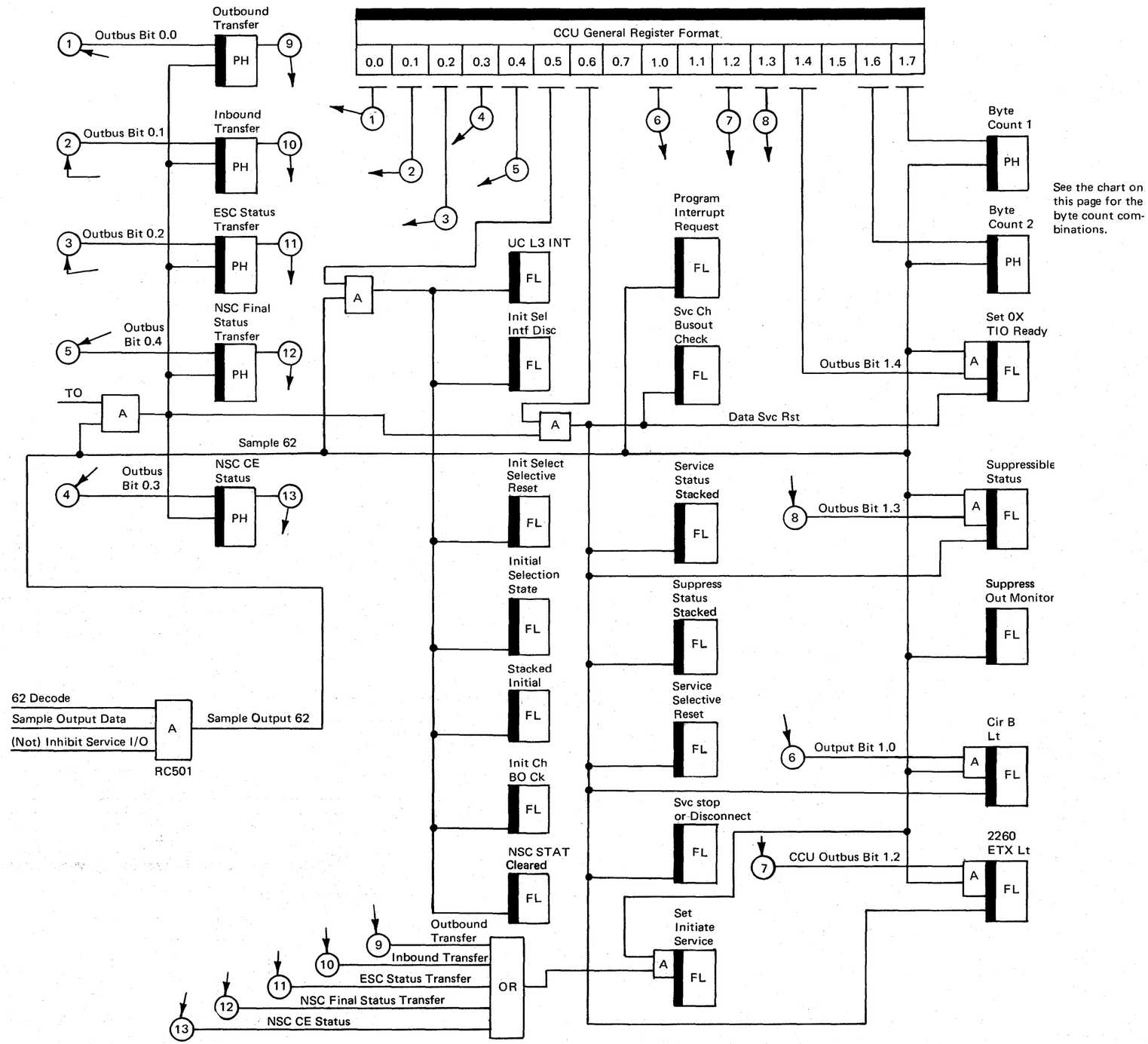
Byte Count	Bits		
	1.5	1.6	1.7
1	0	0	1
2	0	1	0
3	0	1	1
4	X	0	0

X This bit may be on or off for a byte count of four.

Summary of Output X'62' bit definitions and ALD locations

Bit	Card Location	ALD Page	Function
0.0*	Y4L2	RC403	1 = set; 0 = rst outbound transfer
0.1*	Y4L2	RC403	1 = set; 0 = rst inbound transfer
0.2*	Y4L2	RC403	1 = set; 0 = rst ESC status transfer
0.3*	Y4L2	RC403	1 = set; 0 = rst NSC channel end status
0.4*	Y4L2	RC403	1 = set; 0 = rst NSC final status transfer
0.5	Y4K2	RC503	Reset NSC status cleared
	Y4L2	RC402	Reset initial channel bus out check
	Y4L2	RC402	Reset stacked initial
	Y4L2	RC402	Reset initial selection state
	Y4L2	RC402	Reset Unit Check L3 interrupt
	Y4N2	RC205	Reset initial selection interface disconnect
	Y4N2	RC205	Reset initial selection selective reset
0.6	Y4K2	RC504	Reset monitor for 2260 ETX
	Y4K2	RC504	Reset monitor for circle B
	Y4L2	RC406	Reset 0X TIO ready
	Y4L2	RC405	Reset service channel bus-out check
	Y4L2	RC405	Reset service status stack
	Y4N2	RC204	Reset suppressible status
	Y4N2	RC205	Reset service selective reset
	Y4N2	RC205	Reset svc stop or disconnect
	Y4N2	RC204	Reset suppress status stack
0.7	– –	– –	This bit ignored
1.0	Y4K2	RC504	Set monitor for circle B
1.1	– –	– –	This bit ignored
1.2	Y4K2	RC504	Set Monitor for 2260 ETX
1.3	Y4N2	RC204	Set suppressible status
1.4	Y4L2	RC406	Set 0X TIO ready
1.5	Y4K2	RC504	This bit ignored
1.6	Y4L2	RC404	Byte count 2
1.7	Y4L2	RC404	Byte count 1

* Any of these bits with 'Sample 62' set Initiate Service, Y4L2, RC404

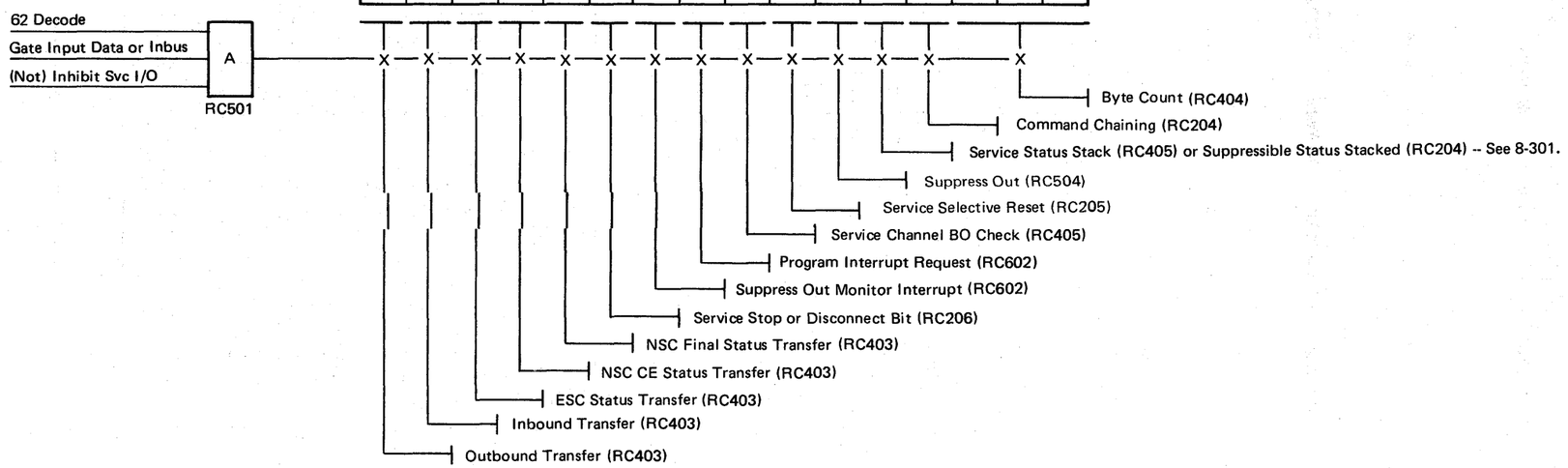


INPUT X'62' INSTRUCTION

This instruction transfers the contents of the data/status control register into a CCU general register. The 3705 control program uses this instruction to determine the exact cause of a type 1 CA data/status level 3 interrupt.

Count transferred to the CCU

Count	Bits		
	1.5	1.6	1.7
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0



OUTPUT AND INPUT X'63' INSTRUCTIONS

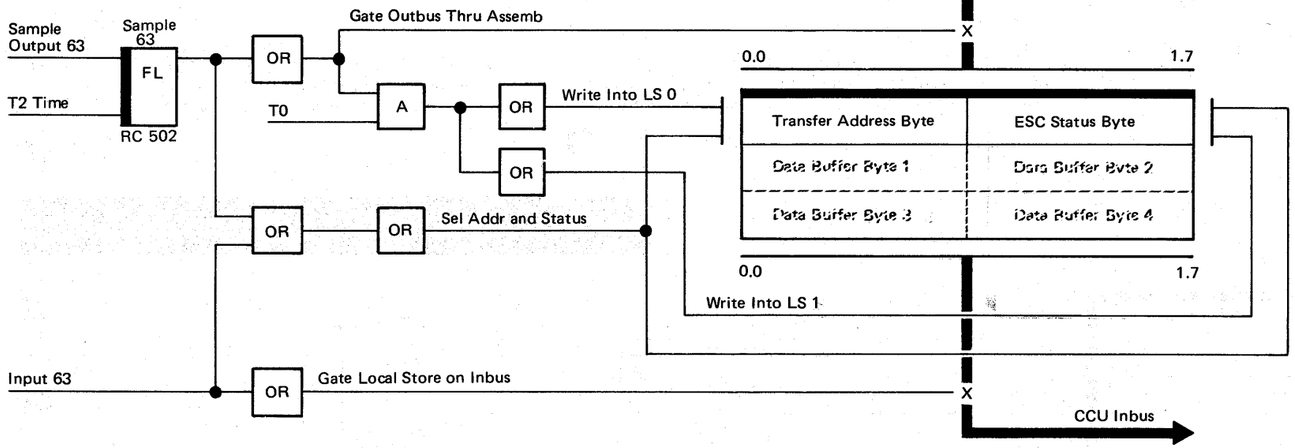
The 3705 control program uses the Output X'63' instruction to load the subchannel address (byte 0) and ESC status byte (byte 1) into the local store buffer. The CA identifies itself to the channel by gating byte 0 onto the channel bus-in, during the data transfer and gates byte 1 onto the channel bus-in to transfer the ESC status to the host CPU. (NSC address and status take a different path, see page 8-170.)

The 3705 control program must ensure that the correct address and status bytes are stored in the register. Otherwise, incorrect channel operation occurs.

With the Input X'63' instruction, the 3705 control program can determine the last subchannel address provided to the host CPU. The level 3 interrupt request latch should be set for this instruction to execute.

CCU Outbus Bit Definitions

Bits	Definition
0.0-0.7	Subchannel address
1.0	Attention
1.1	Status modifier (SM)
1.2	Control unit end (CUE)
1.3	Busy
1.4	Channel end (CE)
1.5	Device end (DE)
1.6	Unit check (UC)
1.7	Unit exception (UE)



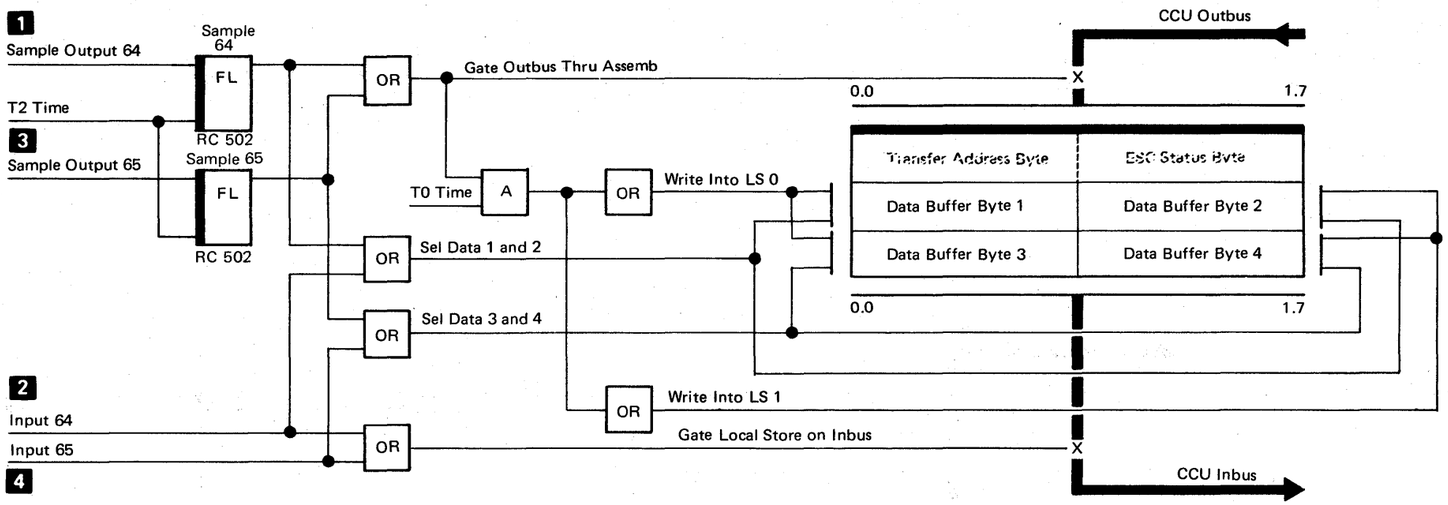
OUTPUT AND INPUT X'64' INSTRUCTION

1

Output X'64' instruction loads data buffer byte 1 and data buffer byte 2 with the first two data bytes to be transferred across the channel to the CPU. These two data bytes are transferred to the CPU one byte at a time during an outbound data transfer.

2

Input X'64' transfers into a CCU general register the two data bytes that were received from the channel and stored in data buffer byte 1 and data buffer byte 2.



OUTPUT AND INPUT X'65' INSTRUCTION

3

Output X'65' instruction loads data buffer byte 3 and data buffer byte 4 with the second two bytes to be transferred across the channel to the CPU. These two data bytes are transferred to the CPU one byte at a time during an outbound data transfer.

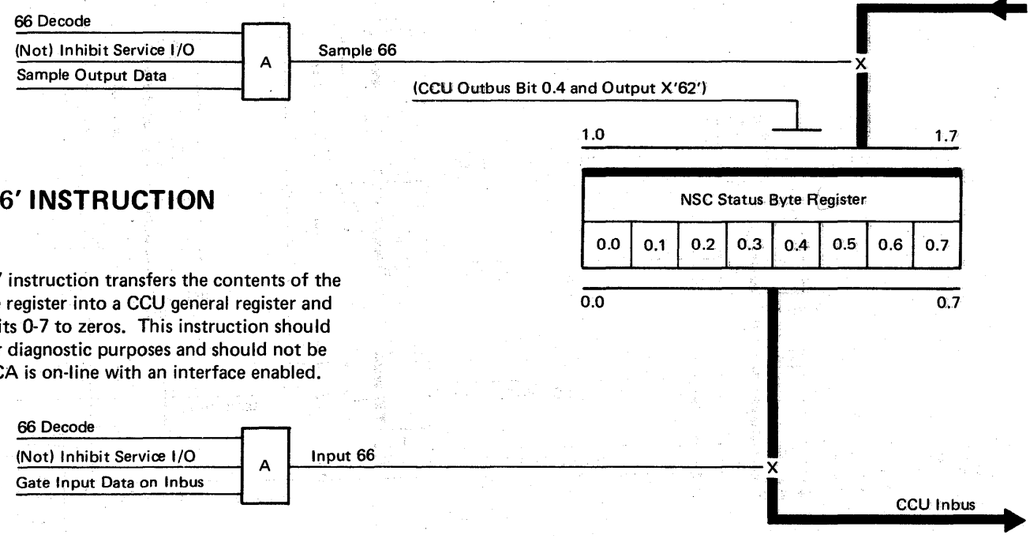
4

Input X'65' transfers into a CCU general register the two data bytes that were received from the channel and stored in data buffer byte 3 and data buffer byte 4.

OUTPUT X'66' INSTRUCTION

The Output X'66' instruction loads the final status byte to be presented to the channel into the NSC Status Byte Register.

LOGIC REFERENCE RC 601. RC 308



INPUT X'66' INSTRUCTION

The Input X'66' instruction transfers the contents of the NSC status byte register into a CCU general register and forces byte 1, bits 0-7 to zeros. This instruction should be used only for diagnostic purposes and should not be used when the CA is on-line with an interface enabled.

NSC STATUS BYTE REGISTER BIT DEFINITIONS

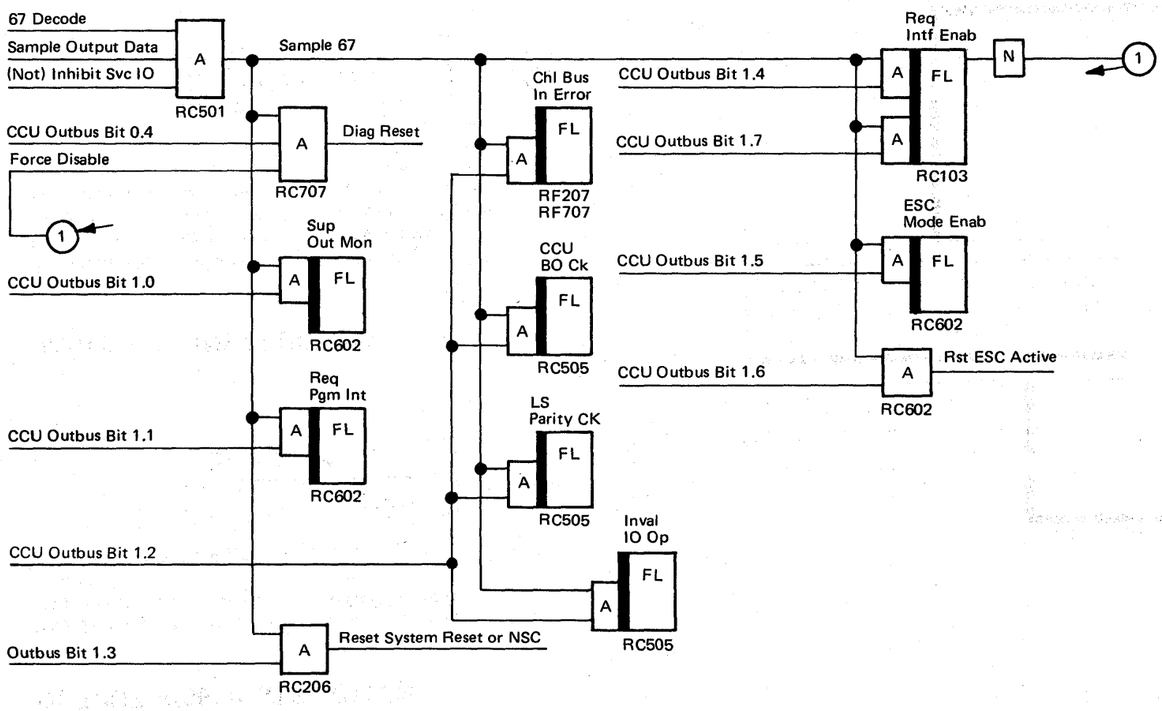
Bit 0.0 — Attention
Bit 0.1 — Status Modifier
Bit 0.2 — 0
Bit 0.3 — 0
Bit 0.4 — Channel End (CE)
Bit 0.5 — Device End (DE)
Bit 0.6 — Unit Check (UC)
Bit 0.7 — Unit Exception (UE)

OUTPUT AND INPUT X'67' INSTRUCTION

The Output X'67' instruction sets or resets the various control latches. The 3705 control program must execute an Output X'67' instruction to enable the CA interface before the CA can transfer data to or from the channel.

Summary of Outbus bits during Output X'67'

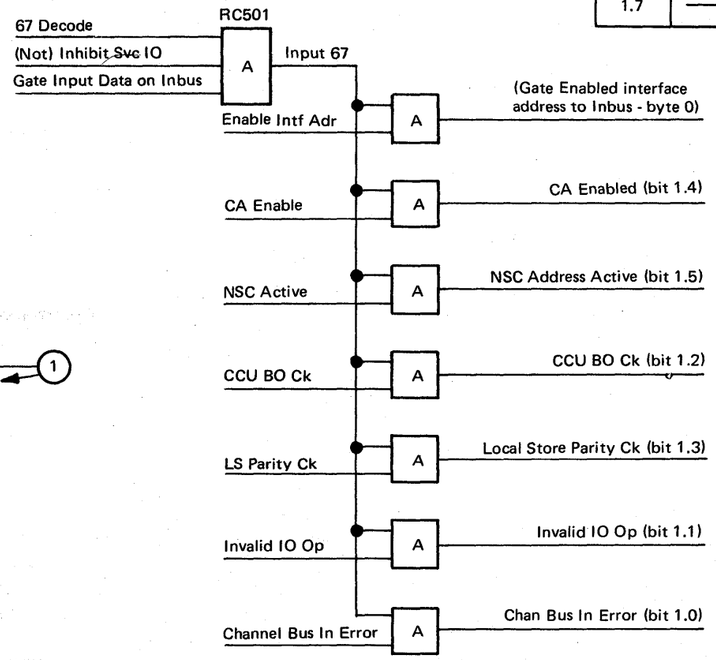
Bit	Card Loc.	ALD Page	Function
0.4	Y4Q2	RC707	Diagnostic reset
1.0	Y4T2	RC602	Set suppress out monitor
1.1	Y4T2	RC602	Set request program interrupt
1.2	Y4K2	RC507 RC507 RC507 RC707 RF207	Reset invalid I/O Op Reset local store parity check Reset CCU outbus check Reset channel bus in error (interface A) Reset channel bus in error (interface B)
1.3	Y4N2	RC206	Reset system reset or NSC
1.4	Y4P2	RC103	Request interface enable
1.5	Y4T2	RC602	Set ESC mode enable
1.6	Y4T2	RC602	Reset ESC active
1.7	Y4P2	RC103	Reset interface enable



The Input X'67' transfers the error condition register and the hardware address of the NSC channel interface address to the CCU.

Summary of Inbus bits during Input X'67':

Bit	Card Loc.	Logic Page	Function
0.0-0.7	Y4P2	RC104	NSC hardware address intf A
0.0-0.7	Y4P2	RC107	NSC hardware address intf B
1.0	Y4Q2	RC707	Chan bus in error
1.1	Y4K2	RC507	Invalid I/O Op
1.2	Y4K2	RC507	CCU outbus check
1.3	Y4K2	RC507	Local store parity check
1.4	Y4K2	RC504	CA enabled
1.5	Y4K2	RC504	NSC address active
1.6	——	——	0
1.7	——	——	0

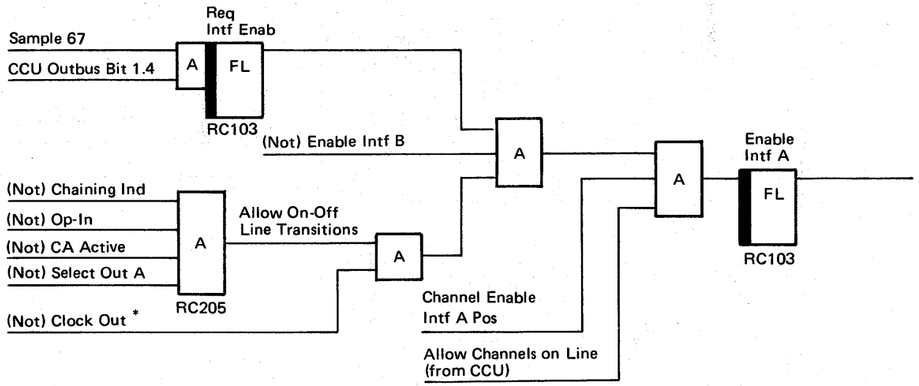


CHANNEL ADAPTER INITIALIZATION (IPL)

• Channel adapter initialization involves enabling the CA to a channel interface and requesting a Write IPL command from the host CPU.

The type 1 CA is not affected by the reset performed in IPL phase 1 unless the IPL sequence is started by a power on sequence. Therefore, the ROS bootstrap program must handle the following situations:

1. Channel interface disabled.
2. Channel interface enabled without a channel command in progress.
3. Channel interface enabled with a channel command in progress.



* This signal not used on the type 4 CA.

The CA can be enabled to one of two channel interfaces. The second channel interface is optional and allows the CA to be attached to two different CPUs. The CA can also be attached to the same channel through the interfaces. However, only one interface can be enabled at a time.

The channel interface must be enabled for the channel and CA to communicate. The manual procedure to enable a channel interface is described on page 1-050. The bootstrap program must execute an Output X'67' instruction with bit 1.4 on in the general register. This bit allows the channel interface to be enabled. The ROS bootstrap program checks for the interface to become enabled with an Input X'67' instruction. When the Input X'67' transfers bit 1.4 to the CCU general register, the ROS bootstrap program requests a CA data/status level 3 interrupt by executing an Output X'67' instruction with bit 1.1 on in the CCU general register.

If no channel command is in progress, the program signals the CA to send an asynchronous status of Device End (DE) Unit Check (UC) to the channel. The bootstrap program must execute the following instructions to present the asynchronous attention.

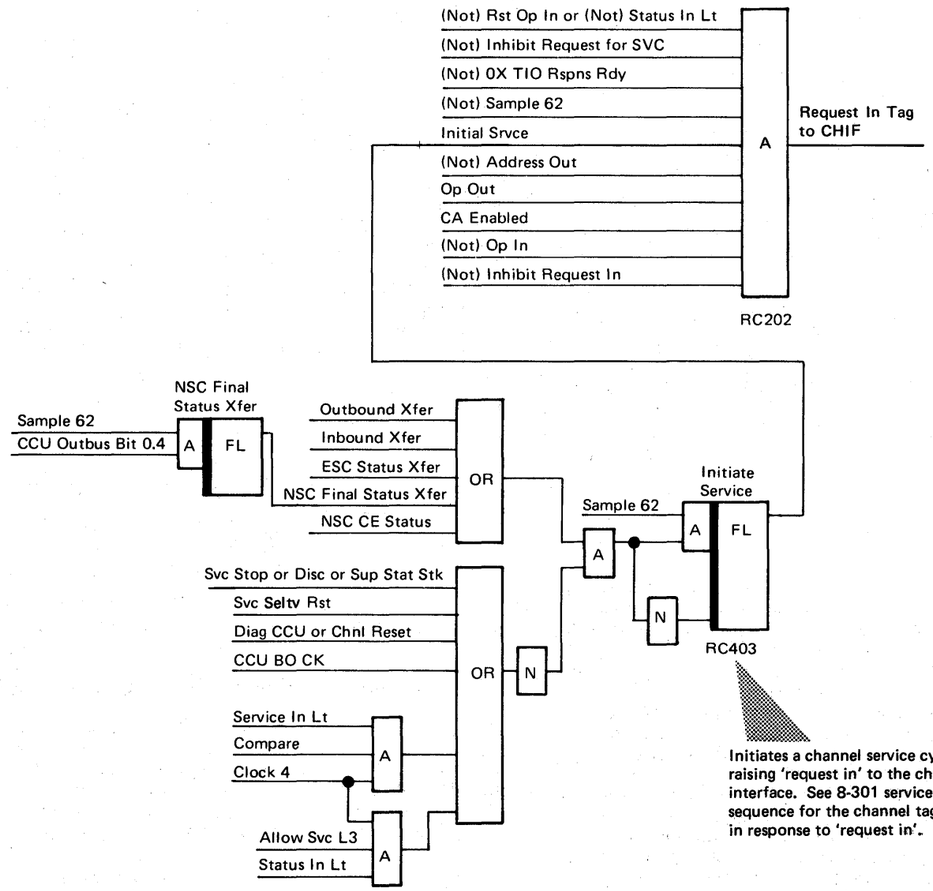
Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Output X'67'	0000 0000	0000 1000	Enable channel interface
Input X'67'	0000 0000	0000 1000	Interface enabled, the ROS bootstrap program loops on this instruction until the interface is enabled.
Output X'67'	0000 0000	0100 0000	Program requests a level 3 interrupt. The ROS bootstrap program executes in level 1 which makes this routine different from the control program routine.

The ROS bootstrap program senses the requested interrupt and executes the following sequence of instructions.

Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Input X'77'	0000 0000	0001 0000	Type 1 CA data/status level 3 interrupt
Input X'62'	0000 0001	0000 0000	0.7 = Program requested level 3 interrupt
Output X'63'	Address	0000 0000	Byte 0 = NSC address Byte 1 = all zeros
Output X'66'	0000 0000	0000 0110	1.5 = Device End 1.6 = Unit Check Note: If a channel command is pending when the IPL sequence is started, the ROS bootstrap program adds Channel End (CE) to the status byte to signal the host CPU to end the pending command.
Output X'62'	0000 1000	0000 0000	0.4 = NSC Final Status transfer

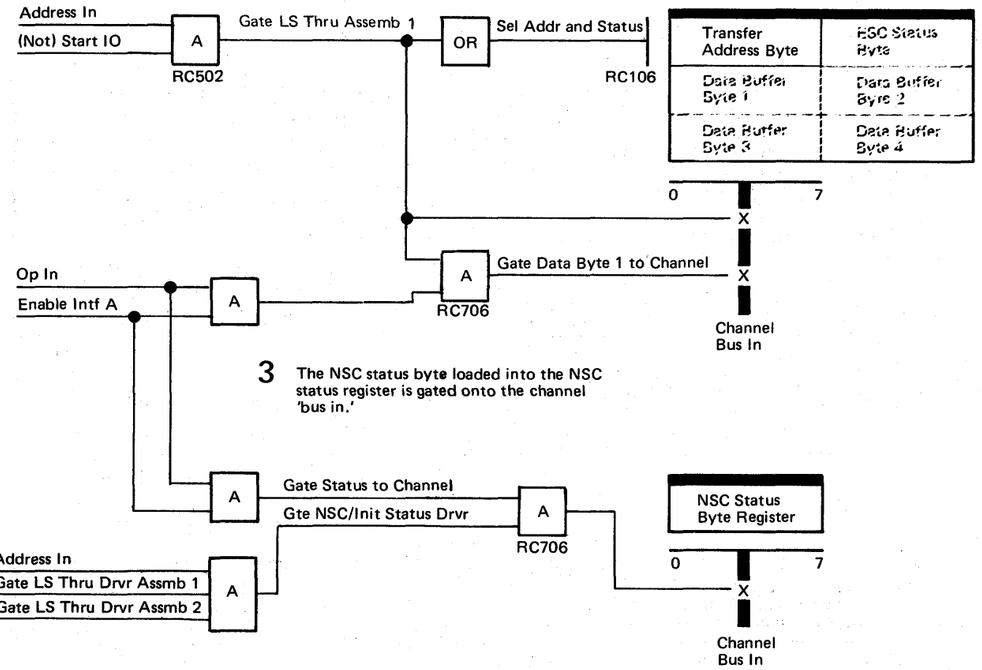
CHANNEL ADAPTER INITIALIZATION (PART 2)

1 The Output X'62' sets bit 0.4 in the data/status control register and causes the CA to attach to the channel and initiate a channel transfer.



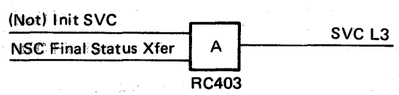
Initiates a channel service cycle by raising 'request in' to the channel interface. See 8-301 service status sequence for the channel tag sequence in response to 'request in'.

2 The NSC address loaded into the transfer address byte buffer is gated onto the channel 'bus in' to identify the device requesting channel service.



3 The NSC status byte loaded into the NSC status register is gated onto the channel 'bus in.'

4 The CA requests a data/status level 3 interrupt to signal the ROS bootstrap program that the status transfer is complete.



EXPECTED CPU RESPONSE TO ASYNCHRONOUS STATUS

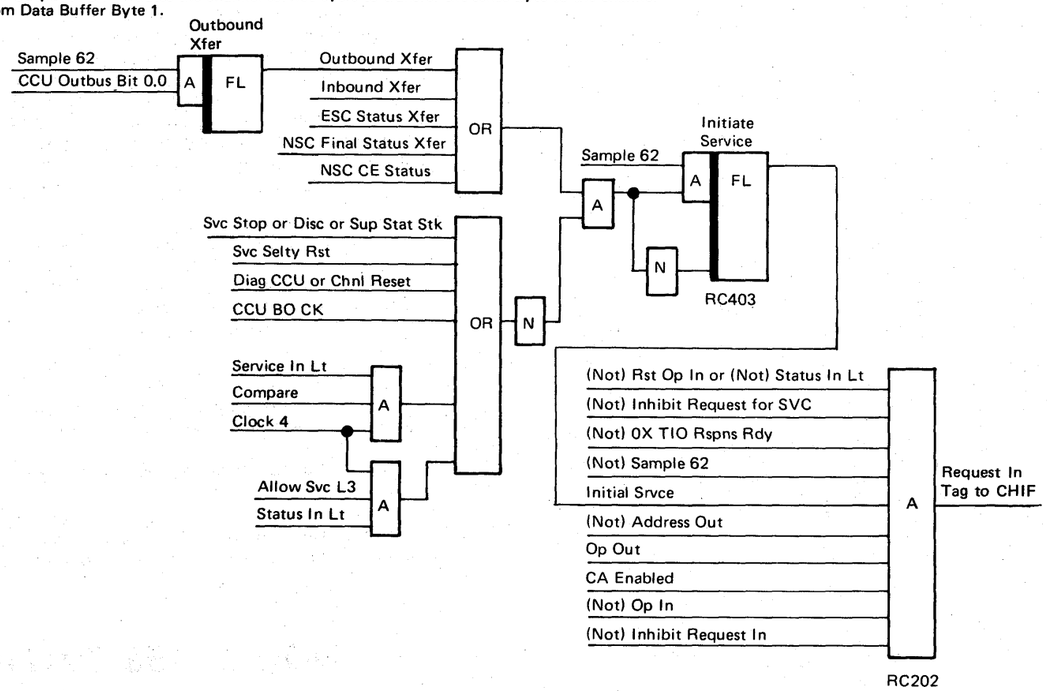
The ROS bootstrap program expects to receive a Channel Sense command in response to the asynchronous DE, UC Status so the program loops waiting for an initial selection level 3 interrupt from the CA.

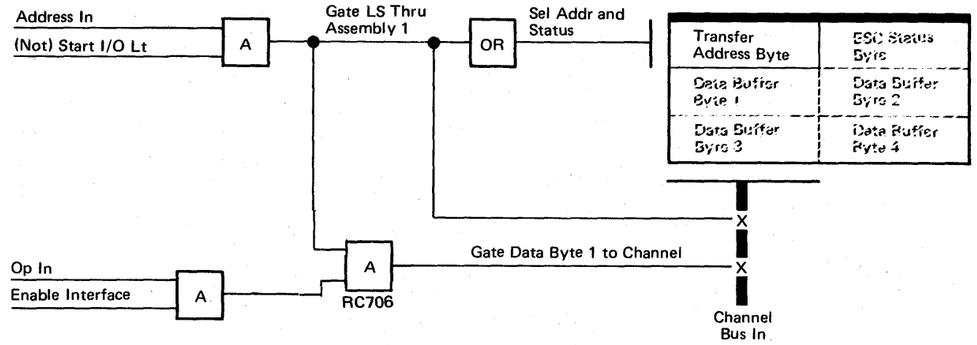
Because the ROS bootstrap program can only handle a Sense or Write IPL command, it rejects others by presenting final status of CE, DE, and UC.

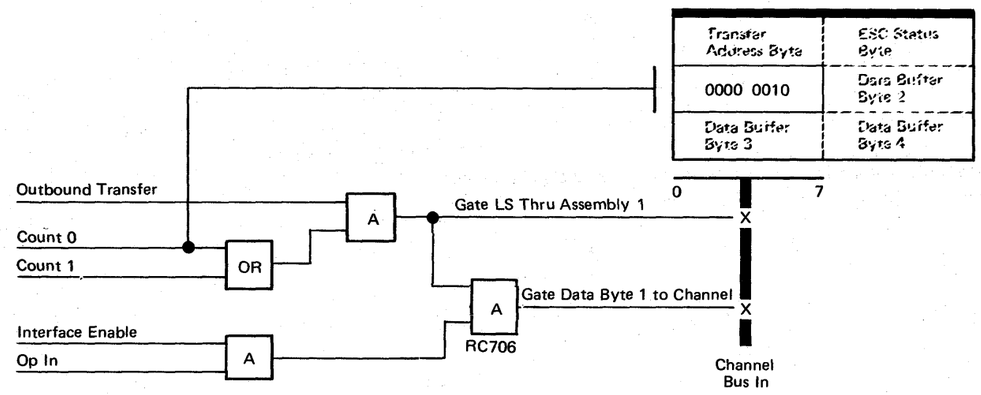
However, any command received by the CA starts an initial selection sequence. When the channel Sense command starts the initial selection sequence, and requests a type 1 CA initial selection level 3 interrupt, the ROS bootstrap program responds with the following instructions:

Instruction	General Register Bits Byte 0	Byte 1	Indication or function
Input X'77'	0000 0000	0000 1000	Type 1 CA Initial Selection L3 Interrupt
Input X'60'	1000 0000	0000 0000	Normal initial selection
Input X'61'	Address	Command	Byte 0 = address of NSC Byte 1 = command
Output X'63'	Address	0000 0000	Byte 0 = NSC address
Output X'64'	0000 0010	0000 0000	0.6 = Not initialized (sense byte)
Output X'62'	1000 0100	0000 0001	0.0 = Outbound transfer sequence 0.5 = Reset initial selection 1.7 = byte count of one

The Output X'62' initiates the channel service cycle to transfer the sense byte to the channel from Data Buffer Byte 1.







SENSE BIT DEFINITIONS

Bit 0 — Command Reject. This bit indicated that the channel command presented to the channel adapter is not a valid command for a particular subchannel address or not valid for the NSC address.

Bit 1 — Intervention Required. This bit indicated that programming errors were detected by either the CA, the CCU, or the 3705 control program. CA hardware sets this bit when the CA is executing a channel Read, Write, or Write Break command.

Bit 2 — Bus Out Check. This bit indicated a parity check was detected on the I/O channel bus out during the initial selection command byte transfer or during host processor to 3705 data transfer.

Note: Refer to the Program Logic Manual for the sense bit definitions because they are program dependent.

Bit 3 — Equipment Check. This bit indicates that an internal hardware check or a parity check is detected during a data transfer between the CCU and the channel adapter.

Bit 4 — Data check.

Bit 5 — Not used.

Bit 6 — This bit indicated that the CCU is not initialized. The host CPU is expected to respond to this bit with a Write IPL command.

Bit 7 — Abort. This bit indicated that the 3705 control program has terminated its channel operation in an abnormal manner.

SENSE COMMAND ENDING STATUS

Ending status can be presented to the channel in one of three combinations:

1. CE, DE presented together - normal operation.
2. Split CE, DE, (that is, not together).
3. CE, DE, and UC, - occurs when interface disconnect is received during a Sense command.

INITIAL SELECTION

- The CA decodes its address from the channel 'bus out' and stores it in the initial selection address and command byte register.
- The CA decodes the channel command and either:
  1. Executes the command without control program intervention, (No-Op, NSC Test I/O).
  2. Requests an initial selection level 3 interrupt so the 3705 control program can process the command.

  The command byte is stored in the initial selection address and command byte register.
- The CA gates initial status to the channel 'bus in' for each command without control program intervention.

  Each channel command issued to the CA starts an initial selection sequence. Since the 3705 can emulate either an IBM 2701, IBM 2702, or an IBM 2703, or operate in native mode (NSC), some differences occur during several commands.

  In native mode (NSC address), the CA handles No-Op and Test I/O commands without control program intervention. The CA also handles No-Op without control program intervention when the 3705 is operating in emulation mode (ESC address).

  In order for the CA to decode its address or commands, the CA must be enabled with respect to a channel interface as described in Channel Adapter Initialization, 8-140. If the 3705 is to operate in emulation mode (ESC), the 3705 control program must also set ESC operational with an Output X'67' instruction.

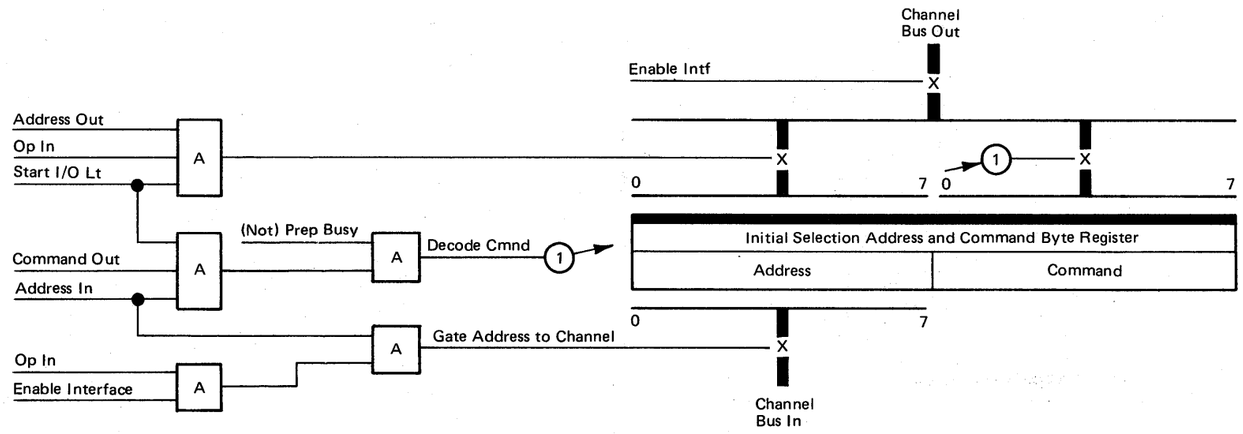
  If the CA raises 'request in' to start a data/status transfer, but the channel responds with 'address out' and 'select out' (initial selection sequence), the initial selection sequence overrides the data/status transfer. The 3705 control program must remember that the data/status in the local store was not transferred to the channel and must present it again. This can only occur during ESC mode.

CA DECODES AND STORES THE ADDRESS

The CA can recognize a range of addresses as described on 8-000. The addresses that are hardware plugged are compared to the address from the channel to determine when the channel is addressing the CA. The NSC address is plugged on card Y4P2 (RC104 for interface A and RC107 and RC106 for interface B). The low ESC address is plugged on card Y4M2 (RC302), and the high ESC address is plugged on card Y4M2 (RC304).

If the address is valid, it is gated into the initial selection address and command byte register. The CA gates the address onto the channel 'bus in' and receives a channel command in response. Channel commands are also maintained in the initial selection address and command byte register. The action taken for each command varies, depending upon the mode (ESC or NSC) and the command. Refer to the discussions of the different commands to determine how they are executed.

LOGIC REFERENCE: RC 306



WRITE IPL COMMAND

- A channel Write IPL command is required to transfer the program load module from the host CPU to 3705 storage.
- The CCU is not initialized until control is passed from the ROS bootstrap program to the program load module.
- The 3705 is controlled by the ROS bootstrap program during the Write IPL command execution.

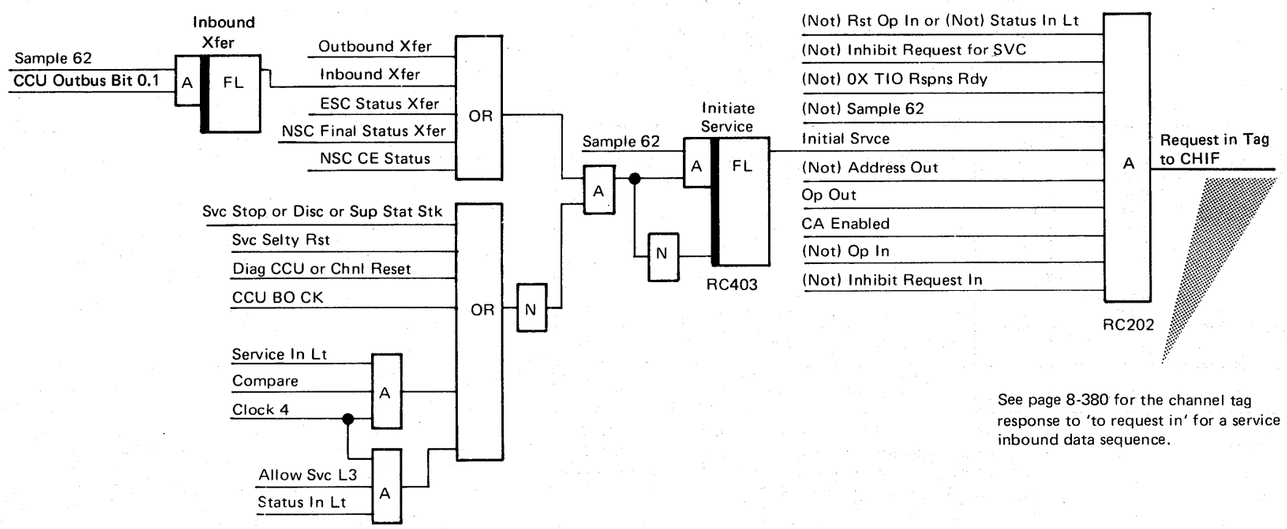
The 3705 ROS bootstrap program expects a Write IPL command in response to the not initialized sense bit. If a command other than Write IPL is decoded by the CA, the ROS bootstrap program signals the CA to end the command by presenting Channel End (CE), Device End (DE), and Unit Check (UC) status to the channel.

When the Write IPL command is decoded by the CA, a Type 1 CA initial selection level 3 interrupt is requested.

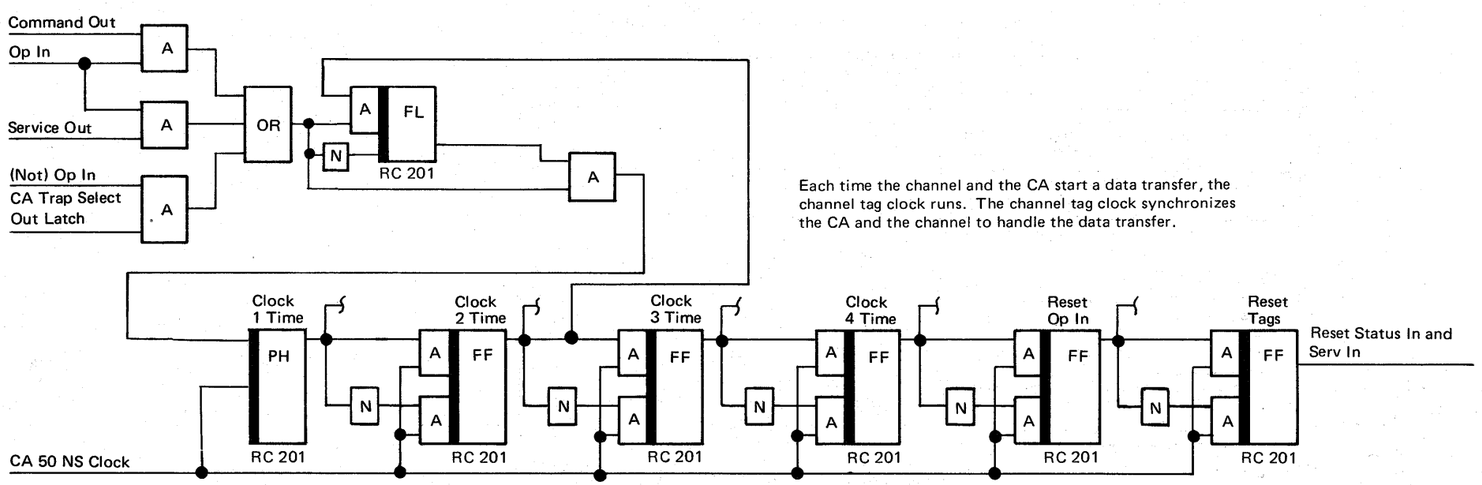
The 3705 control program responds to the interrupt request with the following instructions:

Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Input X'77'	0000 0000	0000 1000	Type 1 CA initial selection level 3 interrupt
Input X'60'	1000 0000	0000 0000	Normal initial selection (see note)
Input X'61'	Address	0000 0101	Byte 0 = address Byte 1 = Write IPL command
Output X'63'	Address	0000 0000	Byte 0 = NSC address Byte 1 = all zeros
Output X'62'	0100 0110	0000 0010	0.1 = Inbound transfer sequence 0.5 = Reset initial selection 0.6 = Reset data service 1.6-1.7 = Number of bytes to transfer. The ROS bootstrap program always requests two data bytes during IPL.

Note: Bit 0.0 is the only bit expected to be on at this time. Other bits may be on at different times and indicate different conditions to the 3705 control program. See Input X'60' instruction 8-070 for descriptions of the other bits in this register.



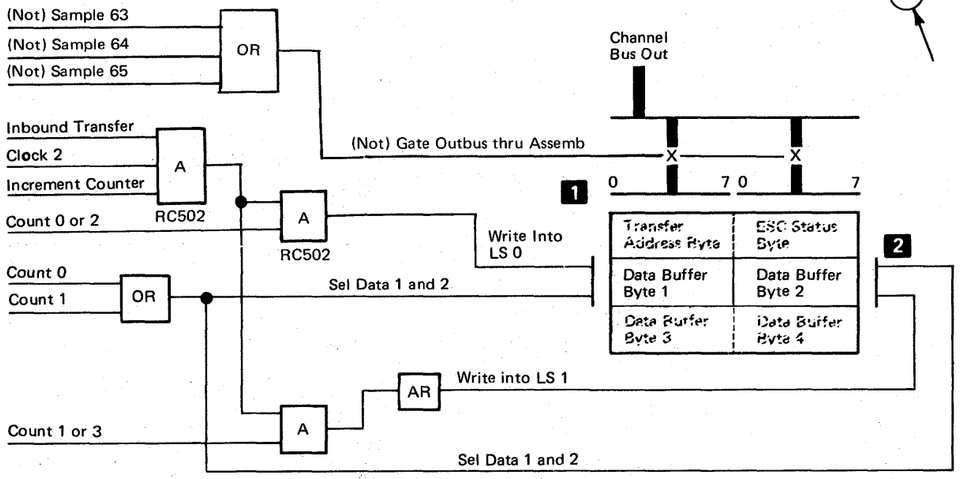
See page 8-380 for the channel tag response to 'to request in' for a service inbound data sequence.



Each time the channel and the CA start a data transfer, the channel tag clock runs. The channel tag clock synchronizes the CA and the channel to handle the data transfer.

WRITE IPL (PART 2)

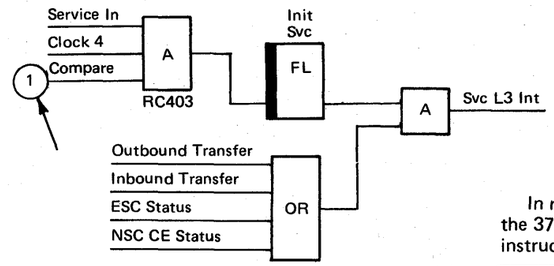
Data transfers across the channel one byte at a time, and each byte is gated into the local store data buffer. The byte count is incremented for each byte transferred.



1 Loads byte 1 into Data Buffer Byte 1

2 Loads byte 2 into Data Buffer Byte 2

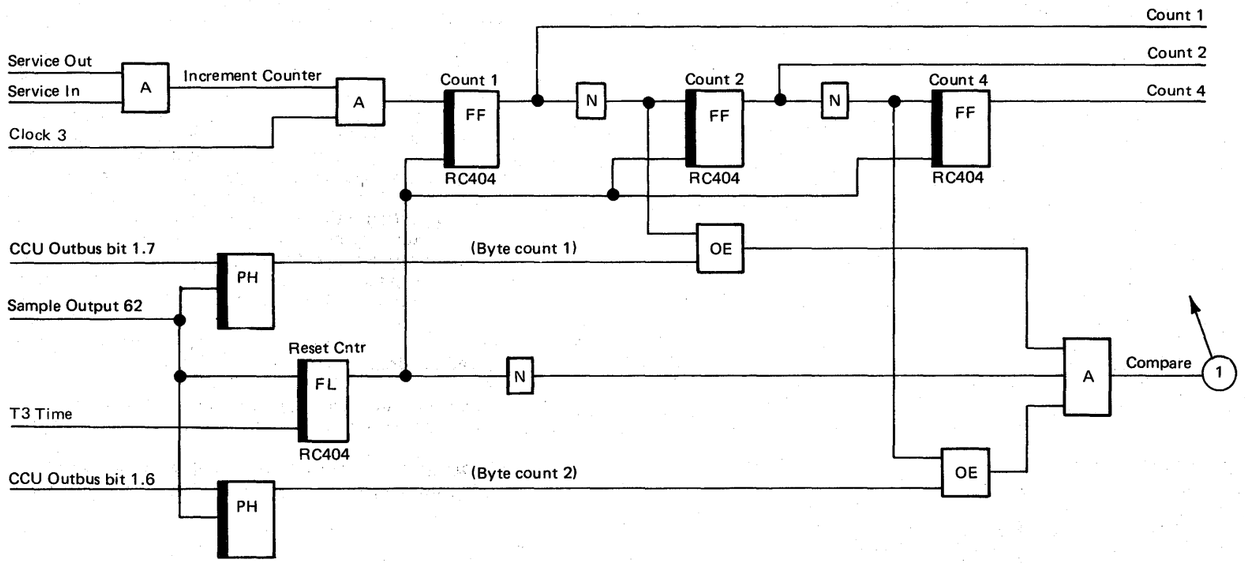
When the number of bytes transferred equals the count specified by the Output X'62' instruction, the CA requests a level 3 data/status interrupt.



In response to the CA data/status level three interrupt, the 3705 control program must execute the following instructions.

Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Input X'77'	0000 0000	0001 0000	Type 1 CA data/status level 3 interrupt.
Input X'62'	0100 0*00	0000 0XXX	0.1 = inbound data transfer *0.5 if on indicates a channel stop or interface disconnect. The control program should end the channel command. 1.5-1.7 = the number of bytes transferred.
Input X'63'	Address	0000 0000	Byte 0 = Subchannel address Byte 1 = all zeros
Input X'64'	Data byte	Data byte	Byte 0 = data byte 1 Byte 1 = data byte 2
Output X'62'	0100 0010	0000 0010	0.1 = inbound data transfer 0.6 = reset data/status condition 1.6 = request 2 bytes of data

Note: This bit pattern is valid only if the CA is to continue the data transfer. The ROS bootstrap program expects to transfer up to 1022 data bytes before ending the channel command and requests 2 bytes of data on each transfer. This sequence is repeated until the transfer is completed. If the transfer is to end, see 8-280



If bit 0.5 is on during the input X '62', the channel has signaled the end of the data transfer by initiating a channel stop sequence. The 3705 control program should send the final status to the channel with the following instructions.

Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Output X'63'	Address	0000 0000	byte 0 = subchannel address See note 1
Output X'66'	0000 0000	0000 1100	1.0 = Attention 1.1 = Status Modifier 1.2 = 0 1.3 = 0 1.4 = Channel End See note 2 1.5 = Device End See note 2 1.6 = Unit Check 1.7 = Unit Exception
Output X'62'	0000 1010	0000 0000	0.4 = Set NSC Final Status Transfer. 0.6 = Reset data/status L3 interrupt

Notes:

1. The 3705 control program does not necessarily have to execute this instruction since the NSC address in the transfer address byte register should not have changed during the data transfer.
2. This is the normal final status that should be presented. However, the 3705 control program can present other bits to designate different conditions if needed.

CA DECODES A CHANNEL COMMAND

The CA accepts any command byte if it is in correct parity on the channel 'Bus Out'. The command is handled without control program intervention if (1) the 3705 is in native mode, and the command is a No-Op or Test I/O, or (2) the 3705 is in emulation mode, and the command is a No-Op.

Otherwise, the command is stored in the initial selection address and command byte register, and an initial selection level 3 interrupt is requested so the 3705 control program can handle the command as required.

Note: Depending upon whether the 3705 is in native mode (NSC) or emulation mode (ESC), different action may be taken for a channel command. Where there is a difference, NSC information is in the left hand column and ESC information is in the right hand column.

NSC

NO-OP COMMAND

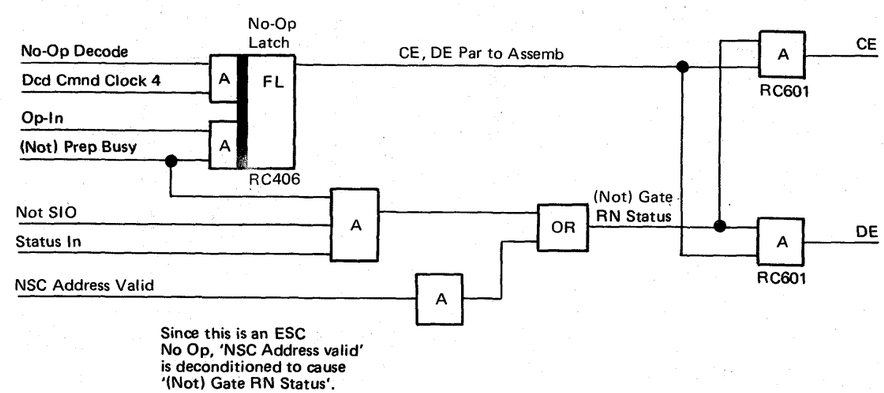
If the CA is free of commands when the No-Op is decoded, CE, DE status is presented immediately to the channel 'Bus In'. See diagram for ESC No-Op.

If any pending status is available, or the CA is not free of commands, the CA presents that status along with Busy to the channel 'Bus In'.

ESC

NO-OP COMMAND

The CA immediately presents CE, DE status to the channel.



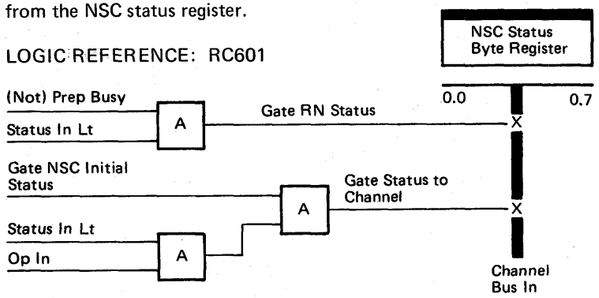
NSC

TEST I/O

- Presents initial status of X'00', or presents any pending status with the initial status.

If NSC status is pending, Test I/O initial status is gated from the NSC status register.

LOGIC REFERENCE: RC601



If NSC status is not pending, Test I/O initial status is gated from the initial selection status register.

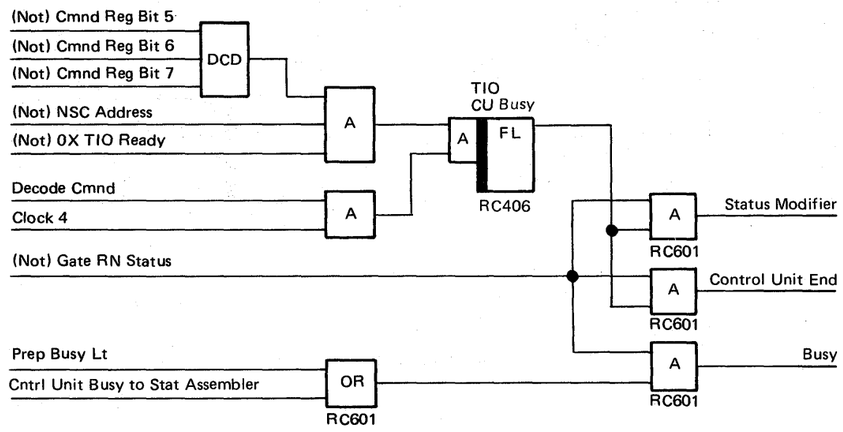
LOGIC REFERENCE: RC406

ESC

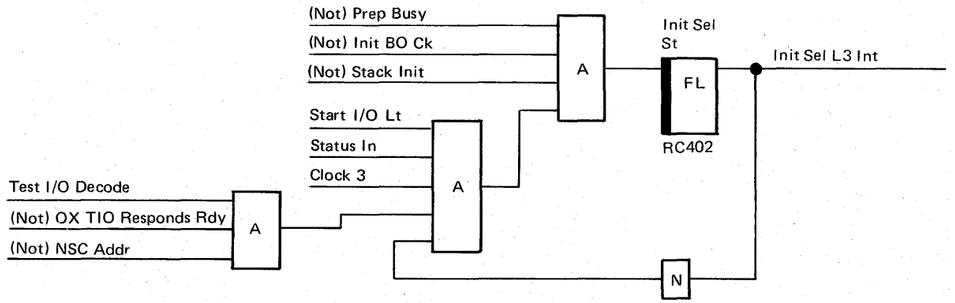
TEST I/O

- Presents initial status of
  - Status Modifier
  - Control Unit End
  - Busy
- Requests a level 3 interrupt so that the 3705 control program can present the status of the subchannel address to which the command was issued.

The CA presents the initial status for this command and requests an initial selection level 3 interrupt so that the 3705 control program can load the status byte for the subchannel address into the ESC status byte register in local store.



TEST I/O (PART 2)



The 3705 control program must determine the status to return to the channel after determining which subchannel address the Test I/O was issued to. The 3705 control program must execute the following instructions in response to the level 3 interrupt.

Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Input X'77'	0000 0000	0000 1000	Type 1 CA initial selection level 3 interrupt.
Input X'60'	1000 0000	0000 0000	Normal Initial Selection
Input X'61'	address	0000 0000	byte 0 = address requesting service byte 1 = Test I/O decode
Output X'63'	address	status	byte 0 = subchannel address byte 1 = status of subchannel
Output X'62'	0010 0110	0000 1000	0.2 = ESC final status transfer 0.5 = Reset Initial Selection 0.6 = Reset data/status control 1.4 = ESC Test I/O Status Ready

The host CPU program must loop on the Test I/O command. When the next initial selection sequence occurs, the hardware compares the address presented to the adapter on the channel 'Bus Out' to the address maintained in the initial selection address and command byte register.

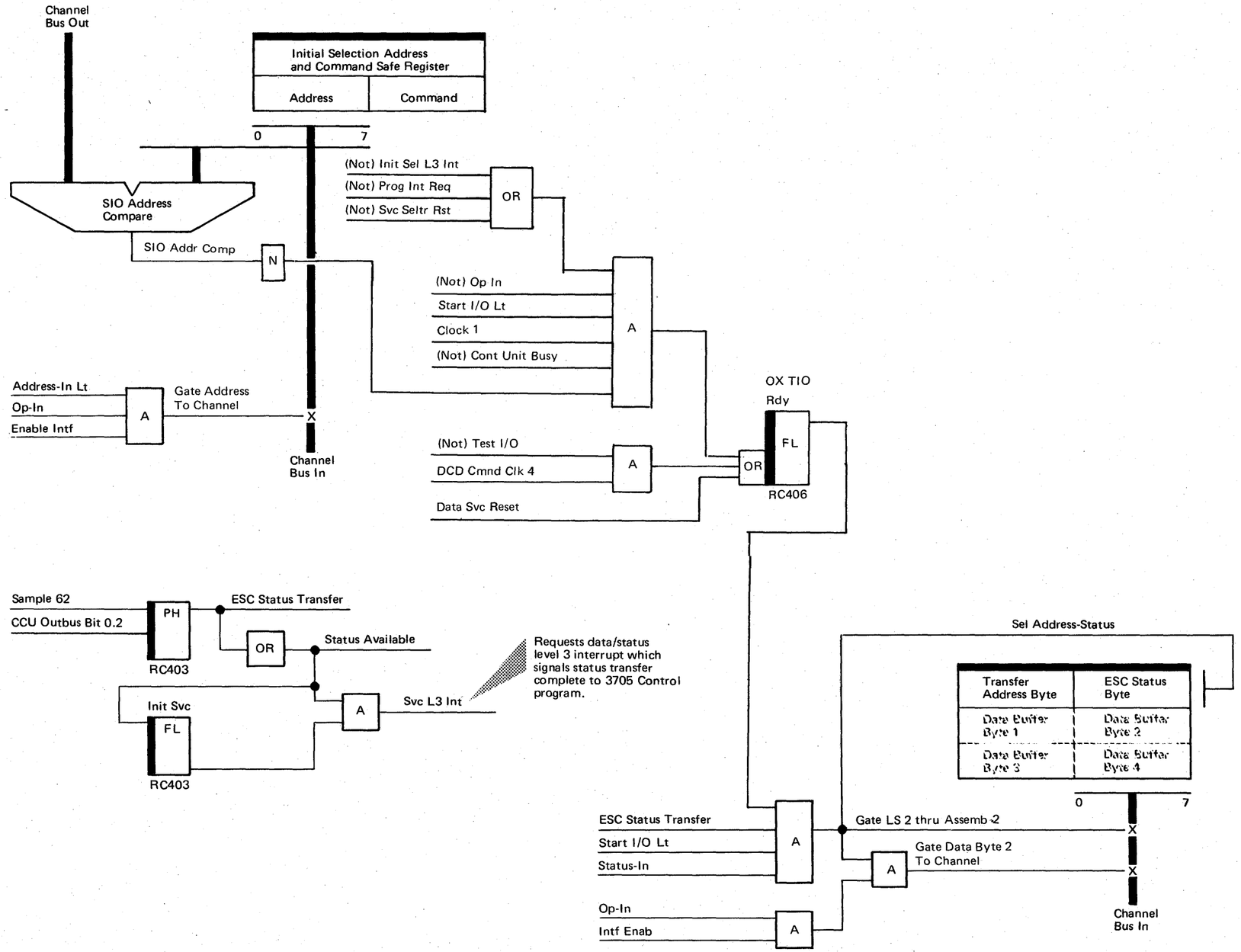
If these addresses compare and the subsequent command is a Test I/O command, the CA presents the status byte loaded by an Output X'63' instruction and then requests a data/status level 3 interrupt so that the 3705 control program can determine that the status was presented.

If the addresses do not compare during the initial selection sequence or if the command is not a Test I/O command, the CA resets out of the ESC Test I/O mode and handles this sequence as a normal initial selection. If this occurs, the 3705 control program does not sense a data/status level 3 interrupt request resulting from the completion of the Test I/O.

Between the time the Test I/O is first issued, and the time the 3705 control program executes the Output X'62' to transfer the status, the CA responds with a short control unit busy status (Status Modifier, Control Unit End, and Busy) to any initial selection sequence from the host CPU.

NSC ESC

TEST I/O (PART 3)

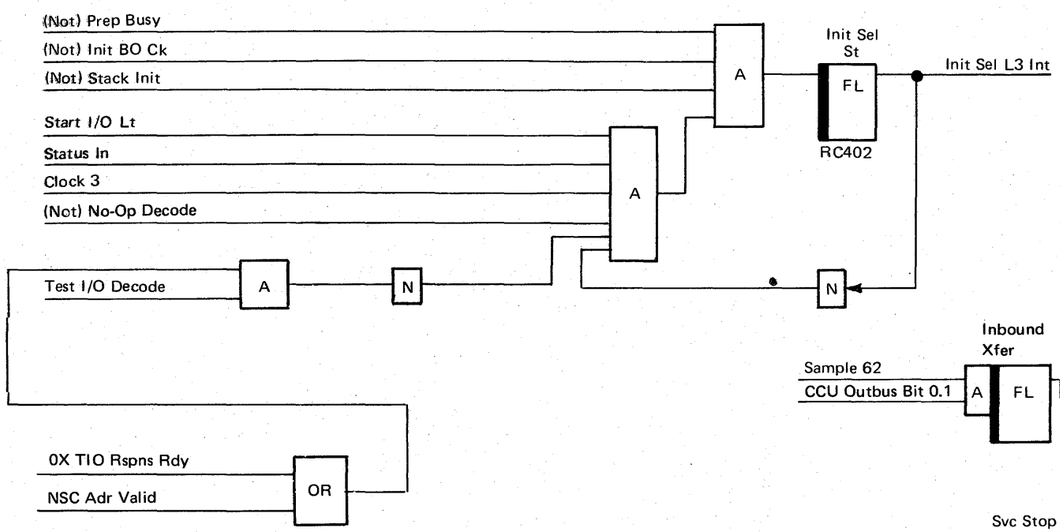


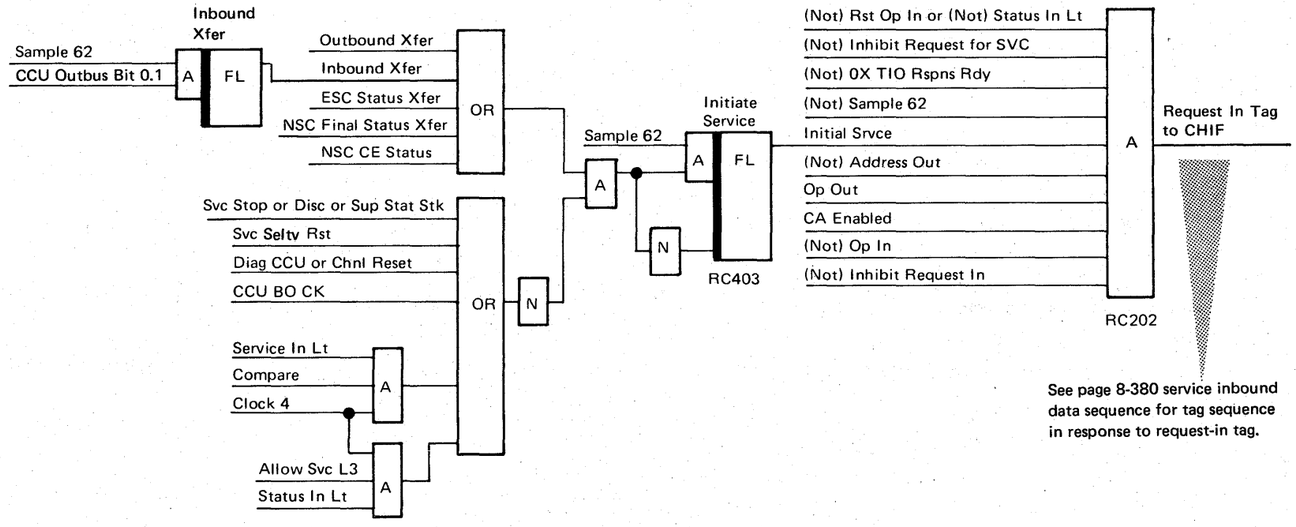
INBOUND DATA TRANSFERS

Inbound data transfers result from commands that require the passing of data from the host CPU to 3705 storage.

When the commands are decoded, they request an initial selection level 3 interrupt so that the 3705 control program can determine what action to take to service the command. The commands start an initial selection sequence as shown on 8-170.

CA REQUESTS AN INITIAL SELECTION LEVEL 3 INTERRUPT





See page 8-380 service inbound data sequence for tag sequence in response to request-in tag.

CONTROL PROGRAM RESPONDS TO THE INTERRUPT

The 3705 control program responds to the initial selection level 3 interrupt with the following sequence of instructions.

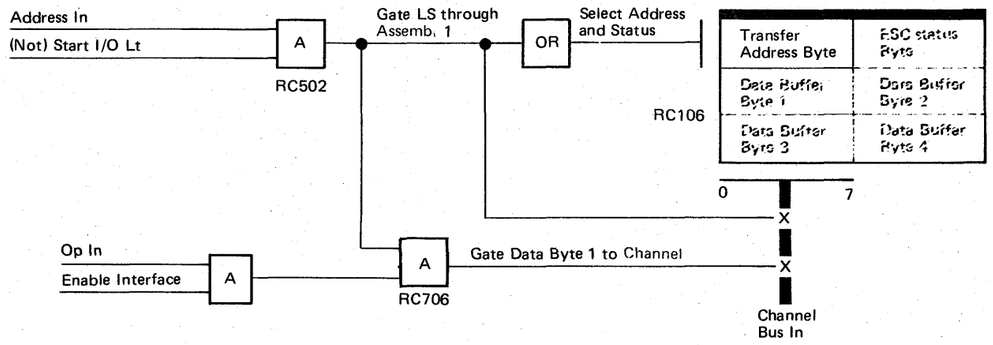
Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Input X'77'	0000 0000	0000 1000	Type 1 CA initial selection level 3 interrupt
Input X'60'	1000 0000	0000 0000	Normal initial selection*
Input X'61'	Address	Command	Byte 0 = subchannel address Byte 1 = command
Output X'63'	Address	0000 0000	Byte 0 = address Byte 1 = all zeros
Output X'62'	0100 0110	0000 0000	0.1 = inbound data transfer 0.5 = reset initial selection 0.6 = reset data/status control 1.6-1.7 = 0 to request 4 bytes transferred in

* If other bits are on during this input, the 3705 control program must take appropriate action to service the condition indicated by the bit.

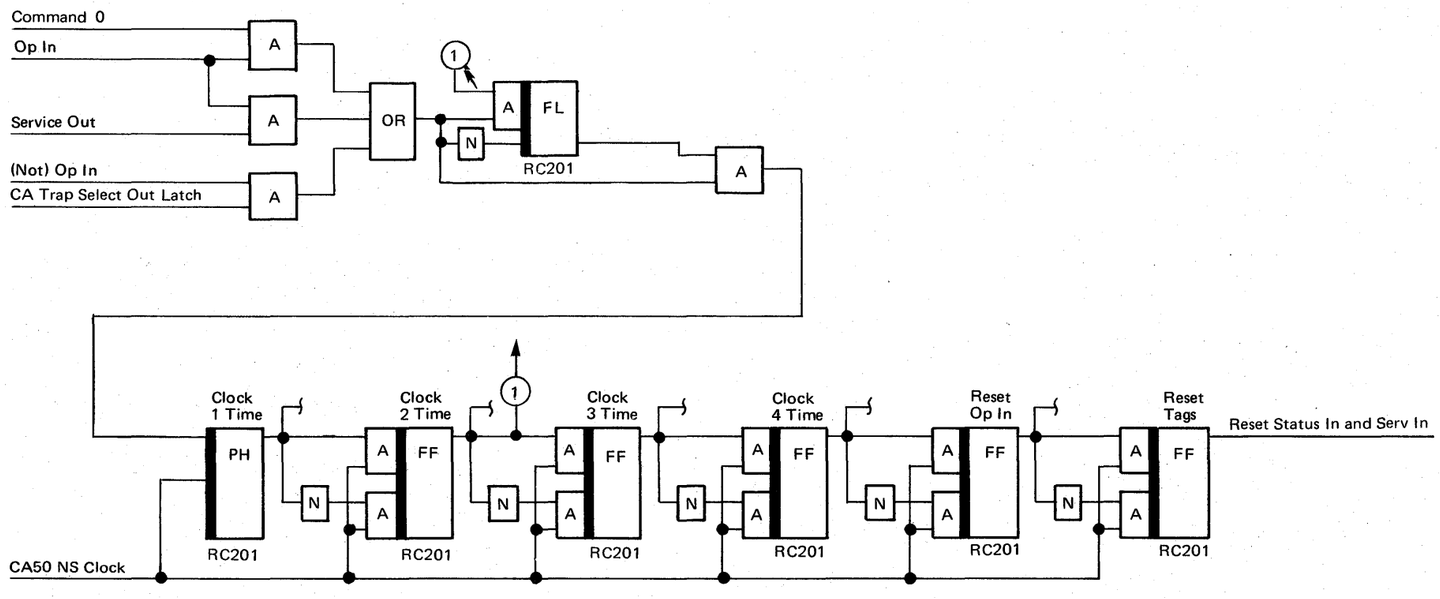
The Output X'62' instruction initiates a channel service cycle to transfer the data from the host CPU to the CA local store.

INBOUND DATA TRANSFER (PART 2)
CA AND CHANNEL TRANSFER DATA

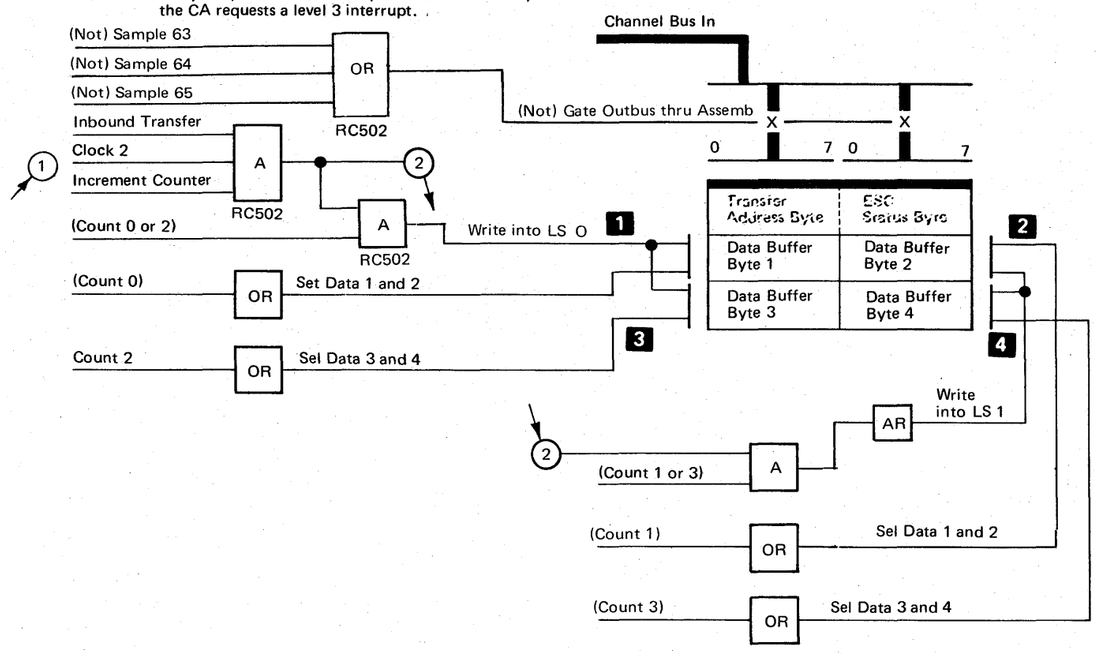
1 After trapping select out, the CA identifies itself to the channel. Refer to page 8-320 for an explanation of 'request in' to the channel.



2 The channel tag clock operates each time the channel and the CA start a data transfer. The clock synchronizes the CA and the channel to handle the data transfer.



3A Data transfers across the channel one byte at a time, and each byte is gated into the local store data buffer. The byte count is incremented for each byte transferred. When the byte count equals the number of bytes specified in the Output X'62' instruction, the CA requests a level 3 interrupt.



1 Loads byte 1 into Data Buffer Byte 1

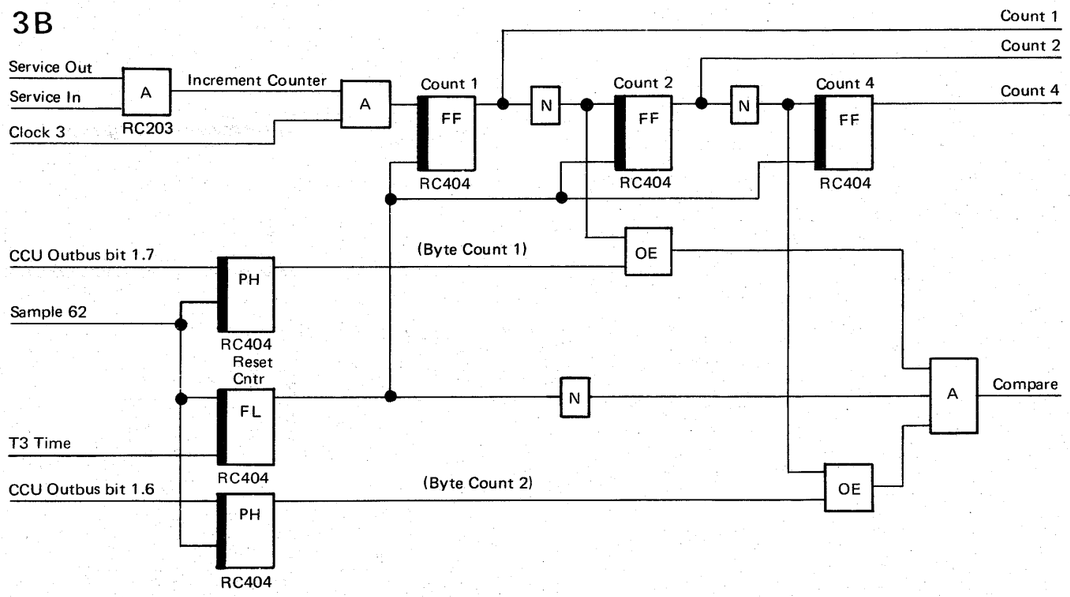
2 Loads byte 2 into Data Buffer Byte 2

3 Loads byte 3 into Data Buffer Byte 3

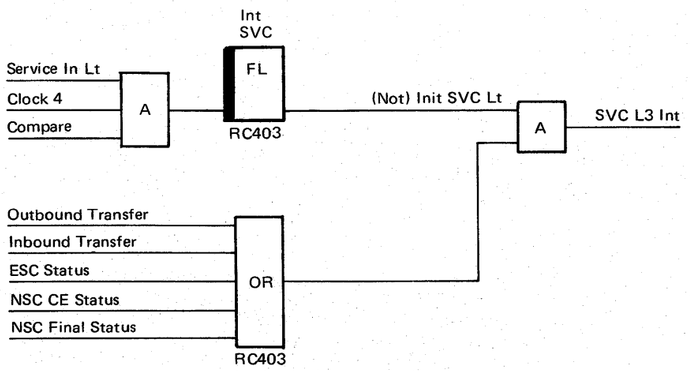
4 Loads byte 4 into Data Buffer Byte 4

INBOUND DATA TRANSFER (PART 3)
CA AND CHANNEL TRANSFER DATA (CONTINUED)

3B



4 When the count of the bytes transferred equals the count specified by the Output X'62' instruction, the CA requests a level 3 data/status interrupt by resetting the initiate service FL.



5 In response to the CA data/status level 3 interrupt, the 3705 control program must execute the following instructions.

Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Input X'77'	0000 0000	0001 0000	Type 1 CA data/status level 3 interrupt.
Input X'62'	0100 0*00	0000 0XXX	0.1 = inbound data transfer *0.5 if on indicates a channel stop condition, and the control program should end the channel command. 1.5-1.7 = the number of bytes transferred.
Input X'63'	Address	0000 0000	Byte 0 = subchannel address Byte 1 = all zeros
Input X'64'	Data byte	Data byte	Byte 0 = data byte 1 (Note 1) Byte 1 = data byte 2 (Note 1)
Input X'65'	Data byte	Data byte	Byte 0 = data byte 3 (Note 1) Byte 1 = data byte 4 (Note 1)
Output X'62'	0100 0010	0000 00XX	0.1 = inbound data transfer 0.6 = reset data service condition (if required). 1.6-1.7 = Indicate the number of bytes of data. (Note 2)

Notes: 1. Execution of Input X'64' and X'65' depends upon how many data bytes are requested.

2. This bit pattern is valid only if the CA is to continue the data transfer. If the transfer is to end, see 8-280.

CA1

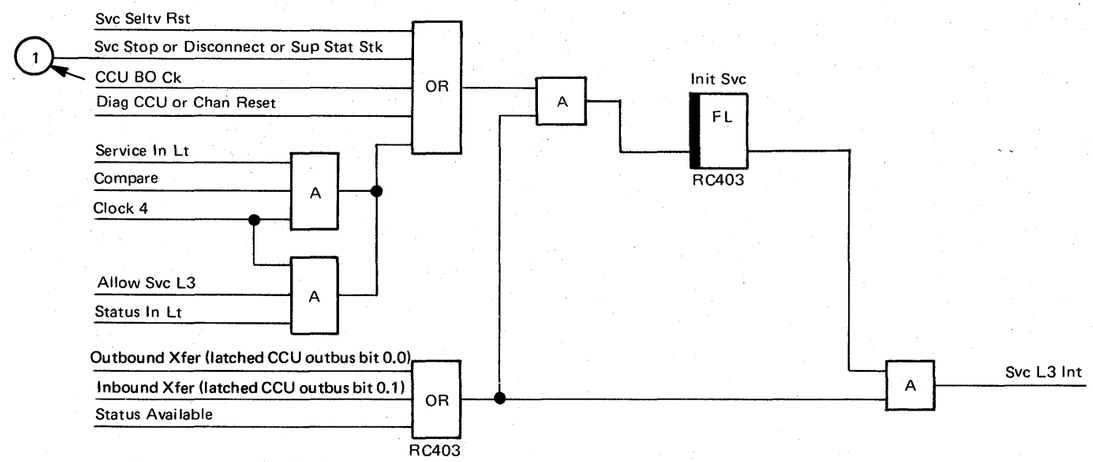
ENDING AN INBOUND TRANSFER

When the host CPU has transferred all the inbound data, a channel stop sequence is initiated. When the 3705 control program executes the Input X'62' instruction in response to the data/status level 3 interrupt, bit 0.5 is transferred to the CCU general register so that the 3705 control program can take appropriate action to end the command. The channel stop sequence initiates a Type 1 CA data/status level 3 interrupt.

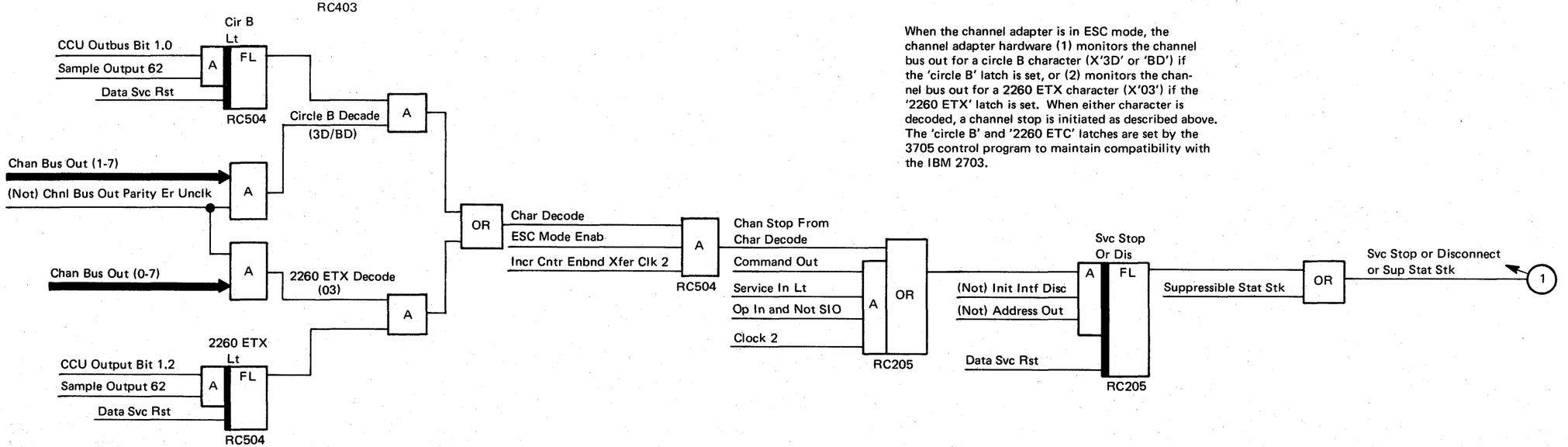
The 3705 control program responds to the data/status level 3 interrupt with the following instructions.

Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Input X'77'	0000 0000	0001 0000	Type 1 CA data/status level 3 interrupt
Input X'63'	Address	0000 0000	Byte 0 = address the channel adapter was serving when channel stop occurred.
Input X'62'	0100 0100	0000 0XXX	0.1 = inbound transfer 0.5 = service stop or disconnect 1.5-1.7 = transferred byte count.

Note: *Where differences exist in NSC and ESC status transfer, NSC information appears on the left, and ESC information on the right of the page.*



When the channel adapter is in ESC mode, the channel adapter hardware (1) monitors the channel bus out for a circle B character (X'3D' or 'BD') if the 'circle B' latch is set, or (2) monitors the channel bus out for a 2260 ETX character (X'03') if the '2260 ETX' latch is set. When either character is decoded, a channel stop is initiated as described above. The 'circle B' and '2260 ETC' latches are set by the 3705 control program to maintain compatibility with the IBM 2703.



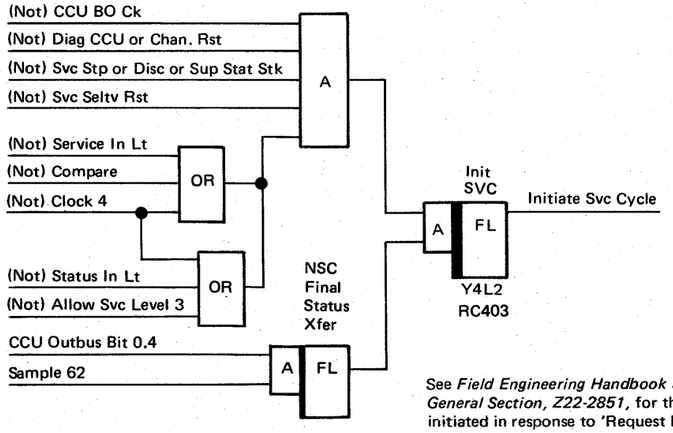
ENDING AN INBOUND TRANSFER (PART 2)

NSC

The 3705 control program must determine what action to take to end the command. When the 3705 control program is ready to present its final status, it executes the following instructions if operating in NSC mode.

Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Output X'63'	Address	0000 0000	byte 0 = subchannel address
Output X'66'	0000 0000	0000 1100	1.0 = Attention 1.1 = Status Modifier 1.2 = 0 1.3 = 0 1.4 = Channel End* 1.5 = Device End* 1.6 = Unit Check 1.7 = Unit Exception
Output X'62'	0000 1000	0000 0000	0.4 = Set NSC Final Status Transfer

*This is the normal final status that should be presented. However, the 3705 control program can present other bits to designate different conditions if needed.



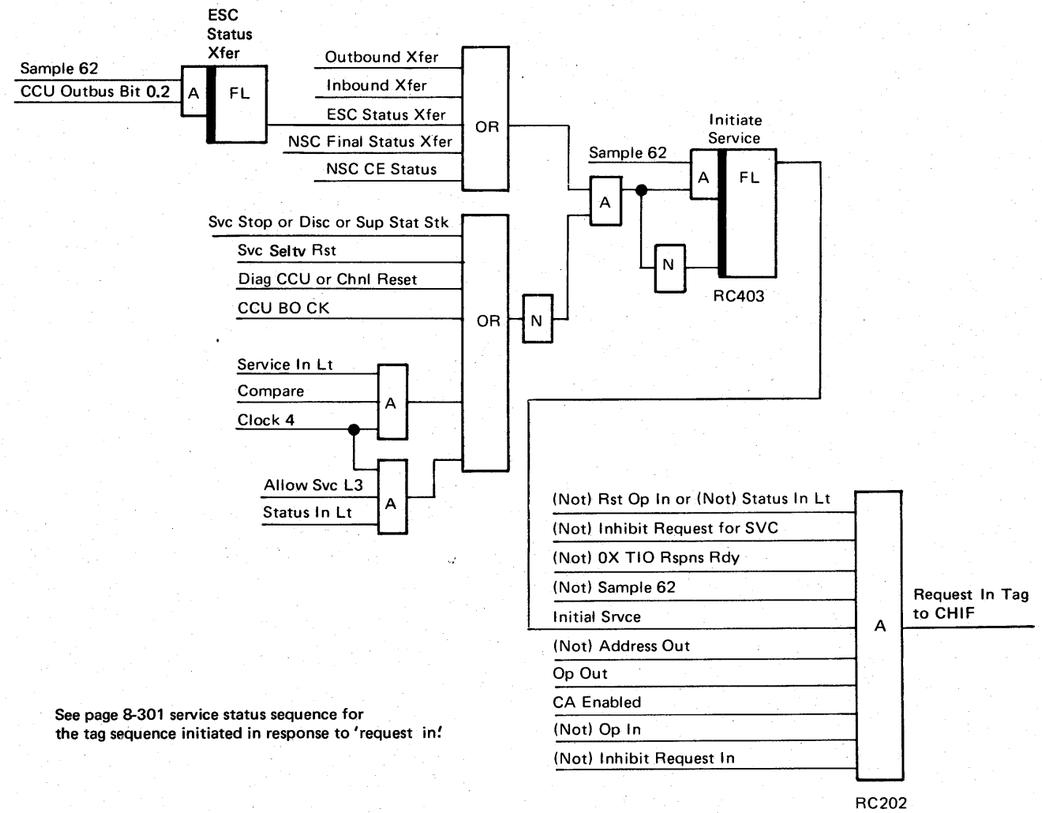
See *Field Engineering Handbook System/360 General Section, Z22-2851,* for the tag sequence initiated in response to 'Request In' from a control unit.

ESC

The 3705 control program executes these instructions to present final status if operating in ESC mode.

Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Output X'63'	Address	0000 1100	Byte 0 = ESC address 1.4 = Channel End* 1.5 = Device End*
Output X'62'	0010 0000	0000 0000	0.2 = ESC status transfer

*These are the normal final status bits. However, the 3705 control program can set other status bits if conditions warrant.



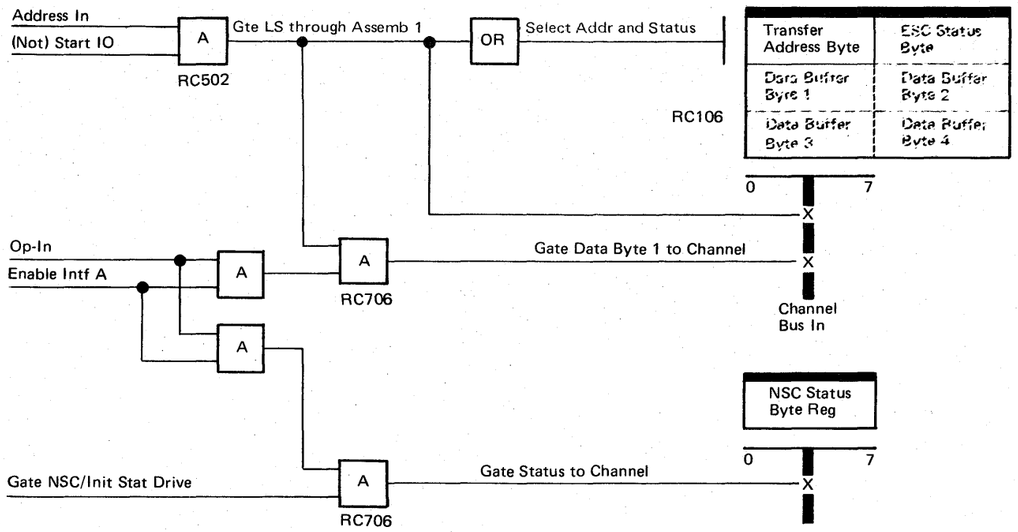
See page 8-301 service status sequence for the tag sequence initiated in response to 'request in'

CA1

ENDING AN INBOUND TRANSFER (PART 3)

NSC

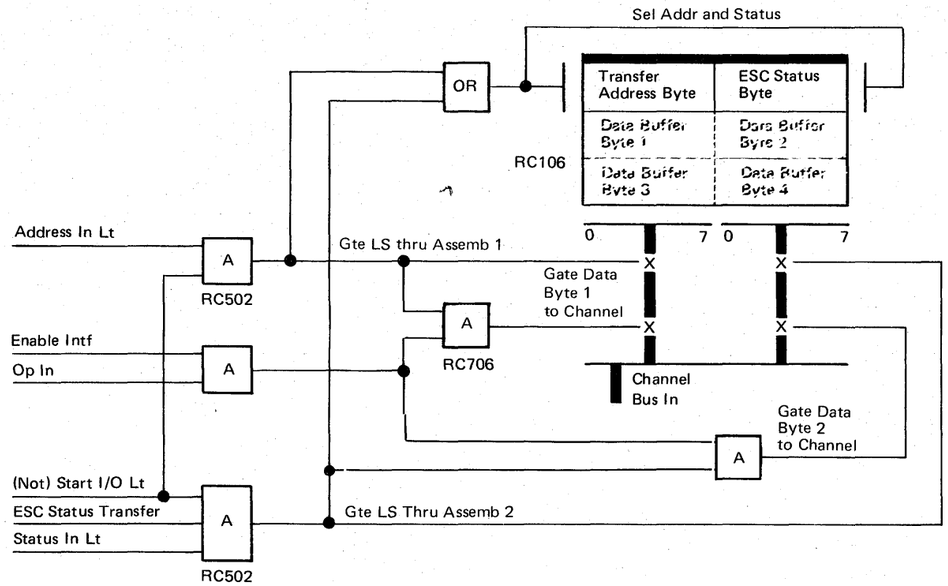
The CA identifies itself to the channel and gates the status byte to the channel 'Bus In'.



'Status in', 'Clock 4' and 'allow svc L3' reset the 'Init Svc' flip latch to request a data/status level 3 interrupt which signals the 3705 Control program that the status transfer is complete.

ESC

The CA identifies itself to the channel and transfers the final status byte to the channel 'Bus In'.



'Status in', 'Clock 4' and 'allow svc L3' reset the 'Init Svc' flip latch to request a data/status level 3 interrupt which signals the 3705 Control program that the status transfer is complete.

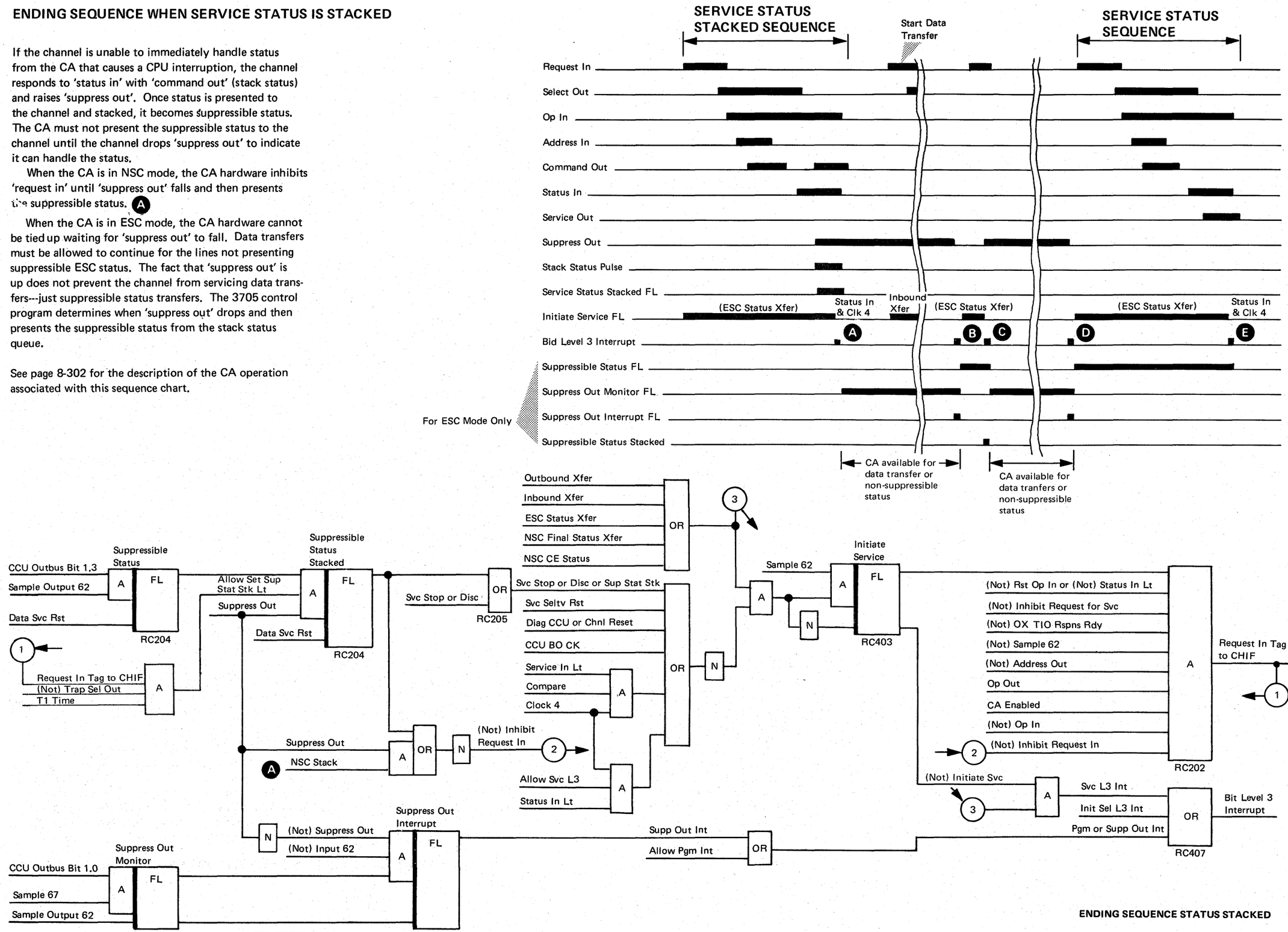
ENDING SEQUENCE WHEN SERVICE STATUS IS STACKED

If the channel is unable to immediately handle status from the CA that causes a CPU interruption, the channel responds to 'status in' with 'command out' (stack status) and raises 'suppress out'. Once status is presented to the channel and stacked, it becomes suppressible status. The CA must not present the suppressible status to the channel until the channel drops 'suppress out' to indicate it can handle the status.

When the CA is in NSC mode, the CA hardware inhibits 'request in' until 'suppress out' falls and then presents the suppressible status. (A)

When the CA is in ESC mode, the CA hardware cannot be tied up waiting for 'suppress out' to fall. Data transfers must be allowed to continue for the lines not presenting suppressible ESC status. The fact that 'suppress out' is up does not prevent the channel from servicing data transfers---just suppressible status transfers. The 3705 control program determines when 'suppress out' drops and then presents the suppressible status from the stack status queue.

See page 8-302 for the description of the CA operation associated with this sequence chart.



ENDING SEQUENCE WHEN SERVICE STATUS IS STACKED (PART 2)

The general sequence of events that occur in the channel interface, the CA, and the 3705 control program for ESC mode is shown in the sequence chart on page 8-301.

The 3705 control program executes Output X'62' to initiate service. This causes 'request in' to start a service status sequence. 'Status in' resets initiate service causing a type 1 CA level 3 interrupt. The 3705 control program must determine that the status has been stacked and that 'suppress out' is up; then turn on the suppress out monitor latch to detect when 'suppress out' is down. The 3705 control program executes the following instructions at (A) in the sequence chart. The CA is now available for data transfers or non-suppressible status for the other ESC lines.

(A)

Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Input X'77'	0000 0000	0001 0000	Type 1 CA data/status level 3 interrupt
Input X'62'	0010 0000	0011 0000	0,2 = ESC status transfer 1,2 = Suppress out 1,3 = Service status stacked
Output X'62'	0000 0010	0000 0000	0,2 = 0 to reset ESC status transfer (inhibits a continuous bid level 3 interrupt) 0,6 = Data service reset (resets service status stacked)
Output X'67'	0000 0000	1000 0000	1,0 = Set suppress out monitor

When 'suppress out' falls, the suppress out interrupt latch turns on causing a type 1 CA level 3 interrupt. The 3705 control program executes the following instructions at (B) in the sequence chart to start another service status sequence to present the suppressible status to the channel. At the same time, the suppressible status latch is set.

(B)

Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Input X'77'	0000 0000	0001 0000	Type 1 CA data/status level 3 interrupt
Input X'62'	0000 0010	0000 0000	0,6 = Suppress out monitor
Output X'62'	0010 0000	0001 0000	0,2 = 1 to set ESC status transfer 1,3 = Set suppressible status Reset suppress out monitor

If for some reason, the channel can not immediately handle any status before it brings up 'select out', the channel raises 'suppress out' again. The suppressible status stacked latch is set when 'request in' and 'suppress out' are up and the suppressible status latch is on. This causes a type 1 CA level 3 interrupt that drops 'request in' and also notifies the 3705 control program the channel can not accept the status. The 3705 control program executes the following instructions at (C) that set the suppress out monitor latch to detect when 'suppress out' falls. The CA is now available for data transfer or non-suppressible status for the other ESC lines.

(C)

Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Input X'77'	0000 0000	0001 0000	Type 1 CA data/status level 3 interrupt
Input X'62'	0010 0000	0011 0000	0,2 = ESC status transfer 1,2 = Suppress out 1,3 = Suppressible status stacked
Output X'62'	0000 0010	0000 0000	0,2 = 0 to reset ESC status transfer (inhibits a continuous bit level 3 interrupt) 0,6 = Data service reset (resets suppressible status) (resets suppressible status stacked)
Output X'67'	0000 0000	1000 0000	1,0 = Set suppress out monitor

When 'suppress out' falls, the suppress out interrupt latch turns on, causing a type 1 CA level 3 interrupt. The 3705 control program executes the following instructions at (D) in the sequence chart to start another service status sequence to present the suppressible status to the channel. At the same time, the suppressible status latch is set.

(D)

Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Input X'77'	0000 0000	0001 0000	Type 1 CA data/status level 3 interrupt
Input X'62'	0000 0010	0000 0000	0,6 = Suppress out monitor
Output X'62'	0010 0010	0001 0000	0,2 = 1 to set ESC status transfer 0,6 = Data service reset 1,3 = Set suppressible status Reset suppress out monitor

'Status in' resets initiate service causing a type 1 CA level 3 interrupt. The 3705 control executes the following instructions at (E) in the sequence chart to determine that the status has been accepted by the channel.

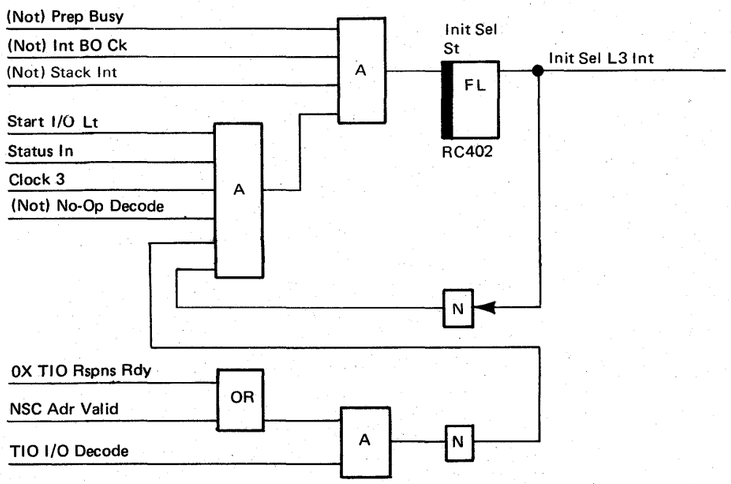
(E)

Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Input X'77'	0000 0000	0001 0000	Type 1 CA data/status level 3 interrupt
Input X'62'	0010 0000	0000 0000	0,2 = ESC status transfer
Output X'62'	0000 0010	0000 0000	0,2 = 0 to reset ESC status transfer (inhibits a continuous bid level 3 interrupt) 0,6 = Data service reset (resets suppressible status)

OUTBOUND DATA TRANSFERS

Outbound data transfers result from channel Read commands that direct the transfer of data from 3705 storage to the host CPU. They are handled by the CA basically the same whether the CA is in ESC or NSC mode. The major difference is the way final status is presented to the channel.

CA DECODES THE COMMAND AND REQUESTS AN INTERRUPT



The 3705 control program responds to the initial select level 3 interrupt with the following instructions.

Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Input X'77'	0000 0000	0000 1000	Type 1 CA initial selection level 3 interrupt
Input X'60'	1000 0000	0000 0000	Normal initial selection (Note 1)
Input X'61'	address	command	Byte 0 = address byte 1 = command
Output X'63'	address	0000 0000	byte 0 = transfer address byte 1 = all zeros
Output X'64'	data	data	Byte 0 = data byte 1 byte 1 = data byte 2
Output X'65'	data	data	byte 0 = data byte 3 byte 1 = data byte 4
Output X'62'	1000 0110	0000 0000	0.0 = outbound data transfer 0.5 = reset initial selection 0.6 = reset data/status control 1.6-1.7 = 0 to transfer four bytes (Note 2)

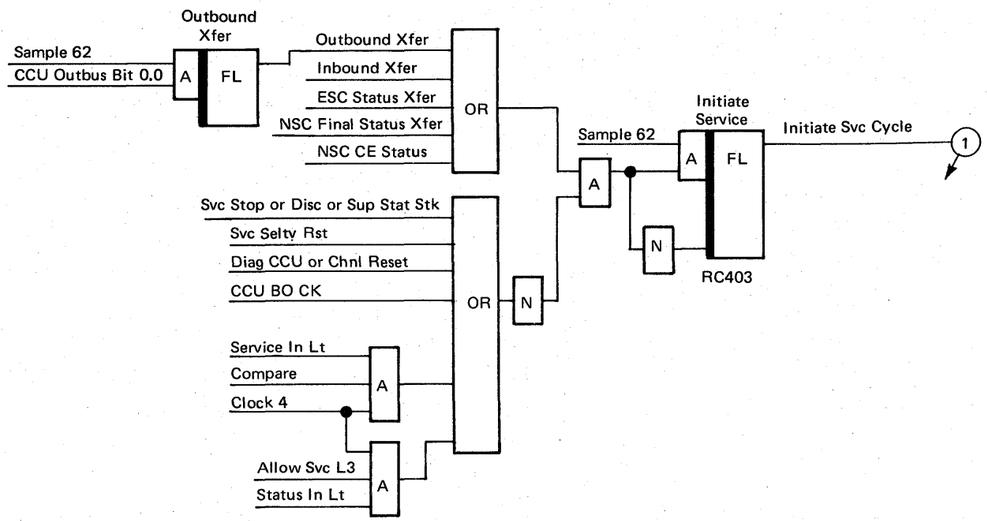
Notes: 1. Other bits may be transferred to the CCU during this input. If other bits are on, the 3705 control program must take action differently from the normal initial selection.

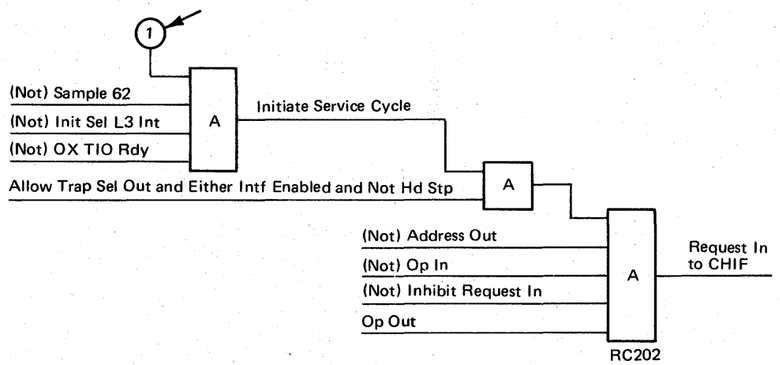
2. From one to four bytes of data may be transferred to the channel. If less than four are to be transferred, the Output X'64' and X'65' vary accordingly.

OUTBOUND DATA TRANSFERS (PART 2)

CA AND CHANNEL TRANSFER DATA

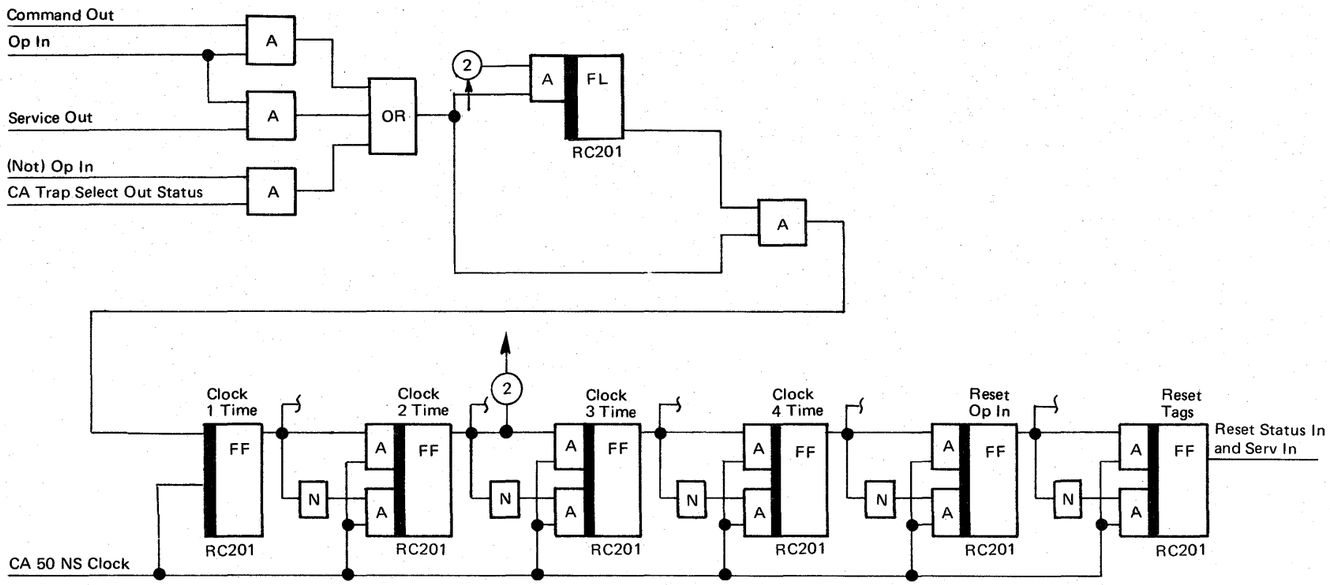
The Output X'62' instruction starts a channel service cycle so that the data loaded into the data buffer bytes can be transferred to the channel.





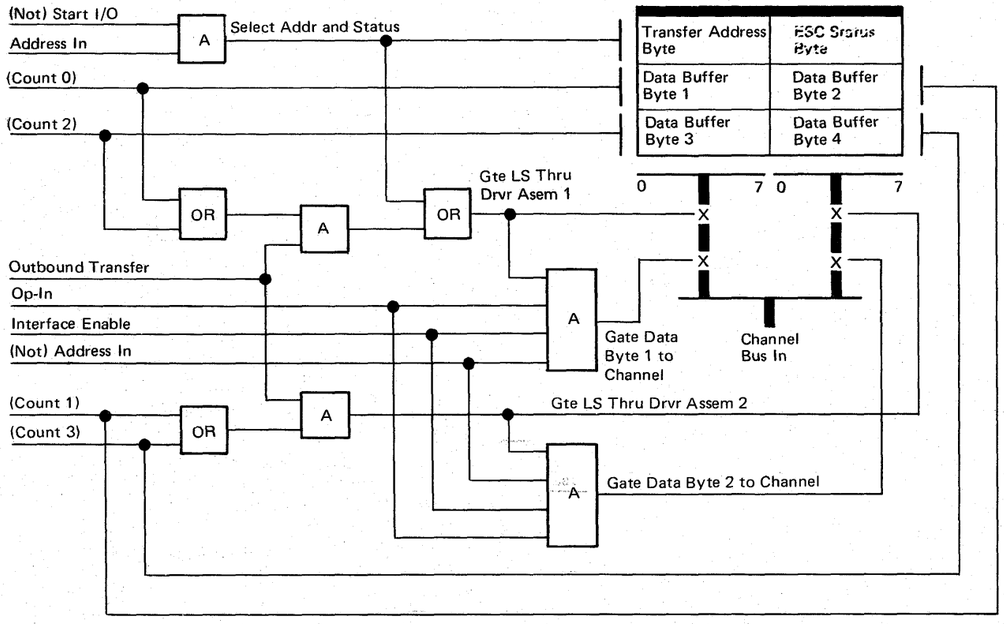
See page 8-380 for the tag sequence resulting from 'request in' to the channel. The data is gated on bus in by 'service in' because this is an outbound data transfer instead of an inbound data transfer as shown.

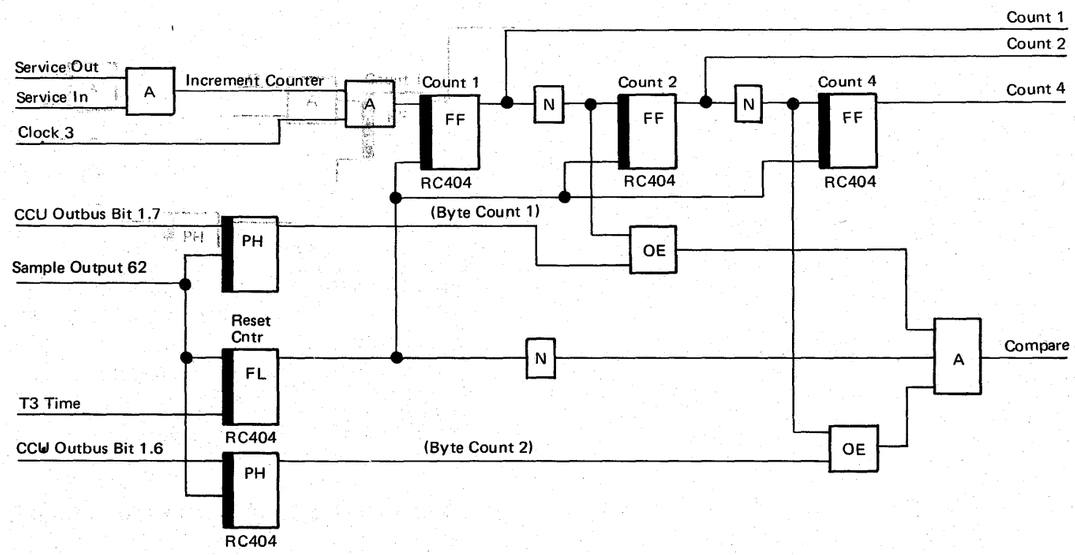
The channel tag clock operates, each time the channel and the CA start a data transfer. The clock synchronizes the CA and the channel to handle the data transfer.



Outbound Data Transfers (Part 3)
CA and Channel Transfer Data (Continued)

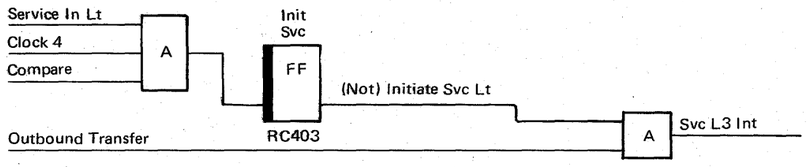
The CA transfers the data to the channel 'Bus In' one byte at a time. As each byte is transferred across the channel interface, the byte count is incremented.





CA AND CCU TRANSFER DATA

When the number of bytes transferred across the channel interface equals the number specified in the byte count, the CA requests a type 1 CA data/status level 3 interrupt.



The 3705 control program responds to the level 3 data/status interrupt with the following instructions.

Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Input X'77'	0000 0000	0001 0000	Type 1 CA data status level 3 interrupt
Input X'62'	1000 0000	0000 0100	0.0 = outbound data transfer 1.5 = number of bytes transferred in (four indicated by bit 1.5)
Output X'64'	Data byte	Data byte	Byte 0 = data byte 1 Byte 1 = data byte 2
Output X'65'	Data byte	Data byte	Byte 0 = data byte 3 Byte 1 = data byte 4
Output X'62'	1000 0010	0000 0000	0.0 = outbound data transfer 0.6 = reset data service condition 1.6 and 1.7 off indicate transfer in four bytes.

CA1

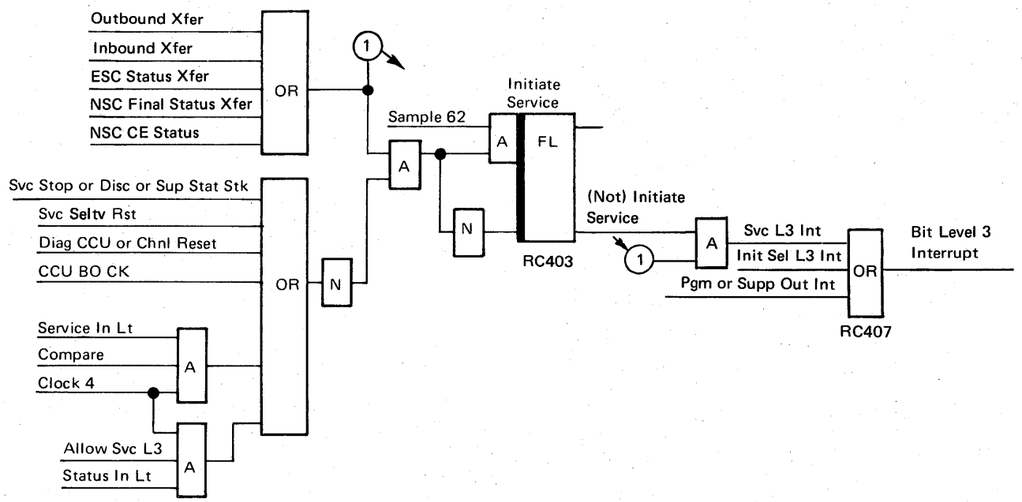
ENDING AN OUTBOUND TRANSFER

Outbound data transfers can be ended either by the host CPU or the 3705 control program. The host CPU ends the transfer by initiating a channel stop sequence or with a Halt I/O. The 3705 control program ends the transfer by initiating a status transfer rather than a data transfer.

Note: There are some differences in the NSC and ESC status presentation. Where differences exist, NSC information appears on the left, and ESC information appears on the right of the page.

CHANNEL INITIATES A CHANNEL STOP

When the host CPU has transferred all the data it has to transfer with the active command, it begins a channel stop sequence to signal the 3705.



The 3705 control program responds to the data/status level 3 interrupt with the following instructions.

Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Input X'77'	0000 0000	0001 0000	Type 1 CA data/status level 3 interrupt
Input X'62'	1000 0100	0000 0XXX	0.0 = Outbound transfer 0.5 = Channel Stop or Intf disconnect 1.5-1.7 = Number of bytes transferred
Input X'61'	Address	Command	Byte 0 = last address presented to the CA* Byte 1 = last command presented to the CA*
Input X'63'	Address	0000 0000	Byte 0 = address CA was serving when channel stop occurred Byte 1 = should be all zeros unless a status byte was loaded into the register.

* If the CA received a new channel command while still processing the previous command, the contents of the initial selection address and command byte register change to reflect the new command and address. The Input X'63' provides the address that was being served when the stop sequence occurred.

ENDING AN OUTBOUND TRANSFER (PART 2)

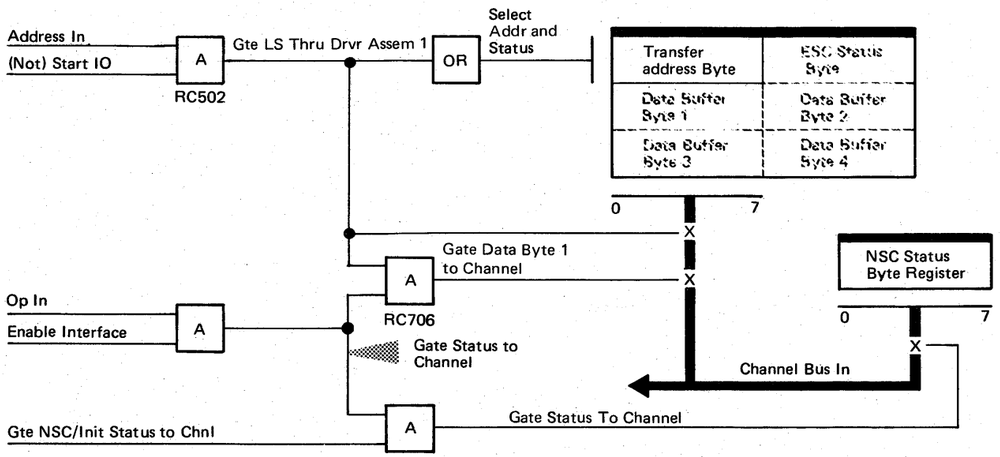
NSC

The 3705 control program executes the following instructions to present the final status to the channel.

Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Output X'63'	address	0000 0000	Byte 0 = Subchannel address whose status is being presented. (Note 1)
Output X'66'	0000 0000	0000 1100	1.0 = Attention 1.1 = Status Modifier 1.2 = * (Not used) 1.3 = * (Not used) 1.4 = Channel End (Note 2) 1.5 = Device End (Note 2) 1.6 = Unit Check 1.7 = Unit Exception
Output X'62'	0000 1000	0000 0000	0.4 = Set NSC final status transfer.

Notes: 1. In NSC mode, this address should not change from transfer to transfer. The 3705 control program may not need to reload the address into this register after it has been loaded correctly the first time.

2. This is the normal final status that should be presented to the channel. However, the 3705 control program can determine whether additional status bits should be presented.



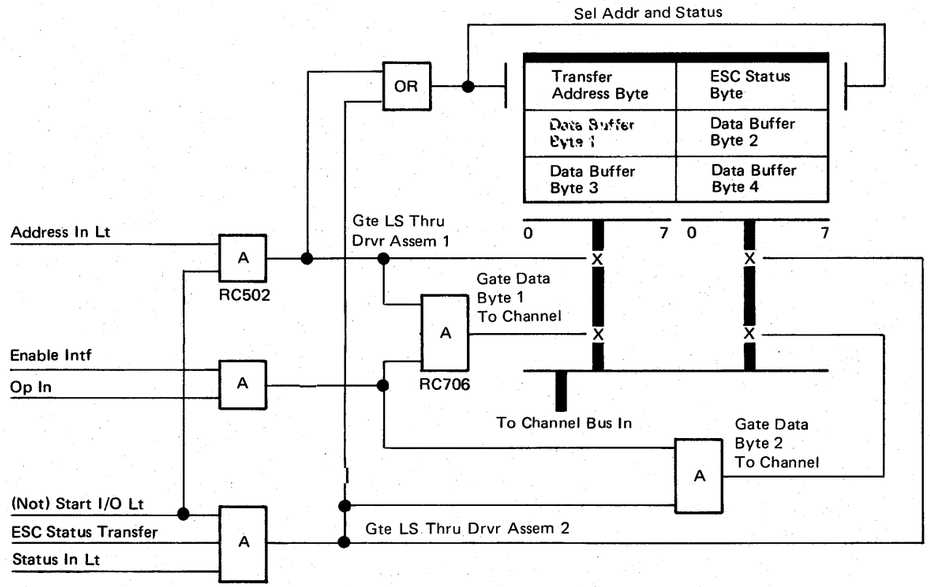
'Status In', 'Clock 4', and 'allow svc L3' reset the 'Init Svc' flip latch to request a data/status level 3 interrupt which signals the 3705 control program that the status transfer is complete.

ESC

The 3705 control program executes the following instructions to present the final status to the channel.

Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Output X'63'	address	0000 1100	Byte 0 = subchannel address to which the status is to be presented. 1.0 = Attention 1.1 = Status Modifier 1.2 = Control Unit End 1.3 = Busy 1.4 = Channel End (See Note) 1.5 = Device End (See Note) 1.6 = Unit Check 1.7 = Unit Exception
Output X'62'	0010 0000	0000 0000	0.2 = ESC status transfer

Note: This is the normal final status to present to the channel. However, the 3705 control program can determine if other bits should be presented.



'Status In', 'Clock 4', and 'allow svc L3' reset the 'Init Svc' flip latch to request a data/status level 3 interrupt which signals the 3705 control program that the status transfer is complete.

CA1

CA ERROR INTERRUPTS

The type I channel adapter requests a level 1 interrupt whenever:

- A channel 'Bus-In' check occurs.

  The channel adapter hardware detects bad parity in the data byte being sent across the channel to the CPU.
  The control program should respond to the interrupt with an Input X'67' instruction to transfer the contents of the error condition register to the CCU. Bit 1.0 should be transferred if a channel 'Bus-In' check occurred.

- An in/out instruction accept check occurs.

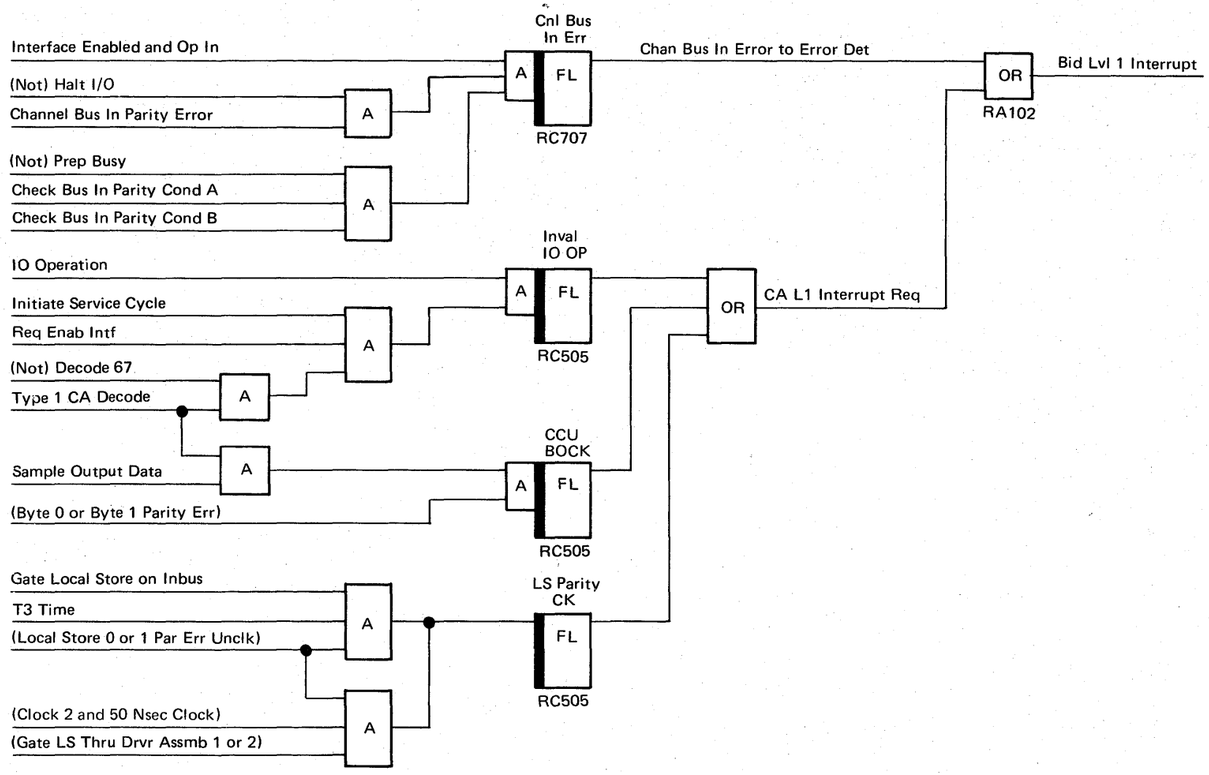
  An in/out instruction accept check (invalid I/O op) occurs if the control program executes an Input or Output X'60' X'61', X'62', X'63', X'64', X'65', or X'66' instruction while the CA is actively handling any data or status transfer sequence. When the control program responds to the level 1 interrupt with an Input X'67', bit 1.1 is transferred to the CCU.

- A 'CCU Outbus' check occurs.

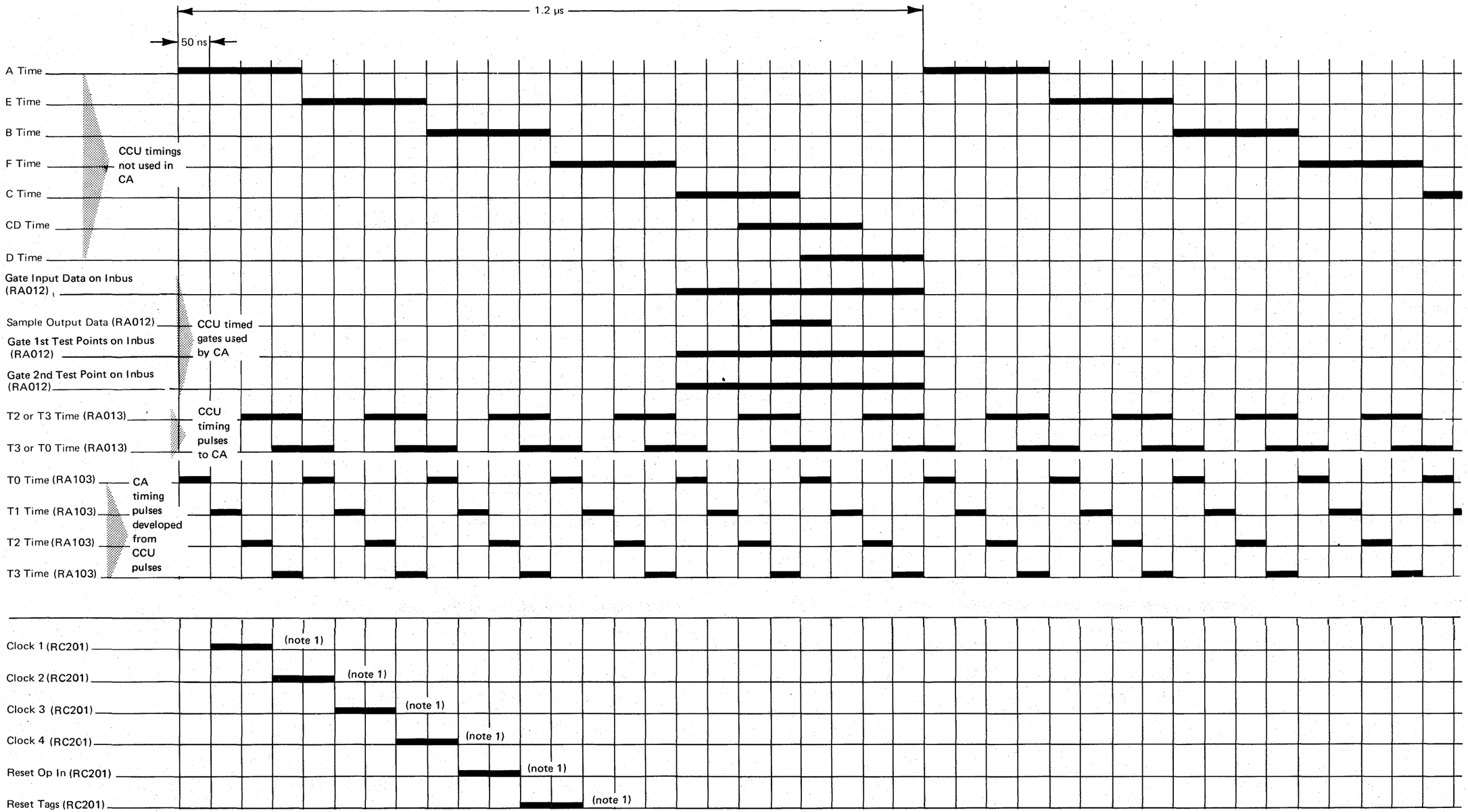
  When bad parity is detected on the 'CCU Outbus', the CA requests a level 1 interrupt. Bit 1.2 is returned to the CCU from the error condition register when the control program executes an Input X'67' instruction in response to the interrupt.

- A local store check occurs.

  Bad parity being gated from the local store registers causes a level 1 interrupt request. Bit 1.3 is returned to the CCU from the error condition register when the control program executes an Input X'67' instruction in response to the interrupt.



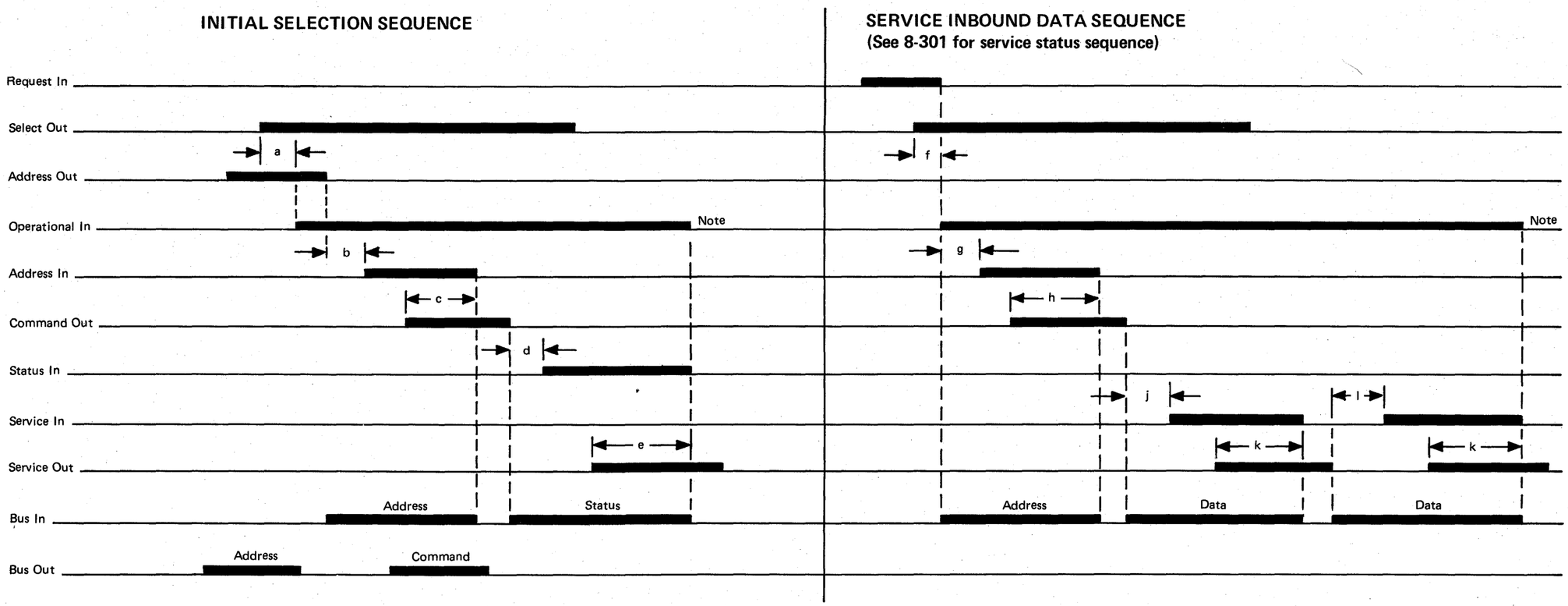
CA TIMING



Note:
1. Clock times are not related to A, E, B, etc time, and clock times occur on either T1 or T3 time.

CA1

CHANNEL INTERFACE SEQUENCES



a - Rise of 'select out' inbound to rise of 'operational in' ——— 200-350ns
b - Rise of 'address in' after the fall of 'address out' ——— 300-350ns
c - Fall of 'address in' after the rise of 'command out' ——— 400-500ns
d - Rise of 'status in' after the fall of 'command out' ——— 300-350ns
e - Fall of 'status in' after the rise of 'service out' ——— 500-600ns
f - Fall of 'request in' after the rise of 'select out' inbound ——— 200-350ns
Rise of 'operational in' after the rise of 'select out' inbound —— 200-250ns
g - Rise of 'address in' after the rise of 'operational in' ——— 350ns
h - Fall of 'address in' after the rise of 'command out' ——— 400-500ns
j - Rise of 'service in' after the fall of 'command out' ——— 300-350ns
k - Fall of 'service in' after the rise of 'service out' ——— 500-600ns
l - Rise of 'service in' after the fall of 'service out' ——— 300-350ns

Note: 'Operational in' falls as shown provided 'select out' is down. If 'select out' is up when 'status in' or 'service in' falls, 'operational in' falls with the fall of 'select out'.

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